LAN9730/LAN9730i

High-Speed Inter-Chip (HSIC) USB 2.0 to 10/100 Ethernet Controller

PRODUCT FEATURES

Datasheet

Highlights

- Single Chip HSIC USB 2.0 to 10/100 Ethernet Controller
- Integrated 10/100 Ethernet MAC with Full-Duplex Support
- Integrated 10/100 Ethernet PHY with HP Auto-MDIX Support
- Integrated USB 2.0 Hi-Speed Device Controller
- Integrated HSIC Interface
- Implements Reduced Power Operating Modes

Target Applications

- Embedded Systems
- Set-Top Boxes
- PVRs
- CE Devices
- Networked Printers
- USB Port Replicators
- Test Instrumentation
- Industrial

Key Features

- USB Device Controller
  - Fully compliant with Hi-Speed Universal Serial Bus Specification, revision 2.0
  - Supports HS (480 Mbps) mode
  - Four Endpoints supported
  - Supports vendor specific commands
  - Integrated HSIC Interface
  - Remote wakeup supported
- High-Performance 10/100 Ethernet Controller
  - Fully compliant with IEEE 802.3/802.3u
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full- and half-duplex support
  - Full- and half-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Loop-back modes
  - TCP/UDP/IP/ICMP checksum offload support
  - Flexible address filtering modes
    - One 48-bit perfect address
    - 64 hash-filtered multicast addresses
    - Pass all multicast
    - Promiscuous mode
    - Inverse filtering
    - Pass all incoming with status report
  - Wakeup packet support
  - Integrated Ethernet PHY
    - Auto-negotiation
    - Automatic polarity detection and correction
    - HP Auto-MDIX support
    - Link status change wake-up detection
  - Support for three status LEDs
  - External MII and Turbo MII support HomePNA® and HomePlug® PHY
- Power and I/Os
  - Various low power modes
  - Supports PCI-like PME wake when USB Host disabled
  - 11 GPIOs
  - Supports bus-powered and self-powered operation
  - Integrated power-on reset circuit
  - Single external 3.3 V I/O supply
    - Optional internal core regulator
- Miscellaneous Features
  - EEPROM controller
  - Supports custom operation without EEPROM
  - IEEE 1149.1 (JTAG) boundary scan
  - Requires single 25 MHz crystal
- Software
  - Windows® 7/XP/Vista driver
  - Linux® driver
  - Win CE driver
  - MAC® OS driver
  - EEPROM utility
- Packaging
  - 56-pin QFN (8x8 mm) lead-free, RoHS compliant
- Environmental
  - Commercial Temperature Range (0°C to +70°C)
  - Industrial Temperature Range (-40°C to +85°C)

Order Numbers:

LAN9730-ABZJ (Tray) for 56-pin, QFN lead-free RoHS compliant package (0 to +70°C temp)

LAN9730i-ABZJ (Tray) for 56-pin, QFN lead-free RoHS compliant package (-40 to +85°C temp)

LAN9730-ABZJ-TR (Tape & Reel) for 56-pin, QFN lead-free RoHS compliant package (0 to +70°C temp)

LAN9730i-ABZJ-TR (Tape & Reel) for 56-pin, QFN lead-free RoHS compliant package (-40 to +85°C temp)

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

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Chapter 1 Introduction

1.1 Block Diagram

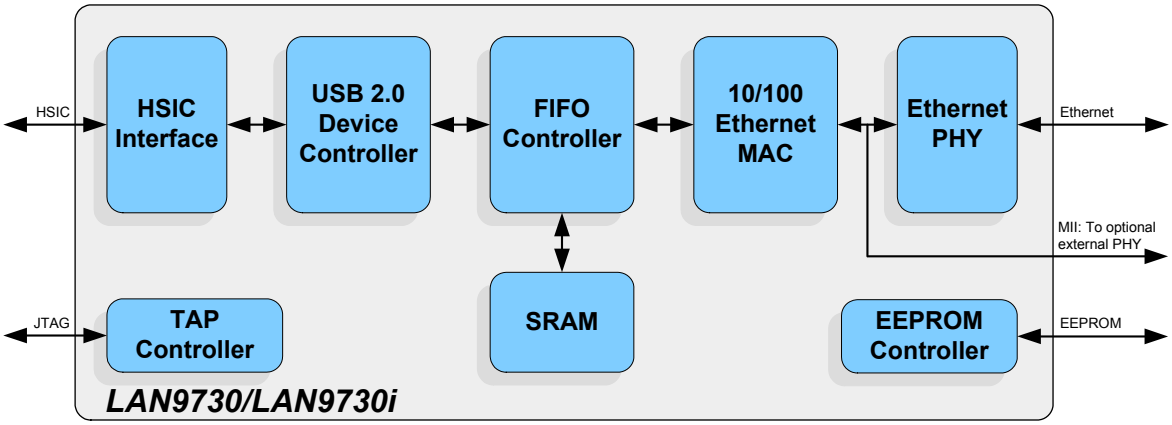


Figure 1.1 LAN9730/LAN9730i Block Diagram

1.2 Overview

The LAN9730/LAN9730i is a high performance solution for USB to 10/100 Ethernet port bridging. With applications ranging from embedded systems, set-top boxes, and PVRs, to USB port replicators, and test instrumentation, the device is targeted as a high-performance, low-cost USB/Ethernet connectivity solution.

The LAN9730/LAN9730i contains an integrated 10/100 Ethernet PHY, HSIC interface, Hi-Speed USB 2.0 device controller, 10/100 Ethernet MAC, TAP controller, EEPROM controller, and a FIFO controller with a total of 30 kB of internal packet buffering.

The internal USB 2.0 device controller is compliant with the USB 2.0 Hi-Speed standard. The HSIC interface is compliant with the High-Speed Interchip USB Electrical Specification Revision 1.0. High-Speed Inter-Chip (HSIC) is a digital interconnect bus that enables the use of USB technology as a low-power chip-to-chip interconnect at speeds up to 480 Mb/s. The device implements Control, Interrupt, Bulk-in and Bulk-out USB Endpoints.

The Ethernet controller supports auto-negotiation, auto-polarity correction, HP Auto-MDIX, and is compliant with the IEEE 802.3 and 802.3u standards. An external MII interface provides support for an external Fast Ethernet PHY, HomePNA, and HomePlug functionality.

Multiple power management features are provided, including various low-power modes, and Magic Packet, Wake On LAN and Link Status Change wake events. These wake events can be programmed to initiate a USB remote wakeup. A PCI-like PME wake is also supported when the Host controller is disabled.

An internal EEPROM controller exists to load various USB configuration information and the device MAC address. The integrated IEEE 1149.1 compliant TAP controller provides boundary scan via JTAG.

1.2.1 USB

The USB portion of the LAN9730/LAN9730i integrates a Hi-Speed USB 2.0 device controller and HSIC interface.

The USB device controller (UDC) contains a USB low-level protocol interpreter which implements the USB bus protocol, packet generation/extraction, PID/Device ID parsing and CRC coding/decoding, with autonomous error handling. The USB device controller is capable of operating in USB 2.0 Hi-Speed mode and contains autonomous protocol handling functions such as handling of suspend/resume/reset conditions, remote wakeup, and stall condition clearing on Setup packets. The USB device controller also autonomously handles error conditions such as retry for CRC and data toggle errors, and generates NYET, STALL, ACK and NACK handshake responses, depending on the Endpoint buffer status.

The LAN9730/LAN9730i implements four USB Endpoints: Control, Interrupt, Bulk-in, and Bulk-out. The Bulk-in and Bulk-out Endpoints allow for Ethernet reception and transmission respectively. Implementation of vendor-specific commands allows for efficient statistics gathering and access to the device's system control and status registers.

The integrated HSIC interface is compliant with the High-Speed Interchip USB Electrical Specification Revision 1.0 (09-23-07) and supports the Hi-Speed mode of operation.

1.2.2 FIFO Controller

The FIFO controller uses an internal SRAM to buffer RX and TX traffic. Bulk-out packets from the USB controller are directly stored into the TX buffer. Ethernet frames are directly stored into the RX buffer and become the basis for bulk-in packets.

1.2.3 Ethernet

LAN9730/LAN9730i integrates an IEEE 802.3 PHY for twisted pair Ethernet applications and a 10/100 Ethernet Media Access Controller (MAC).

The PHY can be configured for either 100 Mbps (100BASE-TX) or 10 Mbps (10BASE-T) Ethernet operation in either Full or Half Duplex configurations. The PHY block includes auto-negotiation, auto-polarity correction, and Auto-MDIX. Minimal external components are required for the utilization of the Integrated PHY.

Optionally, an external PHY may be used via the MII (Media Independent Interface) port, effectively bypassing the internal PHY. This option allows support for HomePNA and HomePlug applications.

The Ethernet MAC/PHY supports numerous power management wakeup features, including Magic Packet, Wake on LAN and Link Status Change. Eight wakeup frame filters are provided by the device.

1.2.4 Power Management

The LAN9730/LAN9730i features four variations of USB suspend: SUSPEND0, SUSPEND1, SUSPEND2 and SUSPEND3. These modes allow the application to select the ideal balance of remote wakeup functionality and power consumption.

- **SUSPEND0:** Supports GPIO, Wake On LAN and Magic Packet events. This state reduces power by stopping the clocks of the MAC and other internal modules.
- **SUSPEND1:** Supports GPIO and Link Status Change for remote wakeup events. This suspend state consumes less power than SUSPEND0.
- **SUSPEND2:** Supports only GPIO assertion for a remote wakeup event. This is the default suspend mode for the device.
- **SUSPEND3:** Supports GPIO and Good Packet events. A Good Packet is a received frame passing certain filtering constraints independent of those imposed on Wake On LAN and Magic Packet frames. This suspend state consumes power at a level similar to the full operational state, however, it allows for power savings in the Host CPU.

1.2.5 EEPROM Controller (EPC)

LAN9730/LAN9730i contains an EEPROM controller for connection to an external EEPROM. This allows for the automatic loading of static configuration data upon power-on reset, pin reset or software reset. The EEPROM can be configured to load USB descriptors, USB device configuration and MAC address.

1.2.6 General Purpose I/O

When configured for Internal PHY Mode, up to eleven GPIOs are supported. All GPIOs can serve as remote wakeup events when the LAN9730/LAN9730i is suspended.

1.2.7 System Software

LAN9730/LAN9730i software drivers are available for the following operating systems:

- Windows 7
- Windows Vista
- Windows XP
- Linux
- Win CE
- MAC OS

In addition, an EEPROM programming utility is available for configuring the external EEPROM.

Chapter 2 Pin Description and Configuration

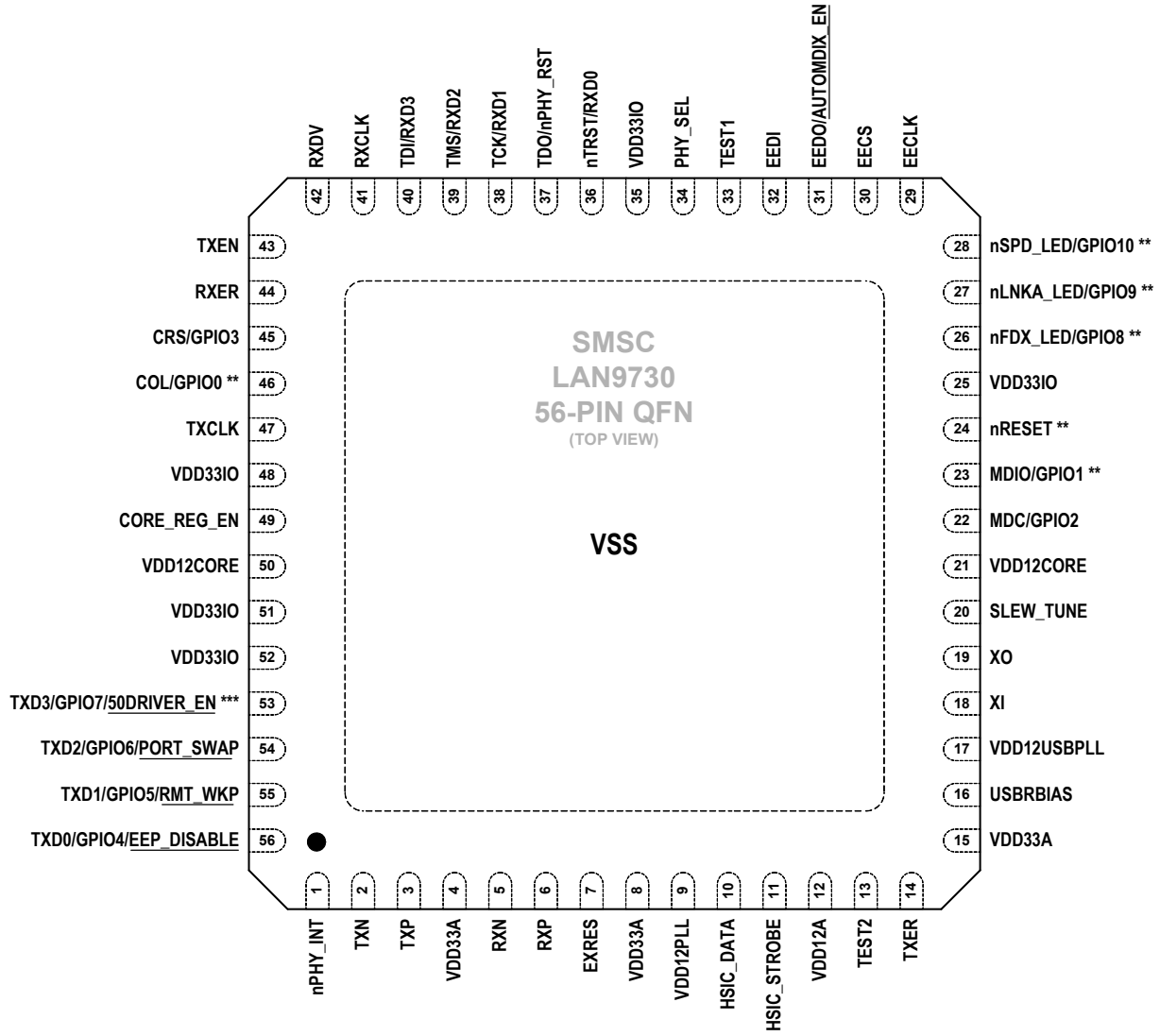


Figure 2.1 Pin Assignments (TOP VIEW)

Note: ** This pin provides additional PME related functionality. Refer to the respective pin descriptions and Chapter 5, "PME Operation," on page 37 for additional information.

Note: *** GPIO7 may provide additional PHY Link Up related functionality.

Note: When HP Auto-MDIX is activated, the TXN/TXP pins can function as RXN/RXP and vice-versa.

Note: Exposed pad (VSS) on bottom of package must be connected to ground.

Table 2.1 MII Interface Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Receive Error (Internal PHY Mode)	RXER	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal.
	Receive Error (External PHY Mode)	RXER	IS (PD)	In External PHY Mode, the signal on this pin is input from the external PHY and indicates a receive error in the packet.
1	Transmit Error (Internal PHY Mode)	TXER	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal.
	Transmit Error (External PHY Mode)	TXER	O8 (PD)	In External PHY Mode, this pin functions as an output to the external PHY and indicates a transmit error.
1	Transmit Enable (Internal PHY Mode)	TXEN	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal.
	Transmit Enable (External PHY Mode)	TXEN	O8 (PD)	In External PHY Mode, this pin functions as an output to the external PHY and indicates valid data on TXD[3:0].
1	Receive Data Valid (Internal PHY Mode)	RXDV	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal.
	Receive Data Valid (External PHY Mode)	RXDV	IS (PD)	In External PHY Mode, the signal on this pin is input from the external PHY and indicates valid data on RXD[3:0].
1	Receive Clock (Internal PHY Mode)	RXCLK	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal.
	Receive Clock (External PHY Mode)	RXCLK	IS (PD)	In External PHY Mode, this pin is the receiver clock input from the external PHY.
1	Transmit Clock (Internal PHY Mode)	TXCLK	IS/O8 (PU)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal.
	Transmit Clock (External PHY Mode)	TXCLK	IS (PU)	In External PHY Mode, this pin is the transmitter clock input from the external PHY.

Table 2.1 MII Interface Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Carrier Sense (Internal PHY Mode)	CRS	IS/O8 (PU)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal.
	Carrier Sense (External PHY Mode)	CRS	IS (PD)	In External PHY Mode, the signal on this pin is input from the external PHY and indicates a network carrier.
	General Purpose I/O 3 (Internal PHY Mode Only)	GPIO3	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input.
1	MII Collision Detect (Internal PHY Mode)	COL	IS/O8 (PU)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal.
	MII Collision Detect (External PHY Mode)	COL	IS (PD)	In External PHY Mode, the signal on this pin is input from the external PHY and indicates a collision event.
	General Purpose I/O 0 (Internal PHY Mode Only)	GPIO0	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. **Note:** This pin may be used to signal PME when Internal PHY and PME Modes of operation are in effect. Refer to Chapter 5, "PME Operation," on page 37 for additional information.
1	Management Data (Internal PHY Mode)	MDIO	IS/O8 (PU)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal.
	Management Data (External PHY Mode)	MDIO	IS/O8 (PD)	In External PHY Mode, this pin provides the management data to/from the external PHY.
	General Purpose I/O 1 (Internal PHY Mode Only)	GPIO1	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. **Note:** This pin may serve as the PME_MODE_SEL input when Internal PHY and PME Modes of operation are in effect. Refer to Chapter 5, "PME Operation," on page 37 for additional information.

Table 2.1 MII Interface Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Management Clock (Internal PHY Mode)	MDC	IS/O8 (PU)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal.
	Management Clock (External PHY Mode)	MDC	O8 (PD)	In External PHY Mode, this pin outputs the management clock to the external PHY.
	General Purpose I/O 2 (Internal PHY Mode Only)	GPIO2	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input.
1	Transmit Data 3 (Internal PHY Mode)	TXD3	IS/O8 (PU)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal.
	Transmit Data 3 (External PHY Mode)	TXD3	O8 (PU)	In External PHY Mode, this pin functions as the transmit data 3 output to the external PHY.
	General Purpose I/O 7 (Internal PHY Mode Only)	GPIO7	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. **Note:** GPIO7 may provide additional external PHY Link Up related functionality.
	HSIC Output Impedance Configuration Strap	50DRIVER_EN	IS (PU)	The 50DRIVER_EN strap selects the driver output impedance for the HSIC_DATA and HSIC_STROBE pins. 0 = 40 Ω output impedance 1 = 50 Ω output impedance See Note 2.1 for more information on configuration straps.

Table 2.1 MII Interface Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Transmit Data 2 (Internal PHY Mode)	TXD2	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal.
	Transmit Data 2 (External PHY Mode)	TXD2	O8 (PD)	In External PHY Mode, this pin functions as the transmit data 2 output to the external PHY.
	General Purpose I/O 6 (Internal PHY Mode Only)	GPIO6	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
	HSIC Port Swap Configuration Strap	PORT_SWAP	IS (PD)	Swaps the mapping of HSIC_DATA and HSIC_STROBE. 0 = The HSIC_DATA and HSIC_STROBE pin functionality is not swapped. 1 = The HSIC_DATA and HSIC_STROBE pin functionality is swapped. See Note 2.1 for more information on configuration straps.
1	Transmit Data 1 (Internal PHY Mode)	TXD1	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal.
	Transmit Data 1 (External PHY Mode)	TXD1	O8 (PD)	In External PHY Mode, this pin functions as the transmit data 1 output to the external PHY.
	General Purpose I/O 5 (Internal PHY Mode Only)	GPIO5	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input.
	Remote Wakeup Configuration Strap	RMT_WKP	IS (PD)	This strap configures the default descriptor values to support remote wakeup. This strap is overridden by the EEPROM. 0 = Remote wakeup is not supported. 1 = Remote wakeup is supported. See Note 2.1 for more information on configuration straps.

Table 2.1 MII Interface Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Transmit Data 0 (Internal PHY Mode)	TXD0	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal.
	Transmit Data 0 (External PHY Mode)	TXD0	O8 (PD)	In External PHY Mode, this pin functions as the transmit data 0 output to the external PHY.
	General Purpose I/O 4 (Internal PHY Mode Only)	GPIO4	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input.
	EEPROM Disable Configuration Strap	EEP_DISABLE	IS (PD)	This strap disables the autoloading of the EEPROM contents. The assertion of this strap does not prevent register access to the EEPROM. 0 = EEPROM is recognized if present. 1 = EEPROM is not recognized even if it is present. See Note 2.1 for more information on configuration straps.

Table 2.2 EEPROM Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	EEPROM Data In	EEDI	IS (PD)	This pin is driven by the EEDO output of the external EEPROM.
1	EEPROM Data Out	EEDO	O8 (PU)	This pin drives the EEDI input of the external EEPROM.
1	Auto-MDIX Enable Configuration Strap	AUTOMDIX_EN	IS (PU)	Determines the default Auto-MDIX setting. 0 = Auto-MDIX is disabled. 1 = Auto-MDIX is enabled. See Note 2.1 for more information on configuration straps.
1	EEPROM Chip Select	EECS	O8	This pin drives the chip select output of the external EEPROM. **Note:** The EECS output may tri-state briefly during power-up. Some EEPROM devices may be prone to false selection during this time. When an EEPROM is used, an external pull-down resistor is recommended on this signal to prevent false selection. Refer to your EEPROM manufacturer's datasheet for additional information.
1	EEPROM Clock	EECLK	O8 (PD)	This pin drives the EEPROM clock of the external EEPROM. **Note:** This pin must be pulled-up externally for proper operation.

Note 2.1 Configuration strap values are latched on Power-On Reset (POR) or External Chip Reset (nRESET). Configuration straps are identified by an underlined symbol name. Pins that function as configuration straps must be augmented with an external resistor when connected to a load.

Table 2.3 JTAG Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	JTAG Test Port Reset (Internal PHY Mode)	nTRST	IS (PU)	In Internal PHY Mode, this active-low pin functions as the JTAG test port reset input.
	Receive Data 0 (External PHY Mode)	RXD0	IS (PD)	In External PHY Mode, this pin functions as the receive data 0 input from the external PHY.
1	JTAG Test Data Out (Internal PHY Mode)	TDO	O8	In Internal PHY Mode, this pin functions as the JTAG data output.
	PHY Reset (External PHY Mode)	nPHY_RST	O8	In External PHY Mode, this active-low pin functions as the PHY reset output.
1	JTAG Test Clock (Internal PHY Mode)	TCK	IS (PU)	In Internal PHY Mode, this pin functions as the JTAG test clock. The maximum operating frequency of this clock is 25 MHz.
	Receive Data 1 (External PHY Mode)	RXD1	IS (PD)	In External PHY Mode, this pin functions as the receive data 1 input from the external PHY.
1	JTAG Test Mode Select (Internal PHY Mode)	TMS	IS (PU)	In Internal PHY Mode, this pin functions as the JTAG test mode select.
	Receive Data 2 (External PHY Mode)	RXD2	IS (PD)	In External PHY Mode, this pin functions as the receive data 2 input from the external PHY.
1	JTAG Test Data Input (Internal PHY Mode)	TDI	IS (PU)	In Internal PHY Mode, this pin functions as the JTAG data input.
	Receive Data 3 (External PHY Mode)	RXD3	IS (PD)	In External PHY Mode, this pin functions as the receive data 3 input from the external PHY.

Table 2.4 Miscellaneous Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	PHY Select	PHY_SEL	IS (PD)	Selects whether to use the internal Ethernet PHY or the external PHY connected to the MII port. 0 = Internal PHY is used. 1 = External PHY is used. **Note:** When in External PHY Mode, the internal PHY is placed into general power down after a POR.
1	System Reset	nRESET	IS (PU)	This active-low pin allows external hardware to reset the device. **Note:** This pin may be used to signal PME_CLEAR when PME Mode of operation is in effect. Refer to Chapter 5, "PME Operation," on page 37 for additional information.
1	Ethernet Full-Duplex Indicator LED	nFDX_LED	OD12 (PU)	This pin is driven low (LED on) when the Ethernet link is operating in Full-Duplex mode.
	General Purpose I/O 8	GPIO8	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. **Note:** This pin may be used to signal PME when External PHY and PME Modes of operation are in effect. Refer to Chapter 5, "PME Operation," on page 37 for additional information. **Note:** By default this pin is configured as a GPIO.
1	Ethernet Link Activity Indicator LED	nLNKA_LED	OD12 (PU)	This pin is driven low (LED on) when a valid link is detected. This pin is pulsed high (LED off) for 80 ms whenever transmit or receive activity is detected. This pin is then driven low again for a minimum of 80 ms, after which time it will repeat the process if TX or RX activity is detected. Effectively, LED2 is activated solid for a link. When transmit or receive activity is sensed, LED2 will function as an activity indicator.
	General Purpose I/O 9	GPIO9	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. **Note:** This pin may serve as the PME_MODE_SEL input when External PHY and PME Modes of operation are in effect. Refer to Chapter 5, "PME Operation," on page 37 for additional information. **Note:** By default this pin is configured as a GPIO.

Table 2.4 Miscellaneous Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
	Ethernet Speed Indicator LED	nSPD_LED	OD12 (PU)	This pin is driven low (LED on) when the Ethernet operating speed is 100 Mbs, or during auto-negotiation. This pin is driven high during 10 Mbs operation or during line isolation.
1	General Purpose I/O 10	GPIO10	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. **Note:** This pin may serve as a wakeup pin whose detection mode is selectable when External PHY and PME Modes of operation are in effect. Refer to Chapter 5, "PME Operation," on page 37 for additional information. **Note:** By default this pin is configured as a GPIO.
1	Core Regulator Enable	CORE_REG_EN	AI	This pin enables/disables the internal core logic voltage regulator. When tied low to VSS, the internal core regulator is disabled and +1.2 V must be supplied to the device by an external source. When tied high to +3.3 V, the internal core regulator is enabled. Refer to Chapter 3, "Power Connections," on page 24 and the device reference schematics for connection information.
1	Test 1	TEST1	-	This pin must always be connected to VSS for proper operation.
1	Test 2	TEST2	-	This pin must always be connected to +3.3 V for proper operation.
1	Crystal Input	XI	ICLK	External 25 MHz crystal input. **Note:** This pin can also be driven by a single-ended clock oscillator. When this method is used, XO should be left unconnected
1	Crystal Output	XO	OCLK	External 25 MHz crystal output.

Table 2.5 USB Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	HSIC Data	HSIC_DATA	HSIC	Bi-directional Double Data Rate (DDR) data signal that is synchronous to the HSIC_STROBE signal as defined in the *High-Speed Inter-Chip USB Specification, Version 1.0*.
1	HSIC Strobe	HSIC_STROBE	HSIC	Bi-directional data strobe signal as defined in the *High-Speed Inter-Chip USB Specification, Version 1.0*.
1	HSIC Slew Tune	SLEW_TUNE	IS (PD)	Applies a slew rate boost to the HSIC_DATA and HSIC_STROBE pins when driven high.
1	External USB Bias Resistor	USBRBIAS	AI	Used for setting HS transmit current level and on-chip termination impedance. Connect to an external 12.0 kΩ 1.0% resistor to ground.

Table 2.6 Ethernet PHY Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Ethernet TX Data Out Negative	TXN	AIO	The transmit data outputs may be swapped internally with receive data inputs when Auto-MDIX is enabled.
1	Ethernet TX Data Out Positive	TXP	AIO	The transmit data outputs may be swapped internally with receive data inputs when Auto-MDIX is enabled.
1	Ethernet RX Data In Negative	RXN	AIO	The receive data inputs may be swapped internally with transmit data outputs when Auto-MDIX is enabled.
1	Ethernet RX Data In Positive	RXP	AIO	The receive data inputs may be swapped internally with transmit data outputs when Auto-MDIX is enabled.
1	PHY Interrupt (Internal PHY Mode)	nPHY_INT	O8	In Internal PHY Mode, this pin can be configured to output the internal PHY interrupt signal. **Note:** The internal PHY interrupt signal is active-high.
	PHY Interrupt (External PHY Mode)	nPHY_INT	IS (PU)	In External PHY Mode, the active-low signal on this pin is input from the external PHY and indicates a PHY interrupt has occurred.
1	External PHY Bias Resistor	EXRES	AI	Used for the internal bias circuits. Connect to an external 12.0 kΩ 1.0% resistor to ground.

Table 2.7 Power Pins and Ground Pad

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
5	+3.3 V I/O Power	VDD33IO	P	Refer to Chapter 3, "Power Connections," on page 24 and the device reference schematics for connection information.
3	+3.3 V Analog Power	VDD33A	P	Refer to Chapter 3, "Power Connections," on page 24 and the device reference schematics for connection information.
2	+1.2 V Digital Core Power	VDD12CORE	P	Refer to Chapter 3, "Power Connections," on page 24 and the device reference schematics for connection information.
1	+1.2 V USB PLL Power	VDD12USBPLL	P	This pin must be connected to VDD12CORE for proper operation. Refer to Chapter 3, "Power Connections," on page 24 and the device reference schematics for additional connection information.
1	+1.2 V HSIC Power	VDD12A	P	This pin must be connected to VDD12CORE for proper operation. Refer to Chapter 3, "Power Connections," on page 24 and the device reference schematics for connection information.
1	+1.2 V Ethernet PLL Power	VDD12PLL	P	This pin must be connected to VDD12CORE for proper operation. Refer to Chapter 3, "Power Connections," on page 24 and the device reference schematics for additional connection information.
Exposed pad on package bottom (Figure 2.1)	Ground	VSS	P	Common Ground

2.1 Pin Assignments

Table 2.8 56-QFN Package Pin Assignments

PIN NUM	PIN NAME	PIN NUM	PIN NAME	PIN NUM	PIN NAME	PIN NUM	PIN NAME
1	nPHY_INT	15	VDD33A	29	EECLK	43	TXEN
2	TXN	16	USBRBIAS	30	EECS	44	RXER
3	TXP	17	VDD12USBPLL	31	EEDO/ AUTOMDIX_EN	45	CRS/GPIO3
4	VDD33A	18	XI	32	EEDI	46	COL/GPIO0 Note 2.2
5	RXN	19	XO	33	TEST1	47	TXCLK
6	RXP	20	SLEW_TUNE	34	PHY_SEL	48	VDD33IO
7	EXRES	21	VDD12CORE	35	VDD33IO	49	CORE_REG_EN
8	VDD33A	22	MDC/GPIO2	36	nTRST/RXD0	50	VDD12CORE
9	VDD12PLL	23	MDIO/GPIO1 Note 2.2	37	TDO/nPHY_RST	51	VDD33IO
10	HSIC_DATA	24	nRESET Note 2.2	38	TCK/RXD1	52	VDD33IO
11	HSIC_STROBE	25	VDD33IO	39	TMS/RXD2	53	TXD3/GPIO7/ 50DRIVER_EN
12	VDD12A	26	nFDX_LED/ GPIO8	40	TDI/RXD3	54	TXD2/GPIO6/ PORT_SWAP
13	TEST2	27	nLNKA_LED/ GPIO9 Note 2.2	41	RXCLK	55	TXD1/GPIO5/ RMT_WKP
14	TXER	28	nSPD_LED/ GPIO10 Note 2.2	42	RXDV	56	TXD0/GPIO4/ EEP_DISABLE
EXPOSED PAD MUST BE CONNECTED TO VSS							

Note 2.2 This pin provides additional PME-related functionality. Refer to the respective pin descriptions and Section Chapter 5, "PME Operation," on page 37 for additional information.

2.2 Buffer Types

Table 2.9 Buffer Types

BUFFER TYPE	DESCRIPTION
IS	Schmitt-triggered input
O8	Output with 8 mA sink and 8 mA source
OD8	Open-drain output with 8 mA sink
O12	Output with 12 mA sink and 12 mA source
OD12	Open-drain output with 12 mA sink
HSIC	*High-Speed Inter-Chip (HSIC) USB Specification, Version 1.0* compliant input/output
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

Chapter 3 Power Connections

The LAN9730/LAN9730i can be operated with the internal core regulator enabled or disabled. Figure 3.1 illustrates the power connections for operating the device with the internal regulator enabled. Figure 3.2 illustrates the power connections for operating the device with the internal regulator disabled. In this mode, +1.2 V must be supplied to the device by an external source.

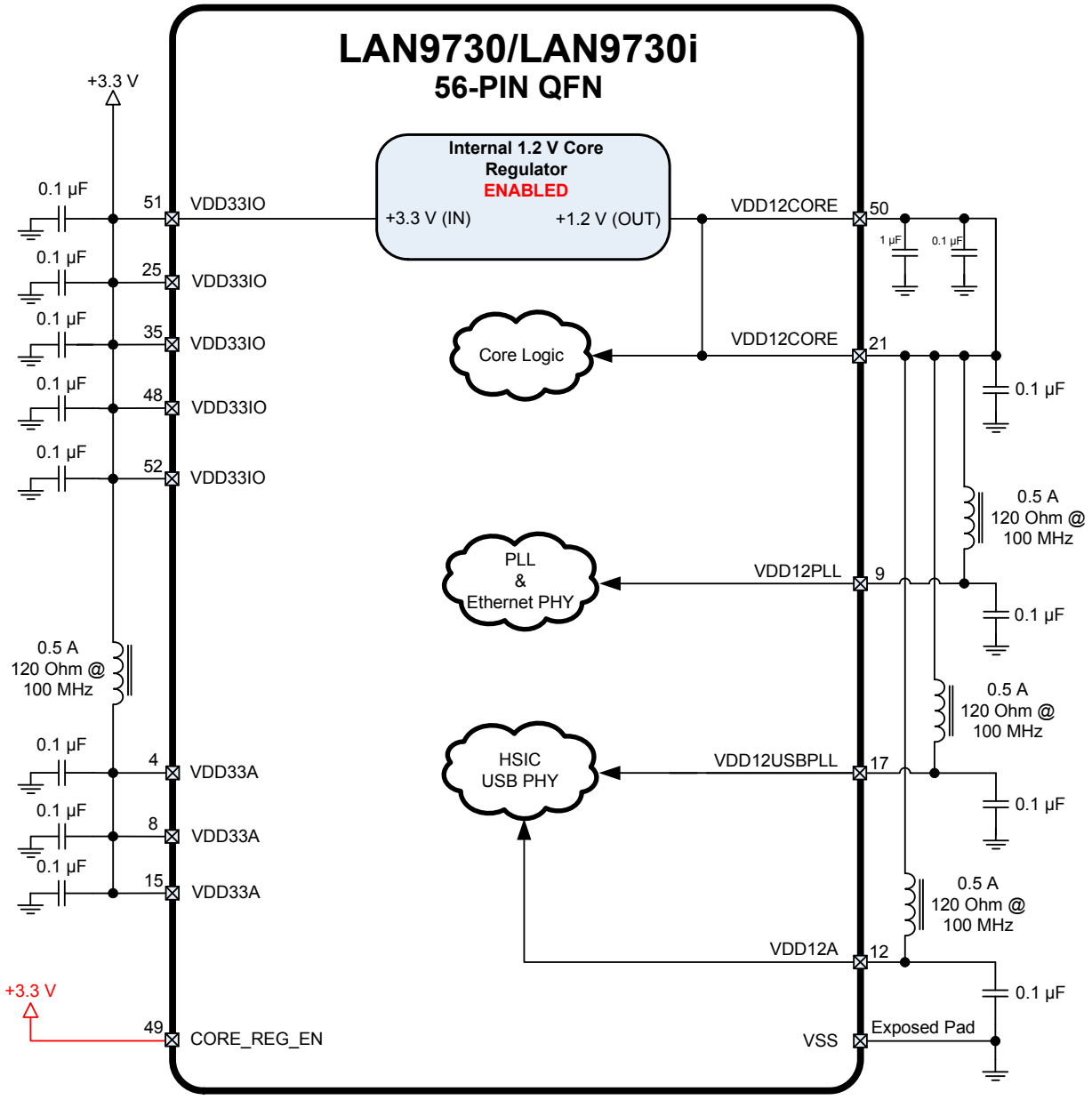


Figure 3.1 Power Connections - Internal Regulator Enabled

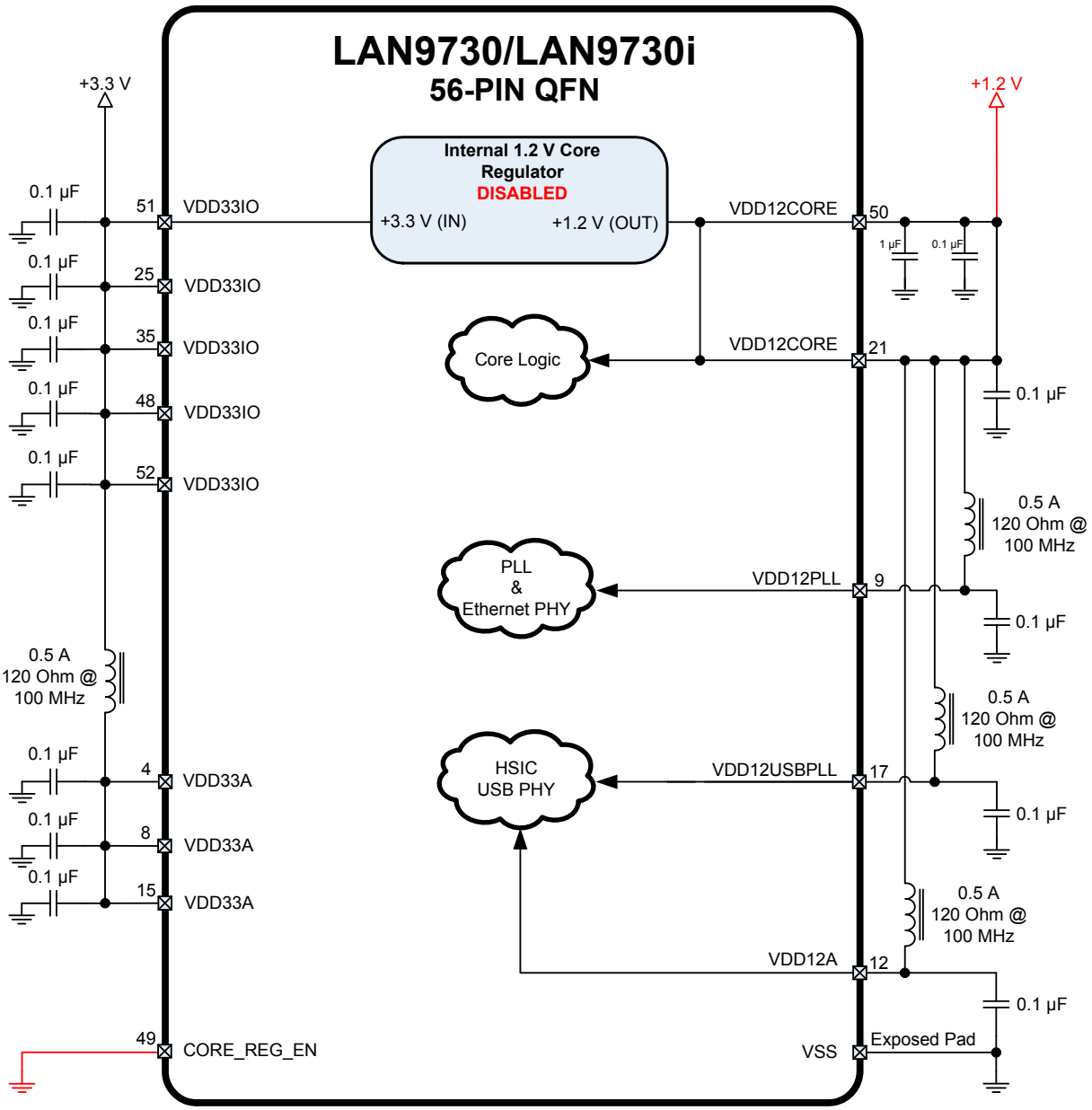


Figure 3.2 Power Connections - Internal Regulator Disabled

Chapter 4 EEPROM Controller

The device may use an external EEPROM to store the default values for the USB descriptors and the MAC address. The EEPROM controller supports most 256/512 byte “93C46” type EEPROMs.

Note: A 3-wire style 2k/4k EEPROM that is organized for 256/512 x 8-bit operation must be used.

The MAC address is used as the default Ethernet MAC address and is loaded into the MAC’s ADDRH and ADDRL registers. If a properly configured EEPROM is not detected, it is the responsibility of the Host LAN Driver to set the IEEE addresses.

After a system-level reset occurs, the device will load the default values from a properly configured EEPROM. The device will not accept USB transactions from the Host until this process is completed.

The EEPROM controller also allows the Host system to read, write and erase the contents of the serial EEPROM.

4.1 EEPROM Format

Table 4.1 illustrates the format in which data is stored inside of the EEPROM.

Note the EEPROM offsets are given in units of 16-bit word offsets. A length field with a value of zero indicates that the field does not exist in the EEPROM. The device will use the field’s HW default value in this case.

Note: For the device descriptor, the only valid values for the length are 0 and 18.

Note: For the configuration and interface descriptor, the only valid values for the length are 0 and 18.

Note: The EEPROM programmer must ensure that if a string descriptor does not exist in the EEPROM, the referencing descriptor must contain 00h for the respective string index field.

Note: If all string descriptor lengths are zero, then a Language ID will not be supported.

Table 4.1 EEPROM Format

EEPROM ADDRESS	EEPROM CONTENTS
00h	0xA5
01h	MAC Address [7:0]
02h	MAC Address [15:8]
03h	MAC Address [23:16]
04h	MAC Address [31:24]
05h	MAC Address [39:32]
06h	MAC Address [47:40]
07h	Full-Speed Polling Interval for Interrupt Endpoint
08h	Hi-Speed Polling Interval for Interrupt Endpoint
09h	Configuration Flags

Table 4.1 EEPROM Format (continued)

0Ah	Language ID Descriptor [7:0]
0Bh	Language ID Descriptor [15:8]
0Ch	Manufacturer ID String Descriptor Length (bytes)
0Dh	Manufacturer ID String Descriptor EEPROM Word Offset
0Eh	Product Name String Descriptor Length (bytes)
0Fh	Product Name String Descriptor EEPROM Word Offset
10h	Serial Number String Descriptor Length (bytes)
11h	Serial Number String Descriptor EEPROM Word Offset
12h	Configuration String Descriptor Length (bytes)
13h	Configuration String Descriptor Word Offset
14h	Interface String Descriptor Length (bytes)
15h	Interface String Descriptor Word Offset
16h	Hi-Speed Device Descriptor Length (bytes)
17h	Hi-Speed Device Descriptor Word Offset
18h	Hi-Speed Configuration and Interface Descriptor Length (bytes)
19h	Hi-Speed Configuration and Interface Descriptor Word Offset
1Ah	Full-Speed Device Descriptor Length (bytes)
1Bh	Full-Speed Device Descriptor Word Offset
1Ch	Full-Speed Configuration and Interface Descriptor Length (bytes)
1Dh	Full-Speed Configuration and Interface Descriptor Word Offset
1Eh	GPIO7:0 Wakeup Enables Bit x = 0 -> GPIOx pin disabled for wakeup use. Bit x = 1 -> GPIOx pin enabled for wakeup use.
1Fh	GPIO10:8 Wakeup Enables Bit x = 0 -> GPIO(x+8) pin disabled for wakeup use. Bit x = 1 -> GPIO(x+8) pin enabled for wakeup use.
20h	GPIO PME Flags

Note: The descriptor type for the device descriptors specified in the EEPROM is a don't care and always overwritten by HW to 0x1.
The descriptor size for the device descriptors specified in the EEPROM is a don't care and always overwritten by HW to 0x12.
The descriptor type for the configuration descriptors specified in the EEPROM is a don't care and always overwritten by HW to 0x2.

Note: Descriptors specified in EEPROM having bcdUSB, bMaxPacketSize0, and bNumConfigurations fields defined with values other than 0200h, 40h and 1, respectively, will result in unwanted behavior and untoward results.

Note: EEPROM byte addresses past 20h can be used to store data for any purpose.

Table 4.2 describes the configuration flags. The configuration flags override the affects of the RMT_WKP strap. If a configuration descriptor exists in the EEPROM it will override both the configuration flags and associated straps.

Table 4.2 Configuration Flags

<table>
<tr><th>BITS</th><th>DESCRIPTION</th></tr>
<tr><td>7:4</td><td>RESERVED</td></tr>
<tr><td>3</td><td>RESERVED</td></tr>
<tr><td>2</td><td>Remote Wakeup Support
0 = The device does not support remote wakeup.
1 = The device supports remote wakeup.</td></tr>
<tr><td>1</td><td>LED Select

This bit determines the functionality of external LED pins.

<table>
<tr><th>BIT VALUE</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td rowspan="3">0</td><td>nSPD_LED</td><td>Speed Indicator</td></tr>
<tr><td>nLNKA_LED</td><td>Link and Activity Indicator</td></tr>
<tr><td>nFDX_LED</td><td>Full Duplex Link Indicator</td></tr>
<tr><td rowspan="3">1</td><td>nSPD_LED</td><td>Speed Indicator</td></tr>
<tr><td>nLNKA_LED</td><td>Link Indicator</td></tr>
<tr><td>nFDX_LED</td><td>Activity Indicator</td></tr>
</table>
</td></tr>
<tr><td>0</td><td>Power Method
0 = The device is bus powered.
1 = The device is self powered.</td></tr>
</table>

Table 4.3 describes the GPIO PME flags.

Table 4.3 GPIO PME Flags

BITS	DESCRIPTION
7	**GPIO PME Enable** Setting this bit enables the assertion of the GPIO0 or GPIO8 pin, as a result of a Wakeup (GPIO) pin, Magic Packet or PHY Link Up. The host processor may use the GPIO0/GPIO8 pin to asynchronously wake up, in a manner analogous to a PCI PME pin. GPIO0 signals the event when operating in Internal PHY Mode, while GPIO8 signals the event when operating in External PHY Mode. Internal or External PHY Mode of operation is dictated by the PHY_SEL pin. 0 = The device does not support GPIO PME signaling. 1 = The device supports GPIO PME signaling. **Note:** When this bit is 0, the remaining GPIO PME parameters in this flag byte are ignored.
6	**GPIO PME Configuration** This bit selects whether the GPIO PME is signaled on the GPIO pin as a level or a pulse. If pulse is selected, the duration of the pulse is determined by the setting of the GPIO PME Length bit of this flag byte. The level of the signal or the polarity of the pulse is determined by the GPIO PME Polarity bit of this flag byte. 0 = GPIO PME is signaled via a level. 1 = GPIO PME is signaled via a pulse. **Note:** If GPIO PME Enable is 0, this bit is ignored.
5	**GPIO PME Length** When the GPIO PME Configuration bit of this flag byte indicates that the GPIO PME is signaled by a pulse on the GPIO pin, this bit determines the duration of the pulse. 0 = GPIO PME pulse length is 1.5 ms. 1 = GPIO PME pulse length is 150 ms. **Note:** If GPIO PME Enable is 0, this bit is ignored.
4	**GPIO PME Polarity** Specifies the level of the signal or the polarity of the pulse used for GPIO PME signaling. 0 = GPIO PME signaling polarity is low. 1 = GPIO PME signaling polarity is high. **Note:** If GPIO PME Enable is 0, this bit is ignored.
3	**GPIO PME Buffer Type** This bit selects the output buffer type for GPIO0/GPIO8. 0 = Open drain driver / open source 1 = Push-Pull driver **Note:** Buffer Type = 0, Polarity = 0 implies open drain Buffer Type = 0, Polarity = 1 implies open source **Note:** If GPIO PME Enable is 0, this bit is ignored.
2	**GPIO PME WOL Select** Three types of wakeup events are supported; Magic Packet, PHY Link Up and Wakeup Pin(s) assertion. Wakeup Pin(s) are selected via the GPIO Wakeup Enables specified in bytes 1Eh and 1Fh of the EEPROM. This bit selects whether Magic Packet or Link Up wakeup events are supported. 0 = Magic Packet wakeup supported. 1 = PHY Link Up wakeup supported (not supported in External PHY Mode). **Note:** If GPIO PME Enable is 0, this bit is ignored.

Table 4.3 GPIO PME Flags (continued)

BITS	DESCRIPTION
1	**GPIO10 Detection Select** This bit selects the detection mode for GPIO10 when operating in PME Mode. In PME Mode, GPIO10 is usable in both Internal and External PHY Mode as a wakeup pin. This parameter defines whether the wakeup should occur on an active high or active low signal. 0 = Active-low detection for GPIO10 1 = Active-high detection for GPIO10 **Note:** If GPIO PME Enable is 0, this bit is ignored.
0	**RESERVED**

4.2 EEPROM Defaults

The signature value of 0xA5 is stored at address 0. A different signature value indicates to the EEPROM controller that no EEPROM or an un-programmed EEPROM is attached to the device. In this case, the hardware default values are used, as shown in Table 4.4.

Table 4.4 EEPROM Defaults

FIELD	DEFAULT VALUE
MAC Address	FFFFFFFFFFFFh
Full-Speed Polling Interval (ms)	01h
Hi-Speed Polling Interval (ms)	04h
Configuration Flags	04h
Maximum Power (mA)	FAh
Vendor ID	0424h
Product ID	9730h

Note: The Configuration Flags are affected by the RMT_WKP strap.

4.3 EEPROM Auto-Load

Certain system level resets (USB reset, POR, nRESET and SRST) cause the EEPROM contents to be loaded into the device. After a reset, the EEPROM controller attempts to read the first byte of data from the EEPROM. If the value 0xA5 is read from the first address, then the EEPROM controller will assume that an external Serial EEPROM is present.

Note: The USB reset only loads the MAC address.

4.4 Example of EEPROM Format Interpretation

Table 4.5 and Table 4.6 provide an example of how the contents of a EEPROM are formatted. Table 4.5 is a dump of the EEPROM memory (256-byte EEPROM), while Table 4.6 illustrates, byte by byte, how the EEPROM is formatted.

Table 4.5 Dump of EEPROM Memory

OFFSET BYTE	VALUE
0000h	A5 12 34 56 78 9A BC 01
0008h	04 04 09 04 0A 11 12 16
0010h	10 1F 00 00 00 00 12 27
0018h	12 30 12 39 12 42 00 04
0020h	8A 00 0A 03 53 00 4D 00
0028h	53 00 43 00 12 03 4C 00
0030h	41 00 4E 00 39 00 37 00
0038h	33 00 30 00 10 03 30 00
0040h	30 00 30 00 35 00 31 00
0048h	32 00 33 00 12 01 00 02
0050h	FF 00 FF 40 24 04 30 97
0058h	00 01 01 02 03 01 09 02
0060h	27 00 01 01 00 A0 FA 09
0068h	04 00 00 03 FF 00 FF 00
0070h	12 01 00 02 FF 00 FF 40
0078h	24 04 30 97 00 01 01 02
0080h	03 01 09 02 27 00 01 01
0088h	00 A0 FA 09 04 00 00 03
0090h - 00FFh	FF 00 FF 00 .....

Table 4.6 EEPROM Example - 256 Byte EEPROM

EEPROM ADDRESS	EEPROM CONTENTS (HEX)	DESCRIPTION
00h	A5	EEPROM programmed indicator
01h - 06h	12 34 56 78 9A BC	MAC Address 12 34 56 78 9A BC
07h	01	Full-Speed polling interval for Interrupt Endpoint (1ms)
08h	04	Hi-Speed polling interval for Interrupt Endpoint (4ms)
09h	04	Configuration Flags - The device is bus powered and supports remote wakeup; nSPD_LED = Speed Indicator, nLNKA_LED = Link and Activity Indicator, nFDX_LED = Full Duplex Link Indicator.
0Ah - 0Bh	09 04	Language ID Descriptor 0409h, English
0Ch	0A	Manufacturer ID String Descriptor Length (10 bytes)
0Dh	11	Manufacturer ID String Descriptor EEPROM Word Offset (11h) Corresponds to EEPROM Byte Offset 22h
0Eh	10	Product Name String Descriptor Length (16 bytes)
0Fh	16	Product Name String Descriptor EEPROM Word Offset (16h); corresponds to EEPROM Byte Offset 2Ch
10h	10	Serial Number String Descriptor Length (16 bytes)
11h	1E	Serial Number String Descriptor EEPROM Word Offset (1Eh); corresponds to EEPROM Byte Offset 3Ch
12h	00	Configuration String Descriptor Length (0 bytes - NA)
13h	00	Configuration String Descriptor Word Offset (don't care)
14h	00	Interface String Descriptor Length (0 bytes - NA)
15h	00	Interface String Descriptor Word Offset (don't care)
16h	12	Hi-Speed Device Descriptor Length (18 bytes)
17h	26	Hi-Speed Device Descriptor Word Offset (26h); corresponds to EEPROM Byte Offset 4Ch
18h	12	Hi-Speed Configuration and Interface Descriptor Length (18 bytes)
19h	2F	Hi-Speed Configuration and Interface Descriptor Word Offset (2Fh); corresponds to EEPROM Byte Offset 5Eh
1Ah	12	Full-Speed Device Descriptor Length (18 bytes)
1Bh	38	Full-Speed Device Descriptor Word Offset (38h); corresponds to EEPROM Byte Offset 70h
1Ch	12	Full-Speed Configuration and Interface Descriptor Length (18 bytes)
1Dh	41	Full-Speed Configuration and Interface Descriptor Word Offset (41h); corresponds to EEPROM Byte Offset 82h
1Eh	00	GPIO7:0 Wake Enables - GPIO7:0 not used for wakeup signaling

Table 4.6 EEPROM Example - 256 Byte EEPROM (continued)

EEPROM ADDRESS	EEPROM CONTENTS (HEX)	DESCRIPTION
1Fh	04	GPIO10:8 Wake Enables - GPIO10 used for wakeup signaling
20h	8A	GPIO PME Flags - PME Signaling Enabled via Low Level, Push-Pull Driver, GPIO10 Active High Detection
21h	00	PAD BYTE - Used to align following descriptor on Word Boundary
22h	0A	Size of Manufacturer ID String Descriptor (10 bytes)
23h	03	Descriptor Type (String Descriptor - 03h)
24h - 2Bh	53 00 4D 00 53 00 43 00	Manufacturer ID String (“SMSC” in UNICODE)
2Ch	10	Size of Product Name String Descriptor (16 bytes)
2Dh	03	Descriptor Type (String Descriptor - 03h)
2Eh - 3Bh	4C 00 41 00 4E 00 39 00 37 00 33 00 30 00	Product Name String (“LAN9730” in UNICODE)
3Ch	10	Size of Serial Number String Descriptor (16 bytes)
3Dh	03	Descriptor Type (String Descriptor - 03h)
3Eh - 4Bh	30 00 30 00 30 00 35 00 31 00 32 00 33 00	Serial Number String (“0005123” in UNICODE)
4Ch	12	Size of Hi-Speed Device Descriptor in bytes (18 bytes)
4Dh	01	Descriptor Type (Device Descriptor - 01h)
4Eh - 4Fh	00 02	USB Specification Number that the device complies with (0200h)
50h	FF	Class Code
51h	00	Subclass Code
52h	FF	Protocol Code
53h	40	Maximum Packet Size for Endpoint 0
54h - 55h	24 04	Vendor ID (0424h)
56h - 57h	30 97	Product ID (9730h)
58h - 59h	00 01	Device Release Number (0100h)
5Ah	01	Index of Manufacturer String Descriptor
5Bh	02	Index of Product String Descriptor
5Ch	03	Index of Serial Number String Descriptor
5Dh	01	Number of possible configurations
5Eh	09	Size of Hi-Speed Configuration Descriptor in bytes (9 bytes)
5Fh	02	Descriptor Type (Configuration Descriptor - 02h)

Table 4.6 EEPROM Example - 256 Byte EEPROM (continued)

EEPROM ADDRESS	EEPROM CONTENTS (HEX)	DESCRIPTION
60h - 61h	27 00	Total length in bytes of data returned (0027h = 39 bytes)
62h	01	Number of interfaces
63h	01	Value to use as an argument to select this configuration
64h	00	Index of String Descriptor describing this configuration
65h	A0	Bus powered and remote wakeup enabled
66h	FA	Maximum power consumption is 500 mA
67h	09	Size of Hi-Speed Interface Descriptor in bytes (9 bytes)
68h	04	Descriptor Type (Interface Descriptor - 04h)
69h	00	Number identifying this interface
6Ah	00	Value used to select alternative setting
6Bh	03	Number of Endpoints used for this interface (Less Endpoint 0)
6Ch	FF	Class Code
6Dh	00	Subclass Code
6Eh	FF	Protocol Code
6Fh	00	Index of String Descriptor Describing this interface
70h	12	Size of Full-Speed Device Descriptor in bytes (18 bytes)
71h	01	Descriptor Type (Device Descriptor - 01h)
72h - 73h	00 02	USB Specification Number that the device complies with (0200h)
74h	FF	Class Code
75h	00	Subclass Code
76h	FF	Protocol Code
77h	40	Maximum Packet Size for Endpoint 0
78h - 79h	24 04	Vendor ID (0424h)
7Ah - 7Bh	30 97	Product ID (9730h)
7Ch - 7Dh	00 01	Device Release Number (0100h)
7Eh	01	Index of Manufacturer String Descriptor
7Fh	02	Index of Product String Descriptor
80h	03	Index of Serial Number String Descriptor
81h	01	Number of Possible Configurations

Table 4.6 EEPROM Example - 256 Byte EEPROM (continued)

EEPROM ADDRESS	EEPROM CONTENTS (HEX)	DESCRIPTION
82h	09	Size of Full-Speed Configuration Descriptor in bytes (9 bytes)
83h	02	Descriptor Type (Configuration Descriptor - 02h)
84h - 85h	27 00	Total length in bytes of data returned (0027h = 39 bytes)
86h	01	Number of interfaces
87h	01	Value to use as an argument to select this configuration
88h	00	Index of String Descriptor describing this configuration
89h	A0	Bus powered and remote wakeup enabled
8Ah	FA	Maximum power consumption is 500 mA
8Bh	09	Size of Full-Speed Interface Descriptor in bytes (9 bytes)
8Ch	04	Descriptor Type (Interface Descriptor - 04h)
8Dh	00	Number identifying this interface
8Eh	00	Value used to select alternative setting
8Fh	03	Number of Endpoints used for this interface (Less Endpoint 0)
90h	FF	Class Code
91h	00	Subclass Code
92h	FF	Protocol Code
93h	00	Index of String Descriptor describing this interface
94h - FFh	-	Data storage for use by Host as desired

4.5 Customized Operation Without EEPROM

The device provides the capability to customize operation without the use of an EEPROM. Descriptor information and initialization quantities normally fetched from EEPROM and used to initialize descriptors and elements of the System Control and Status registers may be specified via an alternate mechanism. This alternate mechanism involves the use of the Descriptor RAM in conjunction with the Attribute registers and select elements of the System Control and Status registers. The software device driver orchestrates the process by performing the following actions in the order indicated:

- Initialization of System Control and Status register elements in lieu of EEPROM load
- Attribute register initialization
- Descriptor RAM initialization
- Enable Descriptor RAM and Flag Attribute registers as source
- Inhibit reset of Select System Control and Status register elements

Chapter 5 PME Operation

The device provides a mechanism for waking up a host system via PME Mode of operation. PME signaling is only available while the device is operating in the self-powered mode. Figure 5.1 illustrates a typical application.

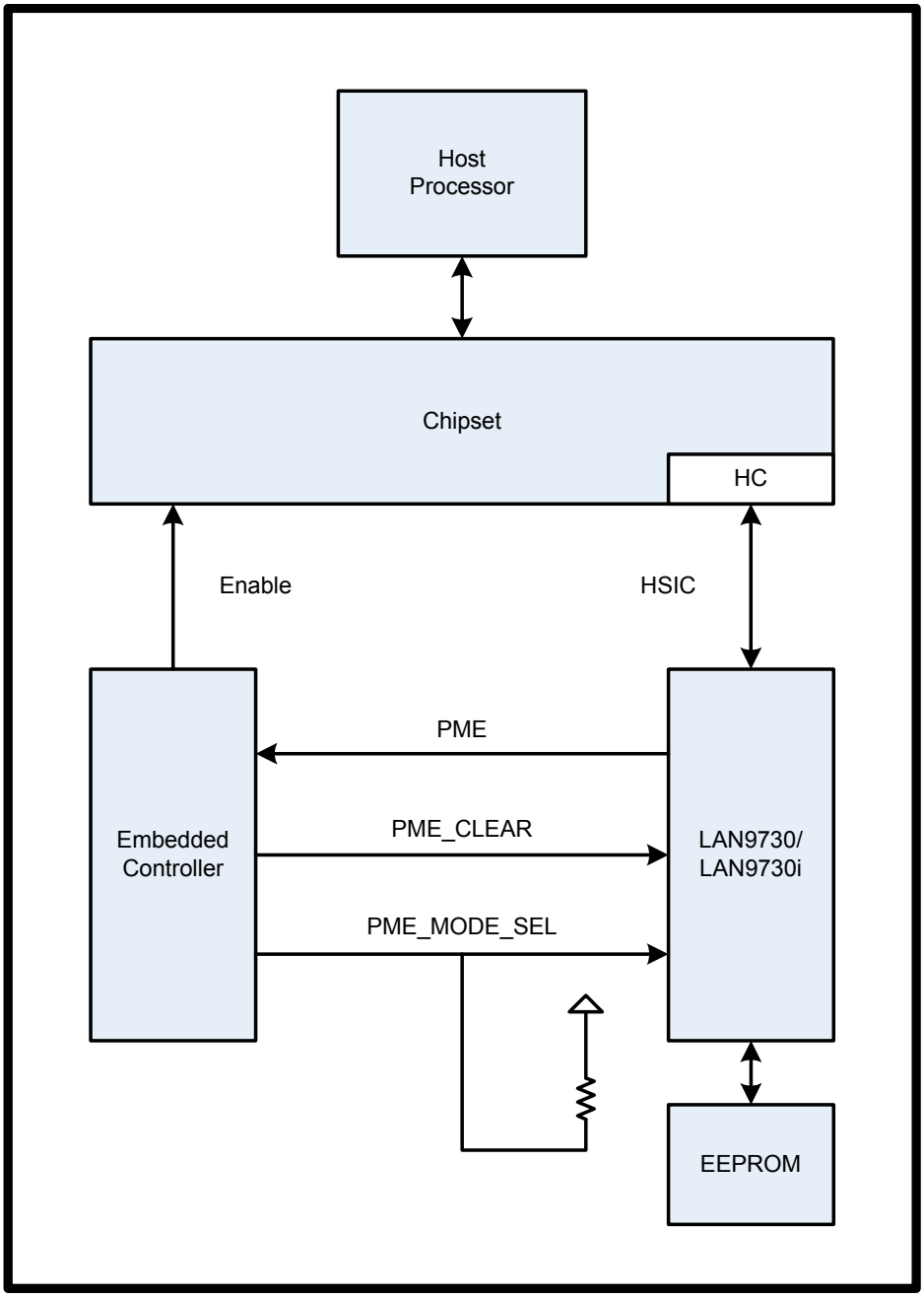


Figure 5.1 Typical Application

The Host processor is connected to a Chipset containing the Host USB Controller (HC). The USB Host Controller interfaces to the device via the HSIC USB signals. An Embedded Controller (EC) signals the Chipset and the Host processor to power up via an Enable signal. The EC interfaces to the device via three signals. The PME signal is an input to the EC from the device that indicates the occurrence of a wakeup event. The PME_CLEAR (nRESET) signal is used to clear the PME. The PME_MODE_SEL signal is sampled by the device when PME_CLEAR (nRESET) is asserted and is used by the device to determine whether it should remain in PME Mode or resume normal operation.

GPIO pins are used for PME handling. The pins used depend on the value of the PHY_SEL pin, which determines PHY Mode of operation. In Internal PHY Mode of operation, GPIO0 is reserved for use as an output to signal the PME. GPIO1 is reserved for use as the PME_MODE_SEL input. GPIO8 and GPIO9 are reserved for analogous use, respectively, in External PHY Mode of operation.

The application scenario in Figure 5.1 assumes that the Host processor and the Chipset are powered off, the EC is operational, and the device is in PME Mode, waiting for a wake event to occur. A wake event will result in the device signaling a PME event to the EC, which will then wake up the Host processor and Chipset via the Enable signal. The EC sets PME_MODE_SEL to determine whether the device is to begin normal operation or continue in PME Mode, and asserts PME_CLEAR (nRESET) to clear the PME.

The following wake events are supported:

- Wakeup Pin(s)

  The GPIO pins not reserved for PME handling have the capability to wake up the device when operating in PME Mode. In order for a GPIO to generate a wake event, its enable bit must be set in the GPIO10:8 Wakeup Enables or GPIO7:0 Wakeup Enables bytes of the EEPROM, as appropriate. During PME Mode of operation, the GPIOs used for signaling (GPIOs 0 and 1 or GPIOs 8 and 9) are not affected by the values set in the corresponding bits of GPIO10:8 Wakeup Enables or GPIO7:0 Wakeup Enables.

  GPIO10 is available as a wakeup pin in External PHY Mode, while GPIOs 2-10 are available in Internal PHY Mode. The GPIO10 Detection Select bit in the GPIO PME Flags byte of the EEPROM sets the detection mode for GPIO10 in both External and Internal PHY Mode (if set in GPIO10:8 Wakeup Enables), while GPIOs 2-9 are active low (by default) when operating in Internal PHY Mode.

- Magic Packet

  Reception of a Magic Packet when in PME Mode will result in a PME being asserted.

- PHY Link Up

  Detection of a PHY link partner when in PME Mode will result in a PME being asserted.

In order to facilitate PME Mode of operation, the GPIO PME Enable bit in the GPIO PME Flags field, must be set and all remaining GPIO PME Flags field bits must be appropriately configured for pulse or level signaling, buffer type and GPIO PME WOL selection. The PME event is signaled on GPIO0 (External PHY Mode) or GPIO8, depending on the PHY Mode of operation.

The PME_MODE_SEL pin (GPIO1 in Internal Mode of operation, GPIO9 in External Mode of operation) must be driven to the value that determines whether or not the device remains in PME Mode of operation (1) or resumes normal operation (0) when the PME is recognized and cleared by the EC via PME_CLEAR (nRESET) assertion.

Note: When in PME Mode, nRESET or POR will always cause the contents of the EEPROM to be reloaded.

Note: GPIO10 may be used in PME and External PHY Mode to connect to an external PHY's Link LED, in order to generate a PHY Link Up wake event.

Figure 5.2 flowcharts PME operation while in Internal PHY Mode. The following conditions hold:

EEPROM Configuration:

- GPIO PME Enable = 1 (enabled)
- GPIO PME Configuration = 0 (PME signaled via level on GPIO pin)
- GPIO PME Length = 0 (NA)
- GPIO PME Polarity = 1 (high level signals event)
- GPIO PME Buffer Type = 1 (push-pull)
- GPIO PME WOL Select = 0 (Magic Packet wakeup)
- GPIO10 Detection Select = 0 (Active-low detection)
- Power Method = 1 (self powered)
- MAC address for Magic Packet

PME signaling configuration (as determined by PHY Mode):

- GPIO0 signals PME
- GPIO1 is PME_MODE_SEL

Note: A POR occurring when PME_MODE_SEL = 1 and an EEPROM present with the GPIO PME Enable set results in the device entering PME Mode.

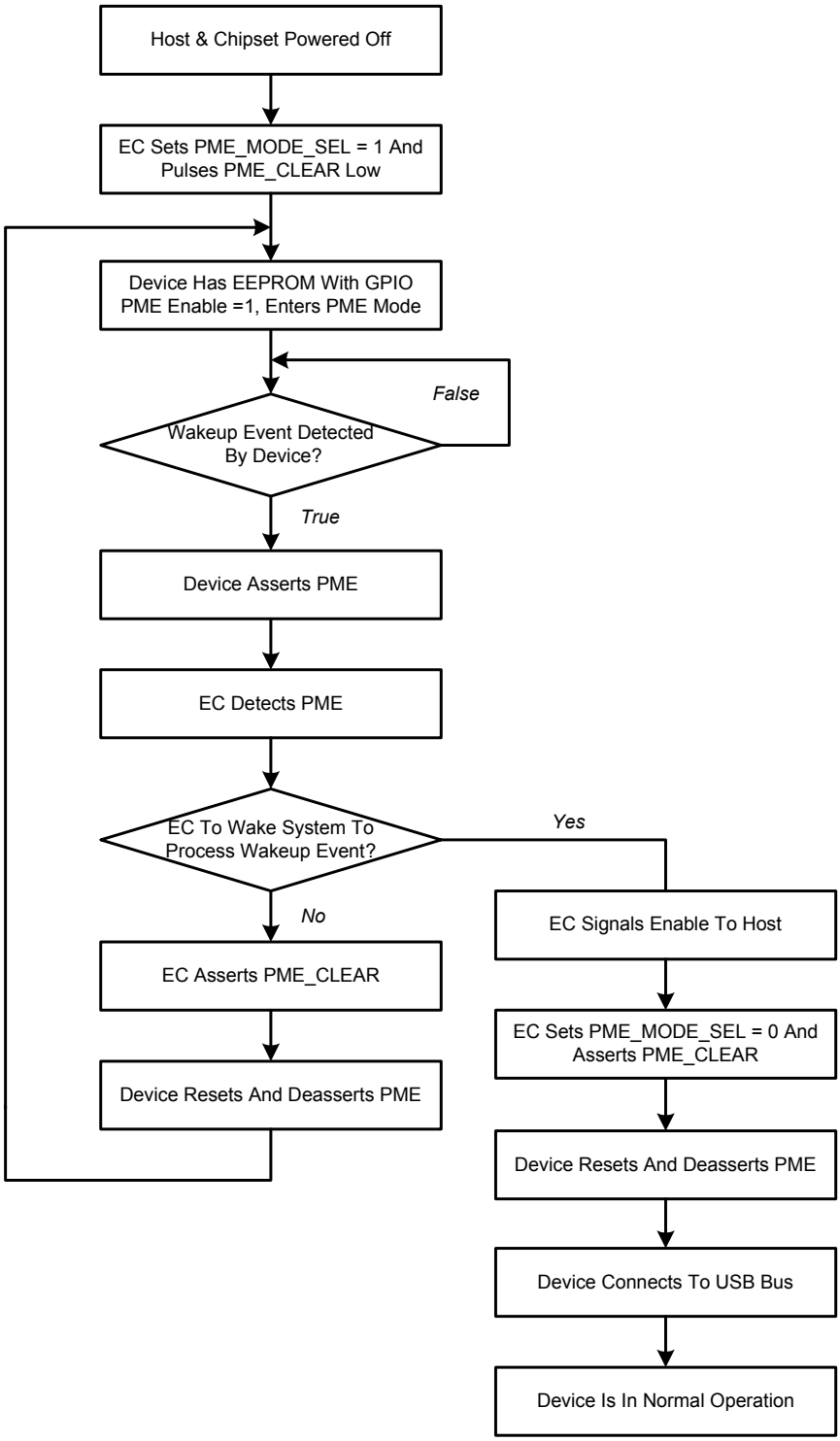


Figure 5.2 PME Operation

Chapter 6 Operational Characteristics

6.1 Absolute Maximum Ratings*

+3.3 V Supply Voltage (VDD33IO, VDD33A) (Note 6.1) . . . . . 0 V to +3.6 V

+1.2 V Supply Voltage (VDD12CORE, VDD12PLL, VDD12USBPLL, VDD12A) (Note 6.1). . . . 0 V to +1.5 V

Positive voltage on input signal pins, with respect to ground (Note 6.2) . . . . . VDD33IO + 2.0 V

Negative voltage on input signal pins, with respect to ground (Note 6.3). . . . . -0.5 V

Positive voltage on XI, with respect to ground. . . . . VDD33IO + 0.3 V

Positive voltage on XO, with respect to ground. . . . . +2.5 V

Storage Temperature . . . . . -55°C to +150°C

Lead Temperature Range. . . . . Refer to JEDEC Spec. J-STD-020

HBM ESD Performance . . . . . JEDEC Class 3A

Note 6.1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested to use a clamp circuit.

Note 6.2 This rating does not apply to the following pins: XI, XO, EXRES, USBRBIAS, HSIC_STROBE, HSIC_DATA.

Note 6.3 This rating does not apply to the following pins: EXRES, USBRBIAS, HSIC_STROBE, HSIC_DATA.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 6.2, "Operating Conditions**", Section 6.4, "DC Specifications", or any other applicable section of this specification is not implied. Note, device signals are *NOT* 5 Volt tolerant unless specified otherwise.

6.2 Operating Conditions**

+3.3 V Supply Voltage (VDD33IO, VDD33A) . . . . . +3.3 V +/-10%

+1.2 V Supply Voltage (VDD12CORE, VDD12PLL, VDD12USBPLL, VDD12A) . . . . . +1.2 V +/-5%

Ambient Operating Temperature in Still Air (T_A) . . . . . Note 6.4

Note 6.4 0°C to +70°C for commercial version, -40°C to +85°C for industrial version.

**Proper operation of the device is guaranteed only within the ranges specified in this section.

6.3 Power Consumption

This section details the power consumption of the device as measured during various modes of operation. Power consumption values are provided for both the device-only, and for the device plus Ethernet components. Power dissipation is determined by temperature, supply voltage and external source/sink requirements.

Note: All current consumption and power dissipation values were measured with VDD33IO and VDD33A equal to 3.3 V.

6.3.1 Power Consumption - Internal Regulator Disabled

6.3.1.1 SUSPEND0 - Internal Regulator Disabled

Table 6.1 Power Consumption/Dissipation - SUSPEND0 - Int. Reg. Disabled

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (device only)		30		mA
Supply current (VDD12CORE, VDD12USBPLL, VDD12A, VDD12PLL) (device only)		19		mA
Power dissipation (device only)		121		mW
Power dissipation (device and Ethernet components)		255		mW

6.3.1.2 SUSPEND1 - Internal Regulator Disabled

Table 6.2 Power Consumption/Dissipation - SUSPEND1 - Int. Reg. Disabled

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (device only)		5		mA
Supply current (VDD12CORE, VDD12USBPLL, VDD12A, VDD12PLL) (device only)		3		mA
Power dissipation (device only)		19		mW
Power dissipation (device and Ethernet components)		19		mW

6.3.1.3 SUSPEND2 - Internal Regulator Disabled

Table 6.3 Power Consumption/Dissipation - SUSPEND2 - Int. Reg. Disabled

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (device only)		1		mA
Supply current (VDD12CORE, VDD12USBPLL, VDD12A, VDD12PLL) (device only)		1		mA

Table 6.3 Power Consumption/Dissipation - SUSPEND2 - Int. Reg. Disabled

PARAMETER	MIN	TYPICAL	MAX	UNIT
Power dissipation (device only)		5		mW
Power dissipation (device and Ethernet components)		6		mW

6.3.1.4 SUSPEND3 - Internal Regulator Disabled

Table 6.4 Power Consumption/Dissipation - SUSPEND3 - Int. Reg. Disabled

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (device only)		30		mA
Supply current (VDD12CORE, VDD12USBPLL, VDD12A, VDD12PLL) (device only)		37		mA
Power dissipation (device only)		145		mW
Power dissipation (device and Ethernet components)		279		mW

6.3.1.5 Operational - Internal Regulator Disabled

Table 6.5 Operational Power Consumption/Dissipation - Int. Reg. Disabled

PARAMETER	MIN	TYPICAL	MAX	UNIT
100BASE-TX Full Duplex (HSIC)				
Supply current (VDD33IO, VDD33A) (device only)		32		mA
Supply current (VDD12CORE, VDD12USBPLL, VDD12A, VDD12PLL) (device only)		42		mA
Power dissipation (device only)		156		mW
Power dissipation (device and Ethernet components)		292		mW
10BASE-T Full Duplex (HSIC)				
Supply current (VDD33IO, VDD33A) (device only)		12		mA
Supply current (VDD12CORE, VDD12USBPLL, VDD12A, VDD12PLL) (device only)		32		mA
Power dissipation (device only)		77		mW
Power dissipation (device and Ethernet components)		407		mW

6.3.2 Power Consumption - Internal Regulator Enabled

6.3.2.1 SUSPEND0 - Internal Regulator Enabled

Table 6.6 Power Consumption/Dissipation - SUSPEND0 - Int. Reg. Enabled

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (device only)		50		mA
Power dissipation (device only)		164		mW
Power dissipation (device and Ethernet components)		296		mW

6.3.2.2 SUSPEND1 - Internal Regulator Enabled

Table 6.7 Power Consumption/Dissipation - SUSPEND1 - Int. Reg. Enabled

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (device only)		8		mA
Power dissipation (device only)		26		mW
Power dissipation (device and Ethernet components)		26		mW

6.3.2.3 SUSPEND2 - Internal Regulator Enabled

Table 6.8 Power Consumption/Dissipation - SUSPEND2 - Int. Reg. Enabled

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (device only)		3		mA
Power dissipation (device only)		9		mW
Power dissipation (device and Ethernet components)		10		mW

6.3.2.4 SUSPEND3 - Internal Regulator Enabled

Table 6.9 Power Consumption/Dissipation - SUSPEND3 - Int. Reg. Enabled

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (device only)		69		mA
Power dissipation (device only)		228		mW
Power dissipation (device and Ethernet components)		361		mW

6.3.2.5 Operational - Internal Regulator Enabled

Table 6.10 Operational Power Consumption/Dissipation - Int. Reg. Enabled

PARAMETER	MIN	TYPICAL	MAX	UNIT
100BASE-TX Full Duplex (HSIC)				
Supply current (VDD33IO, VDD33A) (device only)		71		mA
Power dissipation (device only)		235		mW
Power dissipation (device and Ethernet components)		370		mW
10BASE-T Full Duplex (HSIC)				
Supply current (VDD33IO, VDD33A) (device only)		44		mA
Power dissipation (device only)		146		mW
Power dissipation (device and Ethernet components)		478		mW

6.4 DC Specifications

Table 6.11 I/O Buffer Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
IS Type Input Buffer						
Low Input Level	V_{ILI}	-0.3			V	
High Input Level	V_{IHI}			3.6	V	
Negative-Going Threshold	V_{ILT}	1.01	1.19	1.39	V	Schmitt trigger
Positive-Going Threshold	V_{IHT}	1.39	1.59	1.8	V	Schmitt trigger
SchmittTrigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	336	399	485	mV	
Input Leakage (V_{IN} = VSS or VDD33IO)	I_{IH}	-10		10	µA	Note 6.5
Input Capacitance	C_{IN}			3	pF	
O8 Type Buffers						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA
High Output Level	V_{OH}	VDD33IO - 0.4			V	I_{OH} = -8 mA
OD8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA
O12 Type Buffers						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
High Output Level	V_{OH}	VDD33IO - 0.4			V	I_{OH} = -12 mA
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
HSIC Type Buffers						
Low Input Level	V_{IL}	-0.3		0.35*VDD12A	V	
High Input Level	V_{IH}	0.65*VDD12A		VDD12A + 0.3	V	
Low Output Level	V_{OL}			0.25*VDD12A	V	
High Output Level	V_{OH}	0.75*VDD12A			V	
I/O Pad Drive Strength (50DRIVER_EN = VSS)	O_D	38	40	42	Ohm	
I/O Pad Drive Strength (50DRIVER_EN = +3.3V)	O_D	47.5	50	52.5	Ohm	
Input Leakage (V_{IN} = VSS or VDD33IO)	I_{IH}	-10		10	µA	
Input Capacitance	C_{IN}			4	pF	

Table 6.11 I/O Buffer Characteristics (continued)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
ICLK Type Buffer (XI Input)						Note 6.6
Low Input Level	V_{ILI}	-0.3		0.5	V	
High Input Level	V_{IHI}	1.4		3.6	V	

Note 6.5 This specification applies to all inputs and tri-stated bi-directional pins. Internal pull-down and pull-up resistors add +/- 50 µA per-pin (typical).

Note 6.6 XI can optionally be driven from a 25 MHz single-ended clock oscillator.

Table 6.12 100BASE-TX Transceiver Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Peak Differential Output Voltage High	V_{PPH}	950	-	1050	mVpk	Note 6.7
Peak Differential Output Voltage Low	V_{PPL}	-950	-	-1050	mVpk	Note 6.7
Signal Amplitude Symmetry	V_{SS}	98	-	102	%	Note 6.7
Signal Rise and Fall Time	T_{RF}	3.0	-	5.0	ns	Note 6.7
Rise and Fall Symmetry	T_{RFS}	-	-	0.5	ns	Note 6.7
Duty Cycle Distortion	D_{CD}	35	50	65	%	Note 6.8
Overshoot and Undershoot	V_{OS}	-	-	5	%	
Jitter				1.4	ns	Note 6.9

Note 6.7 Measured at line side of transformer, line replaced by 100 Ω (+/-1%) resistor.

Note 6.8 Offset from 16 ns pulse width at 50% of pulse peak.

Note 6.9 Measured differentially.

Table 6.13 10BASE-T Transceiver Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Transmitter Peak Differential Output Voltage	V_{OUT}	2.2	2.5	2.8	V	Note 6.10
Receiver Differential Squelch Threshold	V_{DS}	300	420	585	mV	

Note 6.10 Min/max voltages guaranteed as measured with 100 Ω resistive load.

6.5 AC Specifications

This section details the various AC timing specifications of the device.

Note: The HSIC_DATA and HSIC_STROBE pin timing adheres to the HSIC 1.0 specification. Refer to the High-Speed Interchip USB Electrical Specification Revision 1.0 (09-23-07) and USB HSIC ECN for detailed USB timing information.

Note: The Ethernet TX/RX pin timing adheres to the IEEE 802.3 specification. Refer to the IEEE 802.3 specification for detailed Ethernet timing information.

6.5.1 Equivalent Test Load

Output timing specifications assume the 25 pF equivalent test load illustrated in Figure 6.1 below, unless otherwise specified.

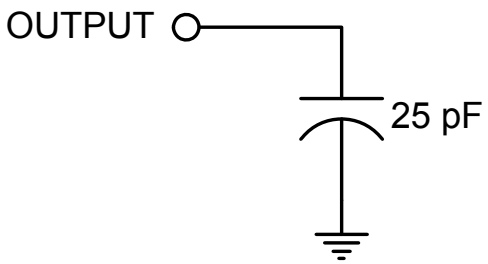


Figure 6.1 Output Equivalent Test Load

6.5.2 Power Sequence Timing

Power supplies must adhere to the following rules:

- All power supplies of the same voltage must be powered up/down together.
- There is no power-up sequencing requirement, however all power supplies must reach operational levels within the time periods specified in Table 6.14.
- There is no power-down sequencing or timing requirement, however the device must not be powered for an extended period of time without all supplies at operational levels.
- Do not drive input signals without power supplied to the device.

Note: When operating with an external 1.2 V power source, the 1.2 V input must not exceed the 3.3 V source by more than 0.4 V.

Note: Violation of these specifications may damage the device.

Note: A Power-On Reset (POR) occurs whenever power is initially applied to the device, or if power is removed and reapplied to the device. A timer within the device will assert the internal reset for approximately 22 ms.

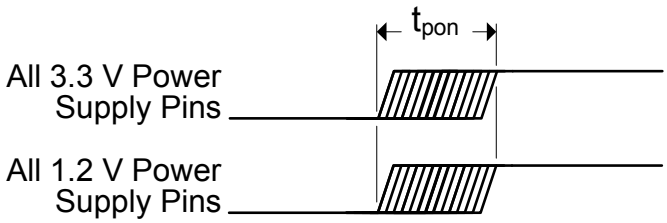


Figure 6.2 Power Sequence Timing

Table 6.14 Power Sequence Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{pon}	Power supply turn on time	0		25	ms

6.5.3 Power-On Configuration Strap Valid Timing

Figure 6.3 illustrates the configuration strap valid timing requirement in relation to power-on. In order for valid configuration strap values to be read at power-on, the following timing requirements must be met.

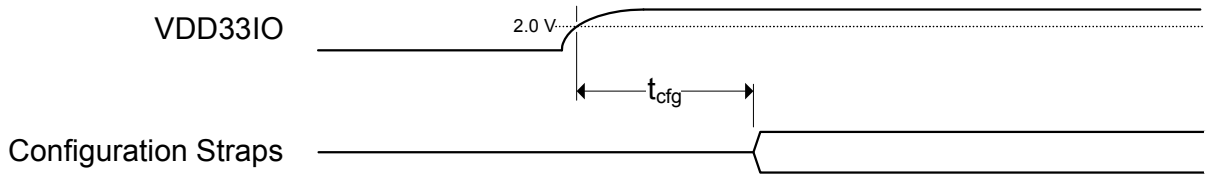


Figure 6.3 Power-On Configuration Strap Valid Timing

Table 6.15 Power-On Configuration Strap Valid Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{cfg}	Configuration strap valid time			15	ms

6.5.4 Reset and Configuration Strap Timing

Figure 6.4 illustrates the nRESET pin timing requirements and its relation to the configuration strap pins and output drive. Assertion of nRESET is not a requirement. However, if used, it must be asserted for the minimum period specified.

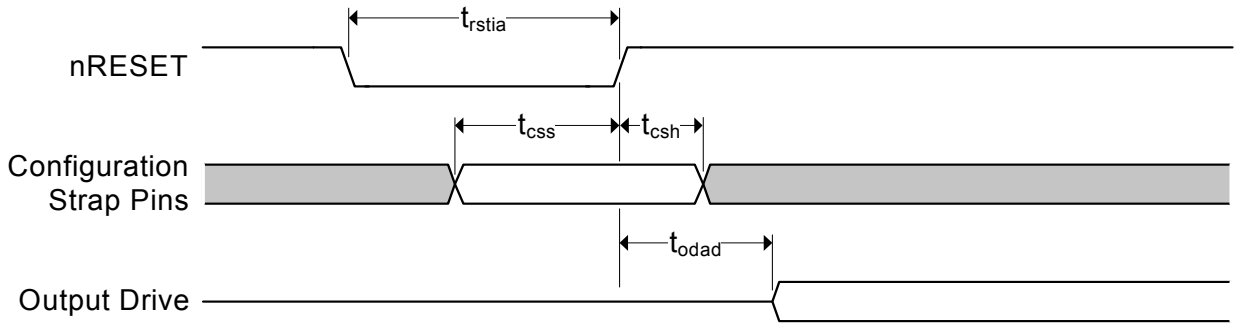


Figure 6.4 nRESET Reset Pin Timing

Table 6.16 nRESET Reset Pin Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{rstia}	nRESET input assertion time	1			µs
t_{css}	Configuration strap pins setup to nRESET deassertion	200			ns
t_{csh}	Configuration strap pins hold after nRESET deassertion	10			ns
t_{odad}	Output drive after nRESET deassertion	30			ns

6.5.5 EEPROM Timing

The following specifies the EEPROM timing requirements for the device:

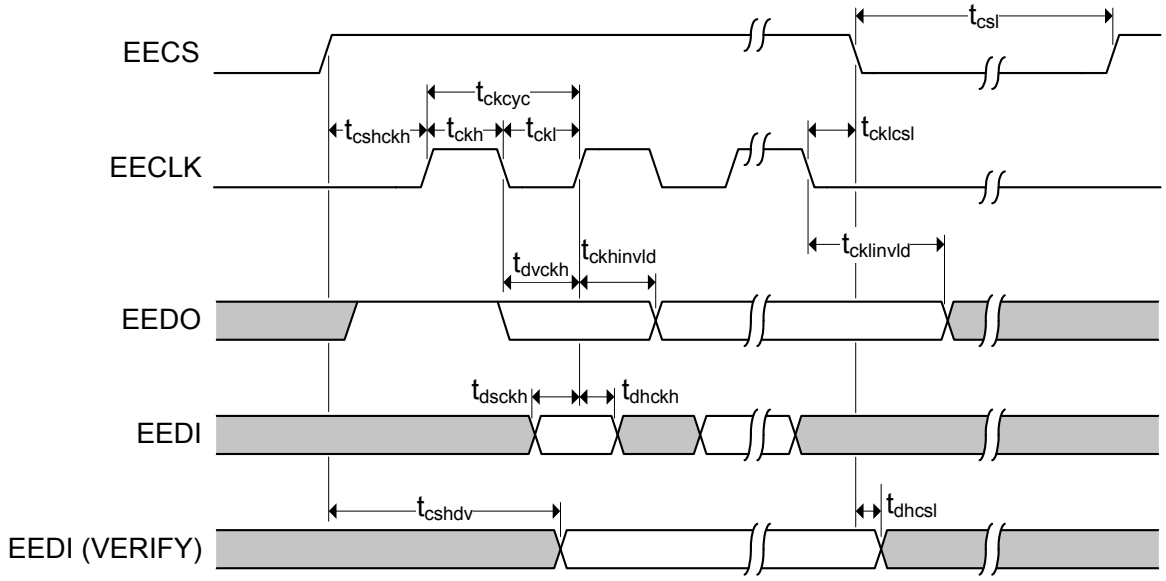


Figure 6.5 EEPROM Timing

Table 6.17 EEPROM Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ckcyc}	EECLK cycle time	1110		1130	ns
t_{ckh}	EECLK high time	550		570	ns
t_{ckl}	EECLK low time	550		570	ns
t_{cshckh}	EECS high before rising edge of EECLK	1070			ns
t_{cklcsl}	EECLK falling edge to EECS low	30			ns
t_{dvckh}	EEDO valid before rising edge of EECLK	550			ns
$t_{ckhinvld}$	EEDO invalid after rising edge EECLK	550			ns
t_{dsckh}	EEDI setup to rising edge of EECLK	90			ns
t_{dhckh}	EEDI hold after rising edge of EECLK	0			ns
$t_{cklinvld}$	EECLK low to data invalid (OUTPUT)	580			ns
t_{cshdv}	EEDIO valid after EECS high (VERIFY)			600	ns
t_{dhcsl}	EEDIO hold after EECS low (VERIFY)	0			ns
t_{csl}	EECS low	1070			ns

6.5.6 MII Interface Timing

This section specifies the MII interface transmit and receive timing.

Note: The MII timing adheres to the IEEE 802.3 specification. Refer to the IEEE 802.3 specification for additional MII timing information.

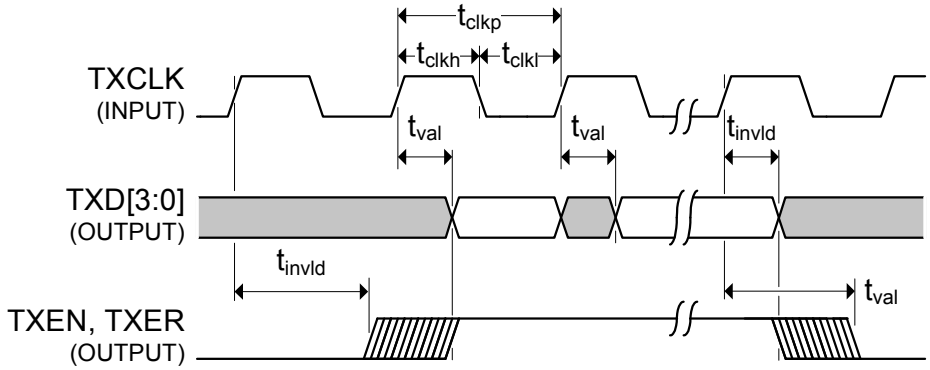


Figure 6.6 MII Transmit Timing

Table 6.18 MII Transmit Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	TXCLK period	40		ns	
t_{clkh}	TXCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	TXCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{val}	TXD[3:0], TXEN, TXER output valid from rising edge of TXCLK		22.0	ns	Note 6.11
t_{invld}	TXD[3:0], TXEN, TXER output invalid from rising edge of TXCLK	0		ns	Note 6.11

Note 6.11 Timing was designed for a system load between 10 pf and 25 pf.

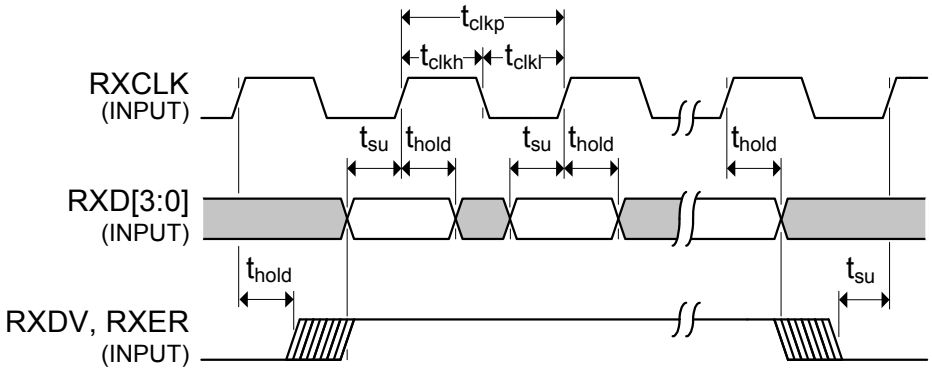


Figure 6.7 MII Receive Timing

Table 6.19 MII Receive Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	RXCLK period	40		ns	
t_{clkh}	RXCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	RXCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{su}	RXD[3:0], RXDV setup time to rising edge of RXCLK	8.0		ns	Note 6.12
t_{hold}	RXD[3:0], RXDV hold time after rising edge of RXCLK	9.0		ns	Note 6.12

Note 6.12 Timing was designed for a system load between 10 pf and 25 pf.

6.5.7 Turbo MII Interface Timing

This section specifies the Turbo MII interface transmit and receive timing.

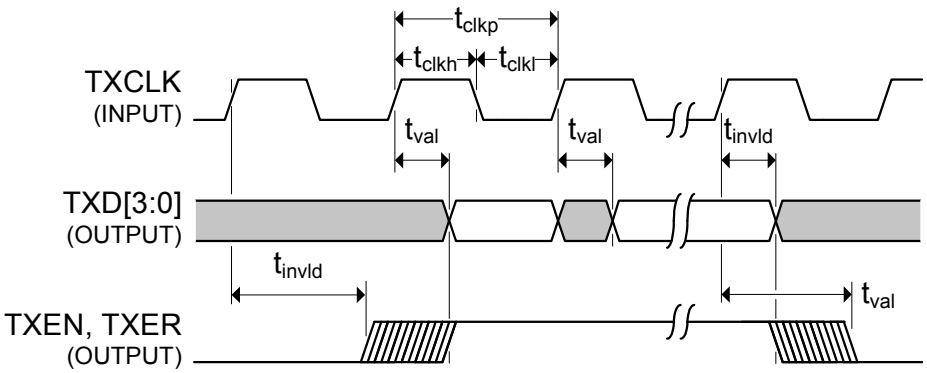


Figure 6.8 Turbo MII Transmit Timing

Table 6.20 Turbo MII Transmit Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	TXCLK period	20		ns	
t_{clkh}	TXCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	TXCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{val}	TXD[3:0], TXEN, TXER output valid from rising edge of TXCLK		12.5	ns	Note 6.13
t_{invld}	TXD[3:0], TXEN, TXER output invalid from rising edge of TXCLK	1.5		ns	Note 6.13

Note 6.13 Timing was designed for a system load between 10 pf and 15 pf.

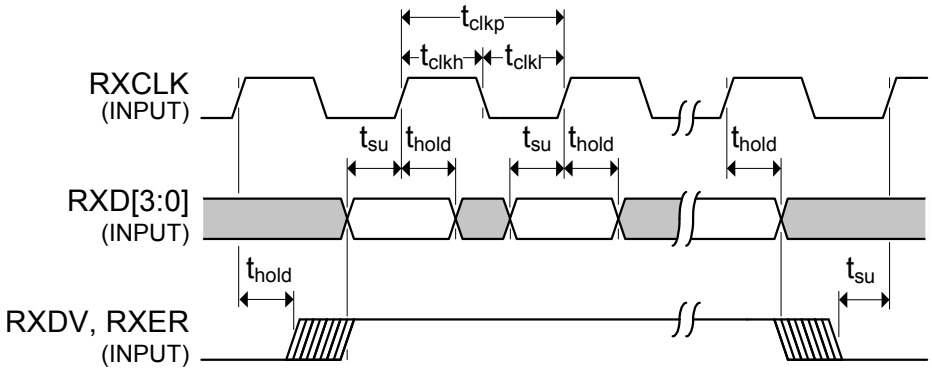


Figure 6.9 Turbo MII Receive Timing

Table 6.21 Turbo MII Receive Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	RXCLK period	20		ns	
t_{clkh}	RXCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	RXCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{su}	RXD[3:0], RXDV setup time to rising edge of RXCLK	5.5		ns	Note 6.14
t_{hold}	RXD[3:0], RXDV hold time after rising edge of RXCLK	0		ns	Note 6.14

Note 6.14 Timing was designed for a system load between 10 pf and 15 pf.

6.5.8 JTAG Timing

This section specifies the JTAG timing of the device.

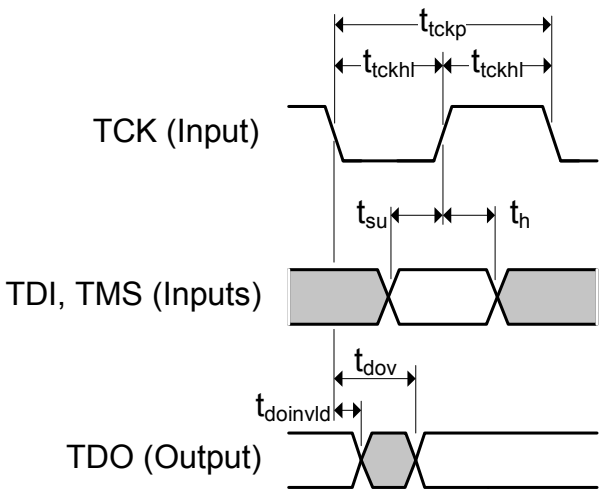


Figure 6.10 JTAG Timing

Table 6.22 JTAG Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{tckp}	TCK clock period	66.67		ns	
t_{tckhl}	TCK clock high/low time	t_{tckp}*0.4	t_{tckp}*0.6	ns	
t_{su}	TDI, TMS setup to TCK rising edge	10		ns	
t_h	TDI, TMS hold from TCK rising edge	10		ns	
t_{dov}	TDO output valid from TCK falling edge		16	ns	
$t_{doinvld}$	TDO output invalid from TCK falling edge	0		ns	

6.6 Clock Circuit

The device can accept either a 25 MHz crystal (preferred) or a 25 MHz single-ended clock oscillator (+/-50ppm) input. If the single-ended clock oscillator method is implemented, XO should be left unconnected and XI should be driven with a nominal 0-3.3 V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (XI/XO). See Table 6.23 for the recommended crystal specifications.

Table 6.23 Crystal Specifications

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	25.000	-	MHz	
Frequency Tolerance @ 25°C	F_{tol}	-	-	+/-50	PPM	Note 6.15
Frequency Stability Over Temp	F_{temp}	-	-	+/-50	PPM	Note 6.15
Frequency Deviation Over Time	F_{age}	-	+/-3 to 5	-	PPM	Note 6.16
Total Allowable PPM Budget		-	-	+/-50	PPM	Note 6.17
Shunt Capacitance	C_O	-	7 typ	-	pF	
Load Capacitance	C_L	-	20 typ	-	pF	
Drive Level	P_W	300	-	-	uW	
Equivalent Series Resistance	R_1	-	-	50	Ohm	
Operating Temperature Range		Note 6.18	-	Note 6.19	°C	
XI Pin Capacitance		-	3 typ	-	pF	Note 6.20
XO Pin Capacitance		-	3 typ	-	pF	Note 6.20

Note 6.15 The maximum allowable values for frequency tolerance and frequency stability are application dependant. Since any particular application must meet the IEEE +/-50 PPM Total PPM Budget, the combination of these two values must be approximately +/-45 PPM (allowing for aging).

Note 6.16 Frequency Deviation Over Time is also referred to as Aging.

Note 6.17 The total deviation for the Transmitter Clock Frequency is specified by IEEE 802.3u as +/-50 PPM.

Note 6.18 0°C for commercial version, -40°C for industrial version.

Note 6.19 +70°C for commercial version, +85°C for industrial version.

Note 6.20 This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The XO/XI pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

Chapter 7 Package Outline

7.1 56-Pin QFN Package

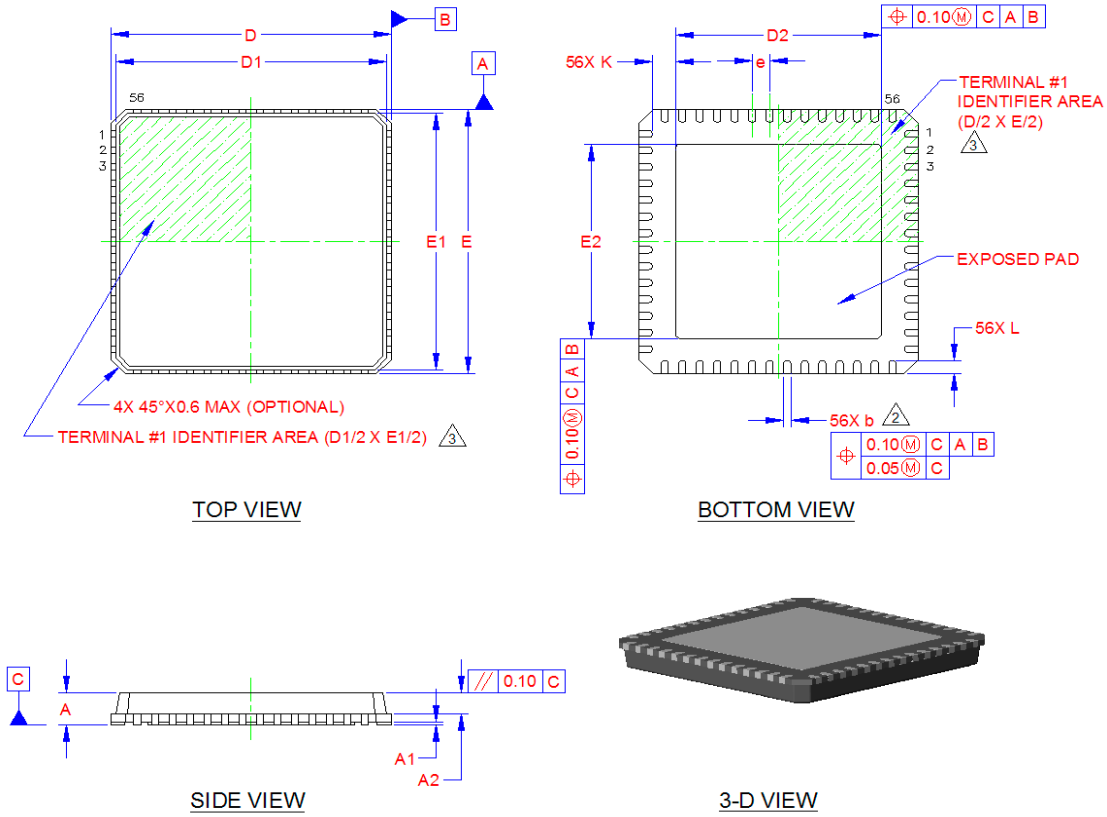


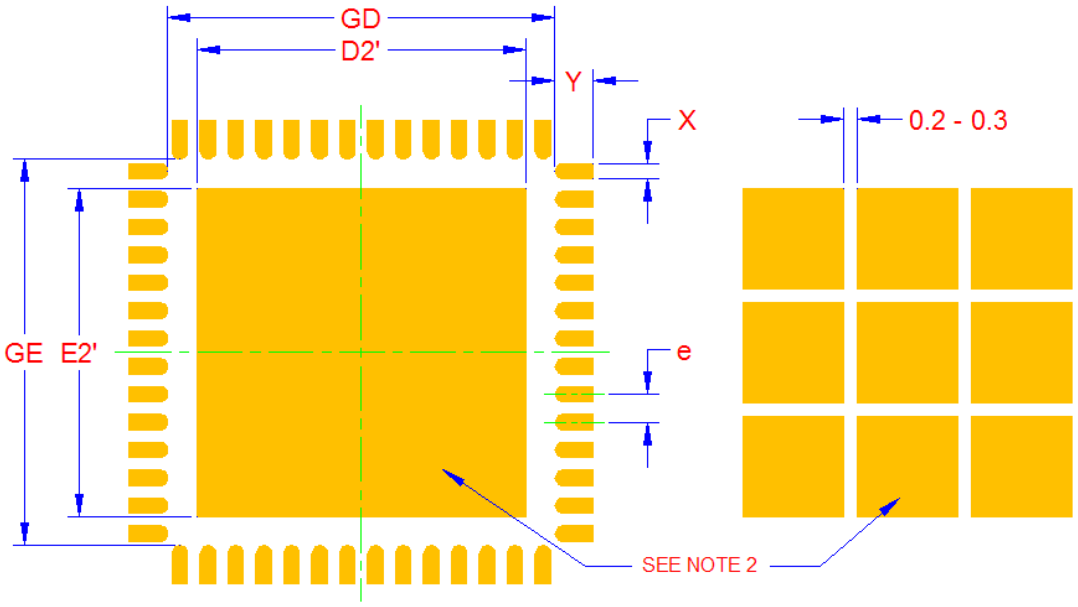
Figure 7.1 56-Pin QFN Package Definition

Table 7.1 56-Pin QFN Dimensions

	MIN	NOMINAL	MAX	REMARKS
A	0.70	0.85	1.00	Overall Package Height
A1	0.00	0.02	0.05	Standoff
A2	-	-	0.90	Mold Cap Thickness
D/E	7.85	8.00	8.15	X/Y Body Size
D1/E1	7.55	7.75	7.95	X/Y Mold Cap Size
D2/E2	5.80	5.90	6.00	X/Y Exposed Pad Size
L	0.30	0.40	0.50	Terminal Length
b	0.18	0.25	0.30	Terminal Width
K	0.55	-	-	Center Pad to Pin Clearance
e	0.50 BSC			Terminal Pitch

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Position tolerance of each terminal and exposed pad is +/-0.05 mm at maximum material condition. Dimension “b” applies to plated terminals and is measured between 0.15 and 0.30 mm from the terminal tip.
3. The pin 1 identifier may vary, but is always located within the zone indicated.



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	6.93	-	7.05
D2'/E2'	-	5.90	5.90
X	-	0.28	0.28
Y	-	0.69	0.69
e		0.50	

NOTES:
1. THE USER MAY MODIFY THE PCB LAND PATTERN DESIGN AND DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY
2. EXPOSED SOLDERABLE COPPER AREA OF THE CENTER PAD CAN BE EITHER SOLID OR SEGMENTED
3. MAXIMUM THERMAL AND ELECTRICAL PACKAGE PERFORMANCE IS ACHIEVED WHEN AN ARRAY OF SOLID VIAS IS INCORPORATED IN THE CENTER LAND PATTERN

PCB LAND PATTERN

Figure 7.2 56-QFN Recommended PCB Land Pattern

Chapter 8 Datasheet Revision History

Table 8.1 Customer Revision History

REVISION LEVEL AND DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.0 (10-11-11)	All	Initial release