NOR Flash with Mobile LPDDR 133-Ball MCP

M39L0Rx0x0U3

Features

Multichip Package

- One die of 128Mb or 256Mb (MUX I/O, multiple bank, multilevel interface, burst) Flash memory
- One die of 128Mb or 512Mb LPDDR
- Supply voltages:
  - $V_{DDF} = V_{DDQF} = 1.7–1.95V$
  - $V_{PPF} = 9V$ for fast program
  - $V_{DDD} = V_{DDQD} = 1.7–1.95V$
- Electronic signature:
  - Manufacturer code: 20h
  - Top device codes:
    M58LR128KC = 882Eh
    M58LR256KC = 881Ch
  - Bottom device codes:
    M58LR128KD = 882Fh
    M58LR256KD = 881Dh
- 133-ball VFBGA package
  - RoHS-compliant

Flash Memory

- Multiplexed address/data
- Synchronous/asynchronous read
  - Synchronous burst read mode: 66 MHz
  - Random access: 70ns
- Synchronous burst read suspend
- Programming time
  - 2.5µs typical word program time using buffer enhanced factory program command
- Memory organization
  - Multiple bank memory array: 16Mb banks
  - Parameter blocks (top or bottom location)
- Dual operations
  - Program/erase in one bank while read in others
  - No delay between READ and WRITE operations
- Block locking
  - All blocks locked at power-up
  - Any combination of blocks can be locked with zero latency
  - $\overline{WP}_F$ for block lock-down
  - Absolute write protection with $V_{PPF} = V_{SSF}$
- Security
  - 64-bit unique device number
  - 2112-bit user programmable OTP Cells
- CFI (common Flash interface)
- 100,000 PROGRAM/ERASE cycles per block

LPDDR

- Synchronous dynamic RAM
  - 128Mb organized as 4 banks of 2 MWords, each 16 bits wide, 1K page
  - 512Mb organized as 4 banks of 8 MWords, each 16 bits wide, 2K page
- DDR
  - Two data transfers/clock cycle
  - Clock rate: 128Mb = 133 MHz (MAX)
    512Mb = 166 MHz (MAX)
- Synchronous burst read and write
- Automatic precharge
- Byte write controlled by $LDQM_D$ and $UDQM_D$
- Low-power features:
  - Partial array self refresh (PASR)
  - Automatic temperature-compensated self refresh (ATCSR)
  - Driver strength (DS)

General Description

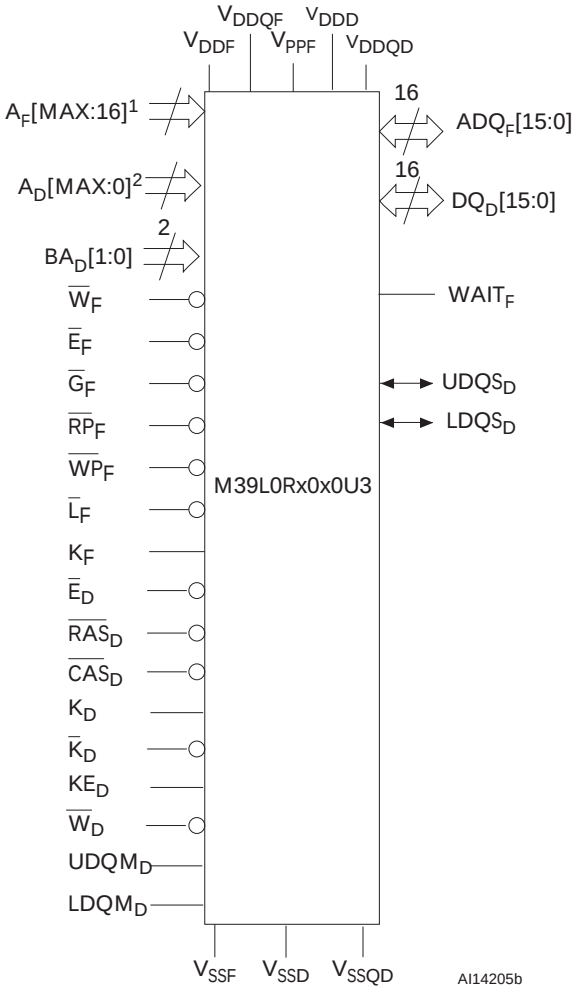
This MCP combines the following two memory devices:

- 128Mb or 256Mb multiplexed I/Os, multiple bank, multilevel interface, burst Flash memory (M58LRxxxKC/D)
- 128Mb or 512Mb LPDDR (M65KGxxxAM)

This document describes how the two memory components operate with respect to each other. It must be read in conjunction with the M58LRxxxKCD and M65KGxxxAM data sheets, where all specifications required to operate the Flash and LPDDR components are fully detailed. These data sheets are available from your local Micron distributor.

The M39L0Rx0x0U3 devices are offered in a stacked 133-ball VFBGA, 8mm × 8mm package, which is supplied with all the bits erased (set to 1).

Figure 1: Logic Diagram



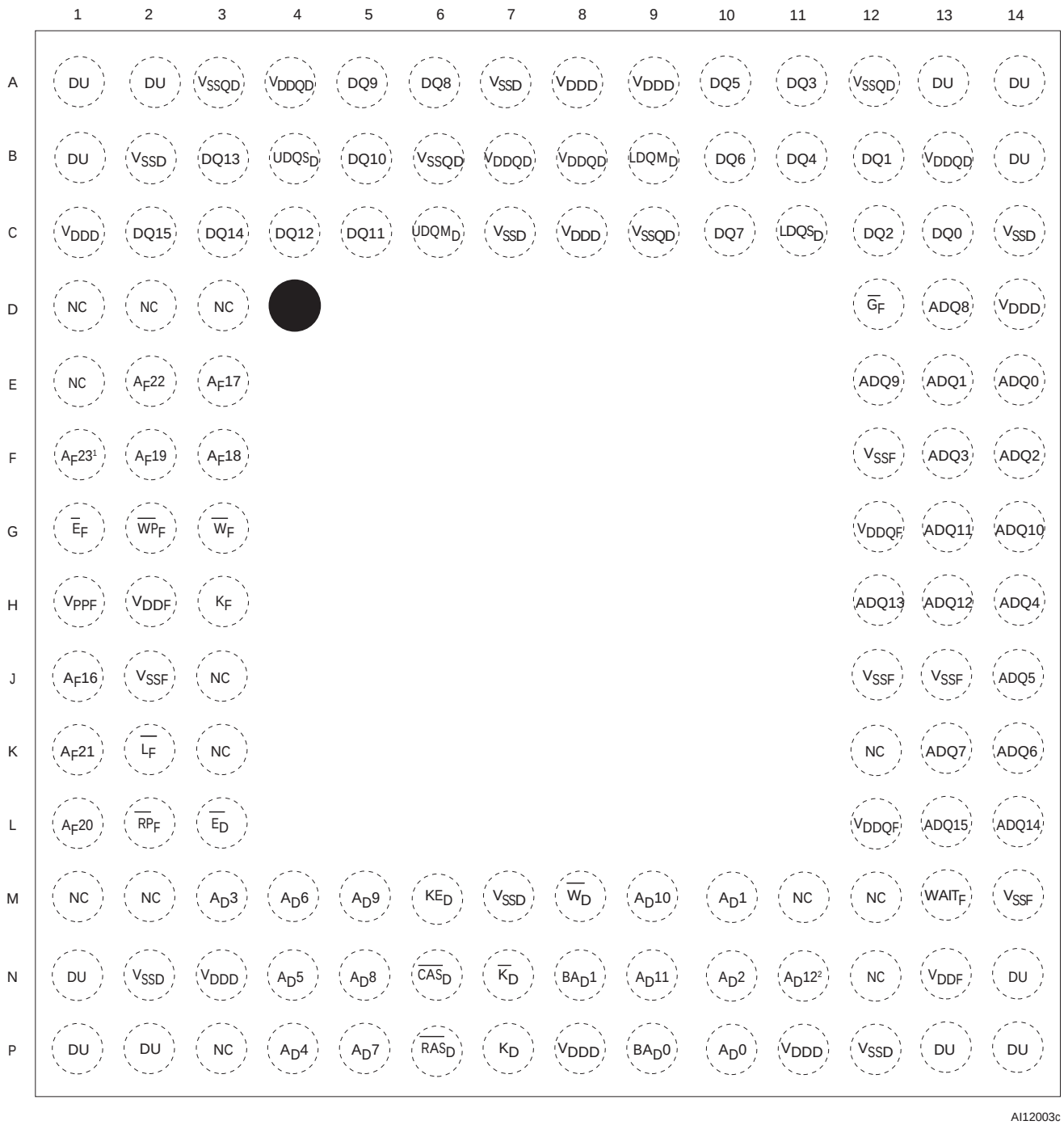
Notes: 1. AFMAX is AF22 for 128Mb and is AF23 for 256Mb Flash memory.
2. A_DMAX is A_D11 for 128Mb and is A_D12 for 512Mb LPDDR.

Ball Assignments and Descriptions

Table 1: Signal Names

Symbol	Type	Description
Shared Signals		
NC		Not connected internally
DU		Do not use
NOR Flash		
A_F[MAX:16]	Inputs	Address inputs
$\overline{E}_F$	Input	Chip enable
$\overline{G}_F$	Input	Output enable
$\overline{W}_F$	Input	Write enable
$\overline{RP}_F$	Input	Reset
$\overline{WP}_F$	Input	Write protect
K_F	Input	Clock
$\overline{L}_F$	Input	Latch enable
ADQ_F[15:0]	I/O	Data I/O or address inputs, command inputs
$WAIT_F$	Output	Wait
V_{DDF}		Supply voltage
V_{DDQF}		Supply voltage for I/O buffers
V_{PPF}		Optional supply voltage for fast program and erase
V_{SSF}		Ground
LPDDR		
A_D[MAX:0]	Inputs	address inputs
BA_D[1:0]	Inputs	Bank select inputs
K_D, $\overline{K}_D$	Inputs	Clock inputs
KE_D	Input	Clock enable input
$\overline{E}_D$	Input	Chip enable input
$\overline{W}_D$	Input	Write enable input
$\overline{RAS}_D$	Input	Row address strobe input
$\overline{CAS}_D$	Input	Column address strobe input
$UDQM_D$	Input	Upper data input mask
$LDQM_D$	Input	Lower data input mask
DQ_D[15:0]	I/O	Data inputs/outputs
$UDQS_D$	I/O	Upper data read/ write strobe I/O
$LDQS_D$	I/O	Lower data read/write strobe I/O
V_{DDD}		Supply voltage
V_{DDQD}		I/O supply voltage
V_{SSD}		Ground
V_{SSQD}		I/O ground

Figure 2: 133-Ball TFBGA (Top View, Balls Down)



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Notes: 1. A_F23 is NC for the 128Mb Flash memory (the M58LR128KCD).
2. A_D12 is NC for 128Mb LPDDR.

Signal Descriptions

Flash Memory Address Inputs ($ADQ_F[15:0]$ and $A_F[MAX:16]$)

The address inputs select the cells in the Flash memory array to access during bus READ operations. During bus WRITE operations they control the commands sent to the command interface of the Flash memory's program/erase controller.

A_FMAX is A_F23 for 256Mb Flash memory and it is A_F22 for 128Mb Flash memory.

FLash Memory Data I/Os ($ADQ_F[15:0]$)

The Flash memory data I/O output the data stored at the selected address during a bus READ operation or input a command or the data to be programmed during a bus WRITE operation.

Flash Memory Chip Enable ($\overline{E}_F$)

The chip enable input activates the Flash memory control logic, input buffers, decoders and sense amplifiers. When chip enable is at V_{IL} and reset is at V_{IH}, the device is in active mode. When chip enable is at V_{IH} the memory is deselected, the outputs are High-Z, and the power consumption is reduced to the standby level.

Flash Memory Output Enable ($\overline{G}_F$)

The output enable input controls data outputs during the bus READ operation of the memory.

Flash Memory Write Enable ($\overline{W}_F$)

The write enable input controls the bus WRITE operation of the memory's command interface. The data and address inputs are latched on the rising edge of chip enable or write enable, whichever occurs first.

Flash Memory RESET ($\overline{RP}_F$)

Reset provides a hardware reset of the memory. When reset is at V_{IL}, the memory is in reset mode, where the outputs are High-Z, and the current consumption is reduced to the reset supply current I_{DD2}. Refer to the M58LRxxxKCD data sheet for the value of I_{DD2}. After reset, all blocks are in the locked state and the configuration register is reset. When reset is at V_{IH}, the device is in normal operation. Upon exiting reset mode, the device enters asynchronous read mode, but a negative transition of chip enable or latch enable is required to ensure valid data outputs.

Flash Memory Write Protect ($\overline{WP}_F$)

Write protect is an input that provides an additional hardware protection for each block. When write protect is at V_{IL}, the lock-down is enabled and the protection status of the locked-down blocks cannot be changed. When write protect is at V_{IH}, the lock-down is disabled and the locked-down blocks can be locked or unlocked (refer to the M58LRxxxKCD data sheet).

Flash Memory Clock (K_F)

The clock input synchronizes the memory to the microcontroller during synchronous READ operations; the address is latched on a clock edge (rising or falling, according to the configuration settings) when latch enable is at V_{IL}. Clock is ignored during asynchronous READ and in WRITE operations.

Flash Memory Latch Enable ($\overline{L}_F$)

Latch enable latches the ADQ_F[15:0] and A_F[MAX:16] address bits on its rising edge. The address latch is transparent when Latch Enable is at V_{IL} and it is inhibited when latch enable is at V_{IH}.

Flash Memory Wait ($WAIT_F$)

Wait is an output signal used during synchronous read to indicate whether the data on the output bus are valid. This output is High-Z when chip enable is at V_{IH} or reset is at V_{IL}. It can be configured to be active during the wait cycle or one clock cycle in advance. The $WAIT_F$ signal is forced de-asserted when output enable is at V_{IH}.

Flash Memory V_{DDF} Supply Voltage

V_{DDF} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (READ, PROGRAM, and ERASE).

Flash Memory V_{DDQF} Supply Voltage

V_{DDQF} provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{DDF}. V_{DDQF} can be tied to V_{DDF} or can use a separate supply.

Flash Memory V_{PPF} Program Supply Voltage

V_{PPF} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0 V to V_{DDQF}), V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLK} gives absolute protection against program or erase, while V_{PPF} in the V_{PP1} range enables these functions (see the M58LRxxxKCD data sheet for the relevant values). V_{PPF} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and PROGRAM or ERASE operations continue.

If V_{PPF} is in the range of V_{PPH} it acts as a power supply pin. In this situation V_{PPF} must be stable until the program/erase algorithm is completed.

Flash Memory V_{SSF} Ground

V_{SSF} ground is the reference for the core supply. It must be connected to the system ground.

LPDDR Address Inputs (A_D[MAX:0])

The A_D[MAX:0] address inputs select the LPDDR row or column to be made active.

For 128Mb LPDDR:

- If a row is selected, all twelve address inputs, A_D[11:0], are used.
- If a column is selected, only the nine least significant address inputs, A_D[8:0], are used.

For 512Mb LPDDR:

- If a row is selected, all thirteen address inputs, A_D[12:0], are used.
- If a column is selected, only the ten least significant address inputs, A_D[9:0], are used.

In this latter case, $A10_D$ determines whether auto precharge is used:

- During a READ or WRITE operation:

  - If A_D10 is HIGH (set to 1), the read or write operation includes an auto precharge cycle.
  - If A_D10 is Low (set to '0'), the READ or WRITE cycle does not include an auto precharge cycle.
- When issuing a PRECHARGE command:
  - If A_D10 is LOW, only the bank selected by $BA_D[1:0]$ is precharged.
  - If A_D10 is HIGH, all the banks are precharged.

The address inputs are latched at the cross point of K_D rising edge and $\overline{K}_D$ falling edge.

LPDDR Data I/Os ($DQ_D[15:0]$)

The LPDDR data I/O output the data stored at the selected address during a READ operation, or to input the data during a WRITE operation.

LPDDR Bank Select Address Inputs ($BA_D[1:0]$)

The bank select address inputs, BA_D0 and BA_D1, select the LPDDR bank to be made active (see the M65KGxxxAM data sheet for details).

When selecting the addresses, the device must be enabled, the row address strobe, $\overline{RAS}_D$, must be LOW, V_{IL}, the column address strobe, $\overline{CAS}_D$, and $\overline{W}_D$ must be HIGH, V_{IH}.

LPDDR Clock Inputs (K_D, $\overline{K}_D$)

The clock signals, K_D and $\overline{K}_D$, are the master clock inputs. All input signals except $UDQM_D/LDQM_D$, $UDQS_D/LDQS_D$ and $DQ_D[15:0]$ are referred to the cross point of K_D rising edge and $\overline{K}_D$ falling edge. During READ operations, $UDQS_D/LDQS_D$ and $DQ_D[15:0]$ are referred to the crosspoint of K_D rising edge and $\overline{K}_D$ falling edge. During WRITE operations, $UDQM_D/LDQM_D$ and $DQ_D[15:0]$ are referred to the crosspoint of $UDQS_D/LDQS_D$ and VREF, and $UDQS_D/LDQS_D$ to the crosspoint of K_D rising edge and $\overline{K}_D$ falling edge.

LPDDR Clock Enable (KE_D)

When driven LOW, V_{IL}, the clock enable input, KE_D, is used to suspend the Clock K_D, to switch the device to self refresh or power-down.

The clock enable, KE_D, must be stable for at least one clock cycle. This means that if KE_D level changes on K_D rising edge and $\overline{K}_D$ falling edge with a setup time of ^tAS, it must be at the same level by the next K_D rising edge with a hold time of ^tAH.

LPDDR Chip Enable ($\overline{E}_D$)

The chip enable input, $\overline{E}_D$, activates the memory state machine, address buffers and decoders when driven Low, V_{IL}. When $\overline{E}_D$ is High, V_{IH}, the device is not selected.

LPDDR Write Enable ($\overline{W}_D$)

The write enable input, $\overline{W}_D$, controls writing.

LPDDR Row Address Strobe ($\overline{RAS}_D$)

The row address strobe, $\overline{RAS}_D$, is used in conjunction with address inputs $A_D[MAX:0]$ and $BA_D[1:0]$, to select the starting address location prior to a READ or WRITE operation.

LPDDR Column Address Strobe ($\overline{CAS}_D$)

The column address strobe, $\overline{CAS}_D$, is used in conjunction with address inputs A_D[8:0] for 128Mb or A_D[9:0] for 512Mb and BA_D[1:0], to select the starting column location prior to a READ or WRITE operation.

LPDDR Lower/Upper Data Input Mask ($LDQM_D$, $UDQM_D$)

Lower data input mask and upper data input mask are input signals used to mask the written data. $UDQM_D$ and $LDQM_D$ are sampled when $UDQS_D$/$LDQS_D$ level crosses V_{REF}. When $LDQM_D$ is LOW, V_{IL}, DQ_D[7:0] I/Os are enabled. When $UDQM_D$ is LOW, V_{IL}, DQ_D[15:8] I/Os are enabled.

LPDDR Lower/Upper Data Read/Write Strobe I/O ($LDQS_D$, $UDQS_D$)

$LDQS_D$ and $UDQS_D$ can be either input or output signals and act as write data strobe and read data strobe respectively. $LDQS_D$ and $UDQS_D$ are the strobe signals for DQ_D[7:0] and DQ_D[15:8], respectively.

LPDDR V_{DDD} Supply Voltage

V_{DDD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (READ and WRITE). It is recommended to power up and power down V_{DDD} and V_{DDQD} together to avoid conditions that would result in data corruption.

LPDDR V_{DDQD} Supply Voltage

V_{DDQD} provides the power supply to the I/O pins and enables all outputs to be powered independently of V_{DDD}. V_{DDQD} can be tied to V_{DDD} or can use a separate supply. It is recommended to power-up V_{DDQD} simultaneously with or after V_{DDD} to avoid data corruption.

LPDDR V_{SSD} Ground

Ground, V_{SSD}, is the reference for the core power supply. It must be connected to the system ground.

LPDDR V_{SSQD} Ground

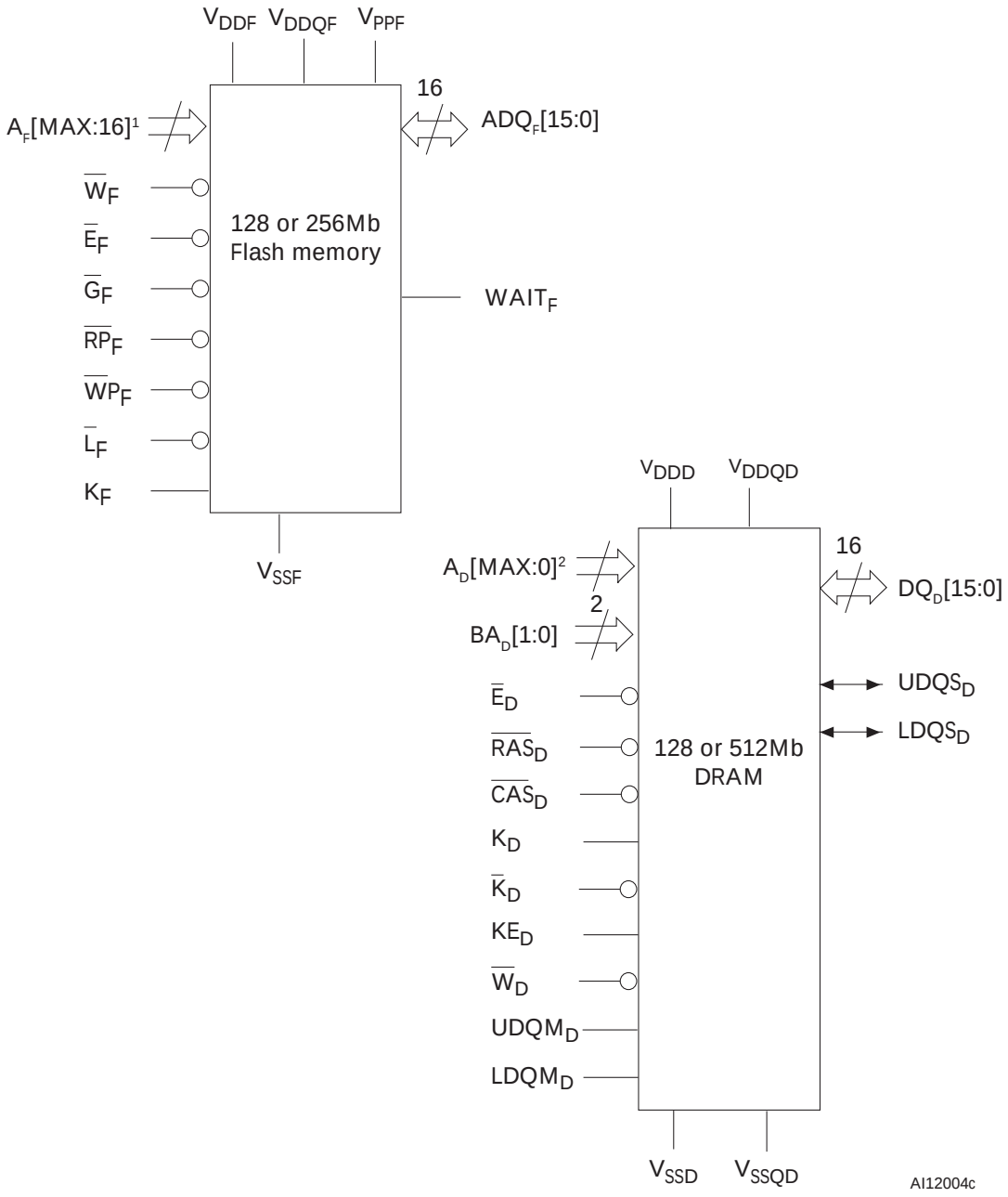
V_{SSQD} ground is the reference for the input/output circuitry driven by V_{DDQD}. V_{SSQD} must be connected to V_{SSD}.

Note: Each device in a system should have V_{DDD}, V_{DDQD}, V_{DDF}, V_{DDQF} and V_{PPF} decoupled with a 0.1µF ceramic capacitor close to the pin (high-frequency, inherently-low inductance capacitors should be as close as possible to the package). See Figure 5: AC Measurement Load Circuit. The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.

Functional Description

The LPDDR and Flash memory components have no signals in common. They have separate power supplies and grounds. Chip enable input EF is used to select the Flash memory and Chip enable input ED is used to select the LPDDR.

Figure 3: FunctioNal Block Diagram



Notes:
1. A_FMAX is A_F22 for 128Mb and A_F23 for 256Mb Flash memory.
2. A_DMAX is A_D11 for 128Mb and A_D12 for 512Mb LPDDR.

Maximum Ratings

Stressing the device above the ratings listed may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2: AbSolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient operating temperature	–40	85	°C
T_{BIAS}	Temperature under bias	–40	85	°C
T_{STG}	Storage temperature	–55	125	°C
V_{IO}	Input or output voltage	–0.5	2.45	V
V_{DDF}	Flash memory supply voltage	–0.2	2.45	V
V_{DDQF}	Flash memory input/output supply voltage	–0.2	2.45	V
V_{DDD}	LPDDR supply voltage	–0.2	2.45	V
V_{DDQD}	LPDDR I/O supply voltage	–0.2	2.45	V
V_{PPF}	Flash memory program voltage	–0.2	10	V
I_O	Output short circuit current		100	mA
t_{VPPH}	Time for V_{PPF} at V_{PPH}		100	hours

DC and AC Parameters

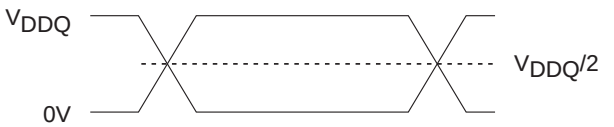
The parameters in the DC and AC characteristics tables that follow are derived from tests performed under the measurement conditions summarized below. Designers must check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 3: Operating and AC measurement conditions

Parameter	Flash Memory		LPDDR			Unit
	Min	Max	Min	Typ	Max	
V_{DDF} supply voltage	1.7	1.95	–	–	–	V
V_{DDD} supply voltage	–	–	1.7	1.8	1.95	V
V_{DDQF} supply voltage	1.7	1.95	–	–	–	V
V_{DDQD}[1] supply voltage	–	–	1.7	1.8	1.95	V
V_{PPF} supply voltage (factory environment)	8.5	9.5	–	–	–	V
V_{PPF} supply voltage (application environment)	–0.4	V_{DDQF} + 0.4	–	–	–	V
Load capacitance (C_L)	30		30			pF
Output circuit resistors (R_1, R_2)	16.7		–			kΩ
Input rise and fall times		5			2	ns
Input low voltage (V_{IL})	0		0.2			V
Input high voltage (V_{IH})	V_{DDQ}		1.6			V
I/O timing reference voltages	V_{DDQF}/2		V_{DDQD}/2			V

Notes: 1. V_{DDD} must be equal to V_{DDQD}.

Figure 4: AC Measurement I/O Waveform



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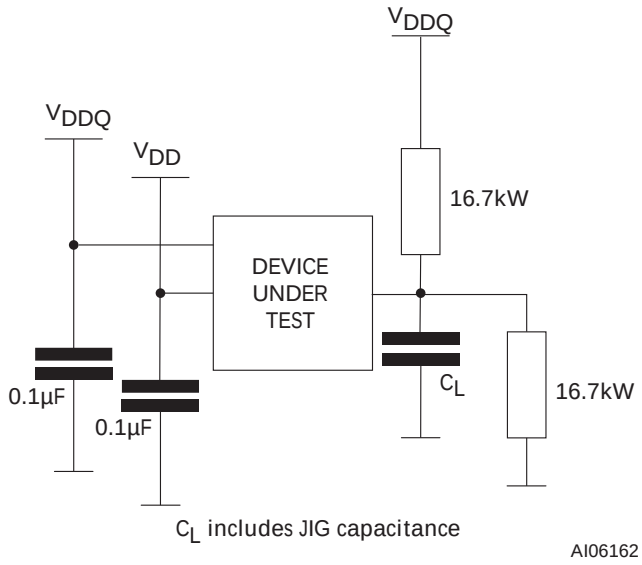
Notes: 1. V_{DDQ} means either V_{DDQF} or V_{DDQD}.

Figure 5: AC Measurement Load Circuit



Notes: 1. V_{DD} means either V_{DDF} or V_{DDD}. V_{DDQ} means either V_{DDQF} or V_{DDQD}.

Table 4: Capacitance[1]

Symbol	Parameter	Test condition	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0V	–	11	pF
C_{OUT}	Output capacitance	V_{OUT} = 0V	–	16	pF

Notes: 1. Sampled only, not 100% tested.
2. Refer to the device data sheets for further DC and AC characteristics values and illustrations.

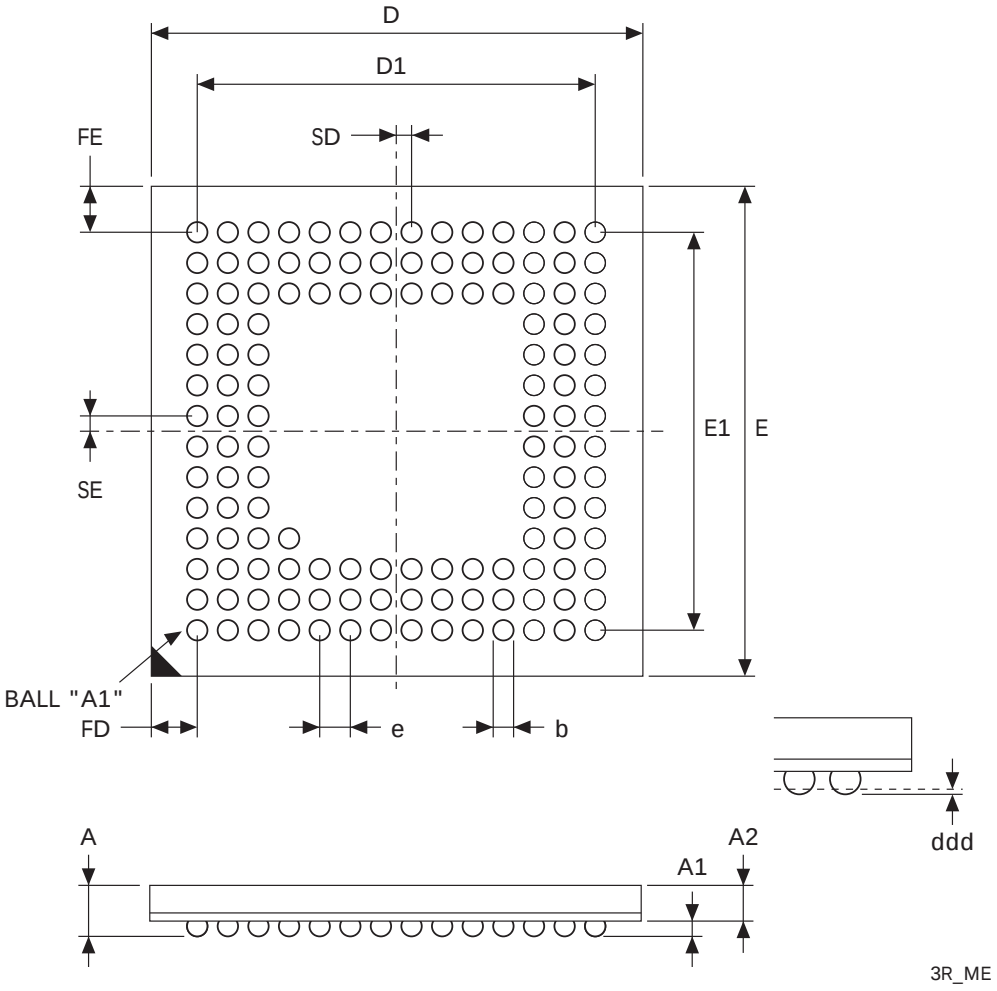
Package Dimensions

To meet environmental requirements, Micron offers these devices in RoHS-compliant packages, which have a lead-free, second-level interconnect. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label.

RoHS-compliant specifications are available at: www.micron.com.

Figure 6: 133-Ball VFBGA, 8mm × 8mm – 3R14 × 14 Active Ball Array, 0.5mm Pitch



Notes: 1. Drawing is not to scale.

Package Data

Table 5: 133-Ball VFBGA, 8mm × 8mm – 3R14 × 14 Active Ball Array, 0.5mm Pitch

Symbol	Millimeters		
	Typ	Min	Max
A			1.00
A1		0.15	
A2	0.64		
b	0.30	0.25	0.35
D	8.00	7.90	8.10
D1	6.50		
ddd			0.08
E	8.00	7.90	8.10
E1	6.50		
e	0.50	-	-
FD	0.75		
FE	0.75		
SD	0.25		
SE	0.25		

Part Numbering

Table 6: Ordering Information Scheme

Example:	M39	L	0	R	x	0	x	0	U	3	ZE	6	E

Device Type

M39 = Multichip package (Flash + LPDDR)

Flash 1 Architecture

L = Multilevel interface, multiple bank, burst mode

Flash 2 Architecture

0 = No die

Operating Voltage

R = V_{DDF} = V_{DDD} = V_{DDQD} = V_{DDQF} = 1.7V to 1.95V

Flash 1 Density

7 = 128Mb

8 = 256Mb

Flash 2 Density

0 = no die

LPDDR 1 Density

7 = 128Mb

9 = 512Mb

LPDDR 0 Density

0 = No Die

Boot Structure

U = Top ADMUX

Product Version

3 = 65nm technology multilevel interface, 70ns Flash; LPDDR

Package

ZE = 133-ball VFBGA, 8mm x 8mm, 0.5mm pitch

Temperature Range

6 = –40 to 85°C

Option

E = RoHS compliant package, standard packing
F = RoHS compliant package, tape and reel packing

Notes: 1. Devices are shipped from the factory with the memory content bits erased to 1. For a list of available options (speed, package, etc.), for daisy chain ordering information, or for further information on any aspect of this device, contact the nearest Micron sales office.

Revision History

Rev. D 09/13

- To Production status

Rev. C 09/12

- Updated clock rate (LPDDR Features)

Rev. B 04/12

- Updated packing options

Rev. A 07/11

- Initial release

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