LTC2123, LTC2122
14-Bit, 250Msps to 170Msps Dual ADCs with JESD204B Outputs

DESCRIPTION

Demonstration circuit 1974 supports the LTC®2123 14-bit dual ADC family with JESD204B compliant CML outputs. It was specially designed for applications that require single-ended AC coupled inputs. The DC1974 supports the LTC2123 and LTC2122 with sample rates from 250Msps to 170Msps.

The specific ADC characteristics are listed in the DC1974 Variants section. The circuitry on the analog inputs is optimized for analog input frequencies from 5MHz to 400MHz.

Refer to the data sheet for proper input networks for different input frequencies.

Design files for this circuit board are available at http://www.linear.com/demo/DC1974

DC1974 VARIANTS

DC1974 VARIANTS	ADC PART NUMBER	RESOLUTION (Bit)	MAXIMUM SAMPLE RATE (Msps)	INPUT FREQUENCY (MHz)
1974A-B	LTC2123	14	250	5 to 400
1974A-C	LTC2122	14	170	5 to 400

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
ADC Supply Voltage	This Supply Must Provide Up to 700mA	4		6	V
Analog Input Range		1.35		1.5	V_{PP}
Sampling Frequency (Device Clock Frequency)	Depending on ADC (1X CLK Mode)	10		250	MHz
Device Clock Level (Single-Ended at J3)	Minimum Logic Levels (DEV_{CLK}+ Tied to GND)	0			V
	Maximum Logic Levels (DEV_{CLK}+ Tied to GND)			3.6	V
Device Clock Level (Differential Signal Across J3 and J4)	Minimum Logic Levels (DEV_{CLK}+ Not Tied to GND, 1.2V Common Mode)	0.2			V
Digital Inputs (ADC_SYS_REF_N, ADC_SYS_REF_P, SYNC_N, SYNC_P)	Differential Input Voltage	0.2		1.8	V
	Common Mode Input Range	1.1	1.2	1.5	V

QUICK START PROCEDURE

Demonstration circuit 1974 is easy to set up to evaluate the performance of the LTC2123 A/D converter family. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

SETUP

The DC1974 evaluation system uses standard, off the shelf FPGA evaluation boards for data capture and communication with the host computer. Follow the instructions in Appendix A for the Xilinx KC705 based system. Verilog code may be downloaded from the respective ADC landing page. www.linear.com/LTC2123

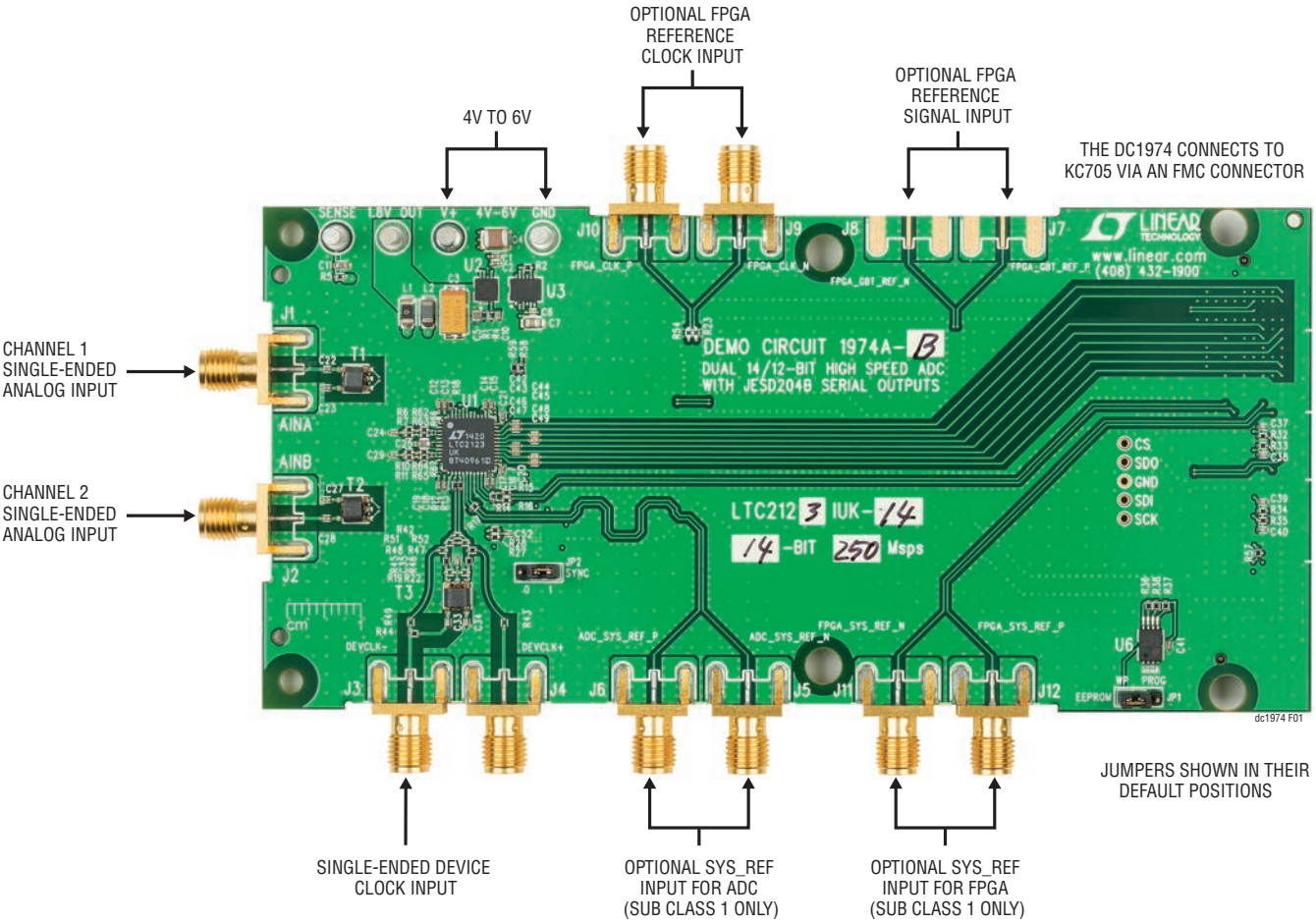


Figure 1. DC1974 Setup

HARDWARE SETUP

SMAs

J1: AINA – Analog input for channel A – Apply a signal to J1 from a 50Ω driver. Filters are required for data sheet performance.

J2: AINB – Analog input for channel B – Apply a signal to J2 from a 50Ω driver. Filters are required for data sheet performance.

J3: DEV_{CLK}– – Encode clock input for single-ended clocks – By default the DC1974 is defined to accept a single-ended clock signal on J3. It can be modified to accept a differential clock signal through J3 and J4. Some component changes are required, see the encode clock section for more information.

J4: DEV_{CLK}+ – Encode clock input for differential signals – By default the DC1974 is defined to accept a single-ended clock signal on J3. It can be modified to accept a differential clock signal through J3 and J4. Some component changes are required, see the encode clock section for more information.

J5 and J6: ADC_SYS_REF – JESD204B Subclass 1 only – When testing the ADC in subclass 1 operation a SYS_REF input is required to synchronize the ADC and FPGA. Apply a SYS_REF signal to this input from a SYS_REF driver board. This input drives the SYS_REF of the ADC.

J11 and J12: FPGA_SYS_REF – JESD204B Subclass 1 only – When testing the ADC in subclass 1 operation a SYS_REF input is required to synchronize the ADC and FPGA. Apply a SYS_REF signal to this input from a SYS_REF driver board. This input drives the SYS_REF of the FPGA.

J7 and J8: FPGA_GBT_REF – This is an optional reference port for the FPGA. It is used for testing purposes only. In the default configuration these SMAs are not used.

J9 and J10: FPGA_CLK – This is an optional clock input port for the FPGA. It is used for testing purposes only. In the default configuration these SMAs are not used.

TURRETS

V+: Positive supply voltage for the ADC and digital logic – This voltage feeds a regulator that supplies the proper voltages for the ADC and buffers. The voltage range for this turret is 4V to 6V. The supply should be able to deliver 700mA of current.

SENSE: Optional reference voltage – This pin is connected directly to the SENSE pin of the ADC. Connecting SENSE to VDD selects the internal reference and a ±0.66V input range. The same input voltage range can be achieved by applying an external 1.25V reference to SENSE. If no external voltage is supplied this pin will be pulled up to VDD through a 1k pull-up resistor.

1.8V OUT: Optional 1.8V turret – This pin is connected directly to the VDD pin of the ADC. It requires a supply that can deliver up to 500mA. Driving this pin will shutdown the on board regulator. It can also be a test point to measure the voltage at the output of the regulators.

GND: Ground Connection – This demo board only has a single ground plane. This turret should be tied to the GND terminal of the power supply being used.

JUMPERS:

JP1 EEPROM: EEPROM write protect. For factory use only. Should be left in the enable (PROG) position.

JP2 SYNC: This jumper is provided to manually force the SYNC~ signal of the ADC to a known value. By default, the resistors connecting this jumper are removed. If R20 and R21 are installed the SYNC jumper can be used to force SYNC~ high or low depending on the position of the jumper. Position 0 is for low and 1 is for high.

APPLYING POWER AND SIGNALS TO THE DC1974 DEMONSTRATION CIRCUIT

If a Kintex 7 FPGA board is used to acquire data from the DC1974, the Kintex 7 FPGA board must FIRST be powered BEFORE applying 4V to 6V across the pins marked "V+" and "GND" on the DC1974. For more information about the Kintex 7 board, please see the demo manual at www.xilinx.com. The DC1974 requires at least 4V for proper operation. Regulators on the board produce the voltages required for the ADC and the required logic devices. The DC1974 requires up to 700mA. The DC1974 should not be removed or connected to the Kintex 7 FPGA board while power is applied.

The DC2159 should also be connected to the Kintex 7 board and the supplied mini USB cable should be connected to the DC2159. The Kintex 7 board should be powered on BEFORE the mini USB connector is connected to the DC2159. See Figure 5 in Appendix A.

ANALOG INPUT NETWORK

Apply the analog input signal of interest to the SMA connector on the DC1974 board marked J1 or J2. In the default setup, the DC1974 has a single SMA input that is meant to be driven with a 50Ω source. The DC1974 is populated with an input network that has 50Ω characteristic impedance over a wide frequency range. This can be modified to produce different frequency responses as needed. Although the input of the DC1974 is single-ended, there is a transformer on the board that translates the single-ended signal to a differential signal to drive the ADC.

In almost all cases, off board filters with good return loss will be required on the analog input of the DC1974 to produce data sheet SNR.

The off board filter should be located close to the input of the demo board to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to make the filter look more like 50Ω to obtain low distortion.

ENCODE CLOCK

Apply an encode clock to the SMA connector on the DC1974 marked J3. By default, the DC1974 is configured to have a single-ended clock input. Although the clock input of the DC1974 is single-ended, there is a transformer on the board that translates the single-ended signal to a differential signal to drive the ADC.

For the best noise performance, the encode input must be driven with a very low jitter signal generator source. The amplitude should be as large as possible up to $2V_{P-P}$ or 10dBm.

The DC1974 is designed to accept single-ended signals by default. To modify the DC1974 to accept a differential signal, remove C33, R44, R45 and R46. Populate R49, R43, R48 and R47 with 0Ω resistors. Drive the demo board with a differential signal on J3 and J4. These SMAs are positioned 0.5" apart to accommodate LTC differential clock boards.

SOFTWARE

The DC1974 is controlled by the PScope™ System Software provided or downloaded from the Linear Technology website at http://www.linear.com/software/. If a Kintex 7 FPGA board and DC2159 were provided, follow the demo manual of these boards for proper setup.

The Kintex 7 FPGA board will act as the data collection board and the DC2159 is used to connect the FPGA to the computer. These boards both are designed to work seamlessly with PScope, Linear Technology's data collection software.

To start the data collection software and if "PScope.exe" is installed (by default) at \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1974 is properly connected to the Kintex 7 FPGA board and the DC2159, PScope should automatically detect the DC1974 and configure itself accordingly. If necessary the procedure below explains how to manually configure PScope.

Under the "Configure" menu, go to "ADC Configuration..." Check the "Config Manually" box and use the following configuration options, shown in Figure 2:

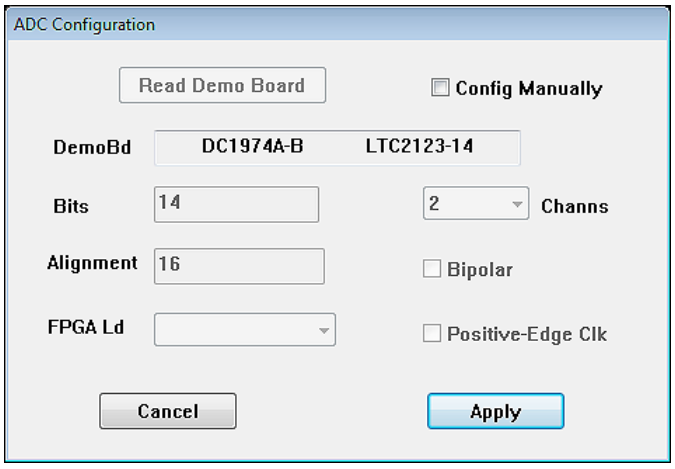


Figure 2: ADC Configuration

Manual Configuration settings:

Bits: 14

Alignment: 16

Channs: 2

Bipolar: Unchecked

Positive-Edge Clk: Unchecked

If everything is hooked up properly, powered and a suitable encode clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the KC705 guide and in the online help available within the PScope program itself.

NOTE: If a PRBS error occurs hit connect again. This is a bug in the first version of the software.

SERIAL PROGRAMMING

PScope has the ability to program the DC1974 board serially through the DC2159. There are several options available for the LTC2123 family that are only available through serial programming. PScope allows all of these features to be tested.

These options are available by first clicking on the "Set Demo Bd Options" icon on the PScope toolbar (Figure 3).

This will bring up the menu shown in Figure 4.

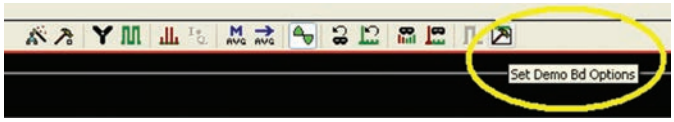


Figure 3: PScope Toolbar

SOFTWARE

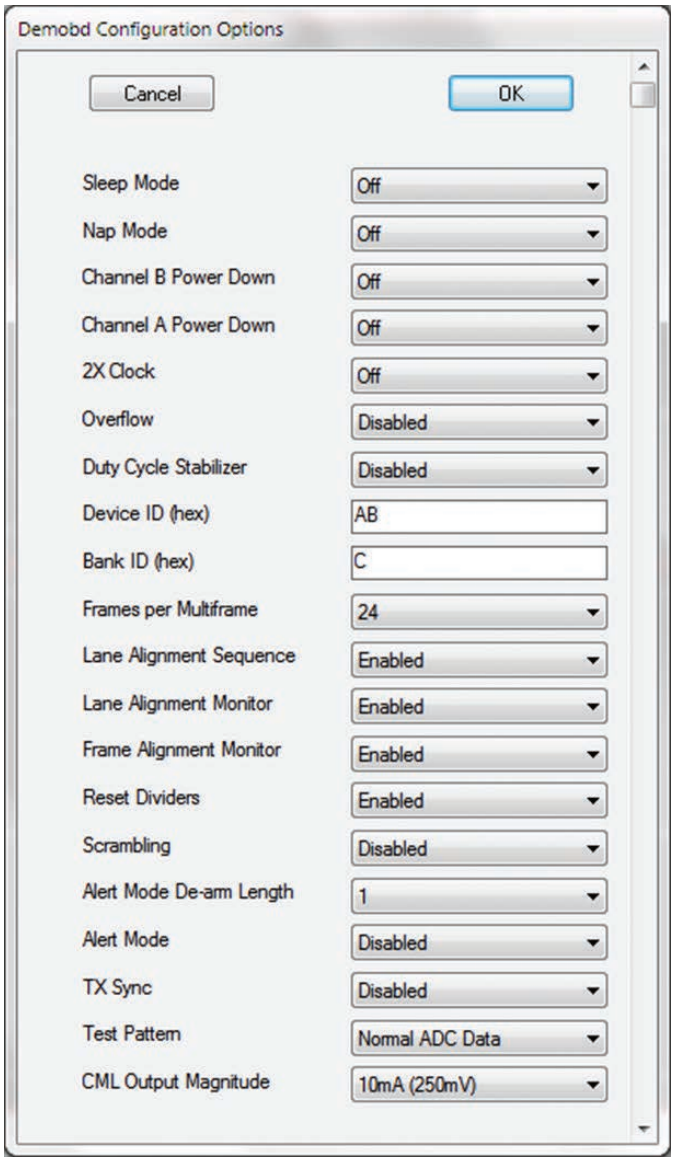


Figure 4: Demo Bd Configuration Options

This menu allows any of the options available for the LTC2123 to be programmed serially. The LTC2123 family has the following options:

Sleep Mode – Selects between normal operation and sleep mode.

- Off (Default) – Entire ADC is powered and active.
- On – The entire ADC is powered down.

Nap Mode – Selects between normal operation and nap mode.

- Off (Default) – Entire ADC is powered and active.
- On – The entire ADC is put into nap mode.

Channel B Power Down – Selects between normal operation and powering down channel B.

- Off (Default) – Normal operation.
- On – Channel B is powered down.

Channel A Power Down – Selects between normal operation and powering down channel B.

- Off (Default) – Normal operation.
- On – Channel A is powered down.

2x Clock – Selects between a sample rate equal to the device clock, or device clock twice the sample rate.

- Off (Default) – DEV_{CLK} is equal to the sample rate.
- On – DEV_{CLK} is twice the sample rate.

Overflow – Enables or disables the overflow bit in the output data.

- Disabled (Default) – Over flow bit is disabled.
- Enabled – Overflow bit is enabled.

Duty Cycle Stabilizer – Enables or disables Duty Cycle Stabilizer.

- Stabilizer off (Default) – Duty Cycle Stabilizer Disabled.
- Stabilizer on – Duty Cycle Stabilizer Enabled.

Device ID – Sets the device ID defined in JESD204B 8.3. Default is 00000000, but can be set to whatever the user chooses.

Bank ID – Sets the bank ID defined in JESD204B 8.3. Default is 0000, but can be set to whatever the user chooses.

Frames per MultiFrame – Selects number of frames in each multiframe as defined in JESD204B 5.3.3.5. The user selects the number of desired frames per multiframe and PScope configures the ADC accordingly. Valid values for number of frames per multiframe are 9 to 32.

SOFTWARE

Lane Alignment Sequence – Enables or disables the lane alignment sequence.

- Enabled (Default) – Lane alignment sequence is enabled.
- Disabled - Lane alignment sequence is disabled.

Lane Alignment Monitor – Enables or disables the lane monitor sequence.

- Enabled (Default) – Lane alignment monitor sequence is enabled.
- Disabled – Lane alignment monitor sequence is disabled.

Frame Alignment Monitor – Enables or disables the Frame monitor sequence

- Enabled (Default) – Frame alignment monitor sequence is enabled.
- Disabled – Frame alignment monitor sequence is disabled.

Reset Dividers (Subclass 1 or 2 Only) – Enables or disables SYSREF reset of dividers.

- Enabled (Default) – Subclass 1 – Enables the SYSREF reset of dividers. Subclass 2 – Enables SYNC~ reset of dividers.
- Disabled – Subclass 1 – Disables the SYSREF reset of dividers. Subclass 2 – Disables SYNC~ reset of dividers.

Scrambling – Enables or disables the scrambling of the output data.

- Disabled (Default) – Scrambling is disabled.
- Enabled – Scrambling is enabled.

Alert Mode De-arm Length (Subclass 1 Only) – Selects the de-arming length in multiframe periods to trigger the alert in subclass 1. Valid values are 1 to 8.

Alert Mode (Subclass 1 Only) – Enables or disables the alert mode.

- Disabled (Default) – Alert mode is disabled.
- Enabled – Alert mode is enabled.

TX Sync – Enables or disables Transmitter induced synchronization.

- Disabled (Default) – Transmitter induced synchronization is disabled.
- Enabled - Transmitter induced synchronization is enabled.

Test Pattern – Selects the data presented at the output of the ADC

Normal ADC Data (Default) – The data that is sampled by the input of the ADC

K28.5 Pattern – A repeating SYNC comma.

K28.7 Pattern – 1111100000.

D21.5 Pattern – 1010101010.

PRBS15 Pattern – A Pseudorandom bit sequence pattern described by $1 + x^{14} + x^{15}$.

Lane Alignment Sequence – The lane alignment sequence is transmitted according to tables 3a to 3h from the datasheet.

Test Samples Sequence – The test samples are repeatedly transmitted according to tables 4a to 4b from the datasheet.

Modified RPAT Pattern – A modified RPAT pattern as described in IEEE Std. 802.3-2008 Annex 48A.

CML Output Magnitude – Magnitude of the CML output signals.

Value selections are:

10mA (250mV) Default

12mA (300mV)

14mA (350mV)

16mA (400mV)

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC1974 demo board.

APPENDIX A

XILINX KC705 BASED EVALUATION SYSTEM

The demonstration system for the LTC2123 family consists of the DC1974, a Xilinx KC705 FPGA evaluation board, a DC2159 USB communication board and a host PC running the PScope software.

Complete systems that ship from Linear Technology will have the KC705 board configured to automatically load the default subclass 0 FPGA image from the onboard configuration EEPROM. The procedure for bringing up the system is as follows:

1) If the boards were obtained separately, assemble them as shown in Figure 5 (FMC connectors are fragile, make sure they are properly aligned before seating.)
2) Connect power supply to the KC705 board and turn on the power switch. If the assembled system was obtained from Linear Technology, the subclass 0 image will load automatically from the onboard configuration memory.
3) Boards not obtained from Linear Technology will need to be configured as described in the Alternate FPGA Configuration section.
4) Apply power, encode clock and analog input signals to the DC1974 board.
5) Verify that PScope software is installed. Connect DC2159 to the host PC with a USB-mini cable. Driver installation will start automatically and PScope will recognize the DC1974 when installation finishes.

NOTE: Power must be applied to the KC705 board when the USB cable is connected or the driver installation will not complete properly.

ALTERNATE FPGA CONFIGURATION

KC705 boards not obtained from Linear Technology will need to be configured via JTAG. FPGA images are located in the PScope installation directory in the FPGA_images folder. Connect a USB micro cable to the JTAG USB connector on the KC705 board and use a Xilinx tool such as Impact to load the Subclass 0, 2 lane bitfile. Once the FPGA is configured, remove the USB cable and exit the software. (The onboard JTAG adapter and the DC2159 USB communication board use the same USB controller and they may interfere with one another.)

APPENDIX A

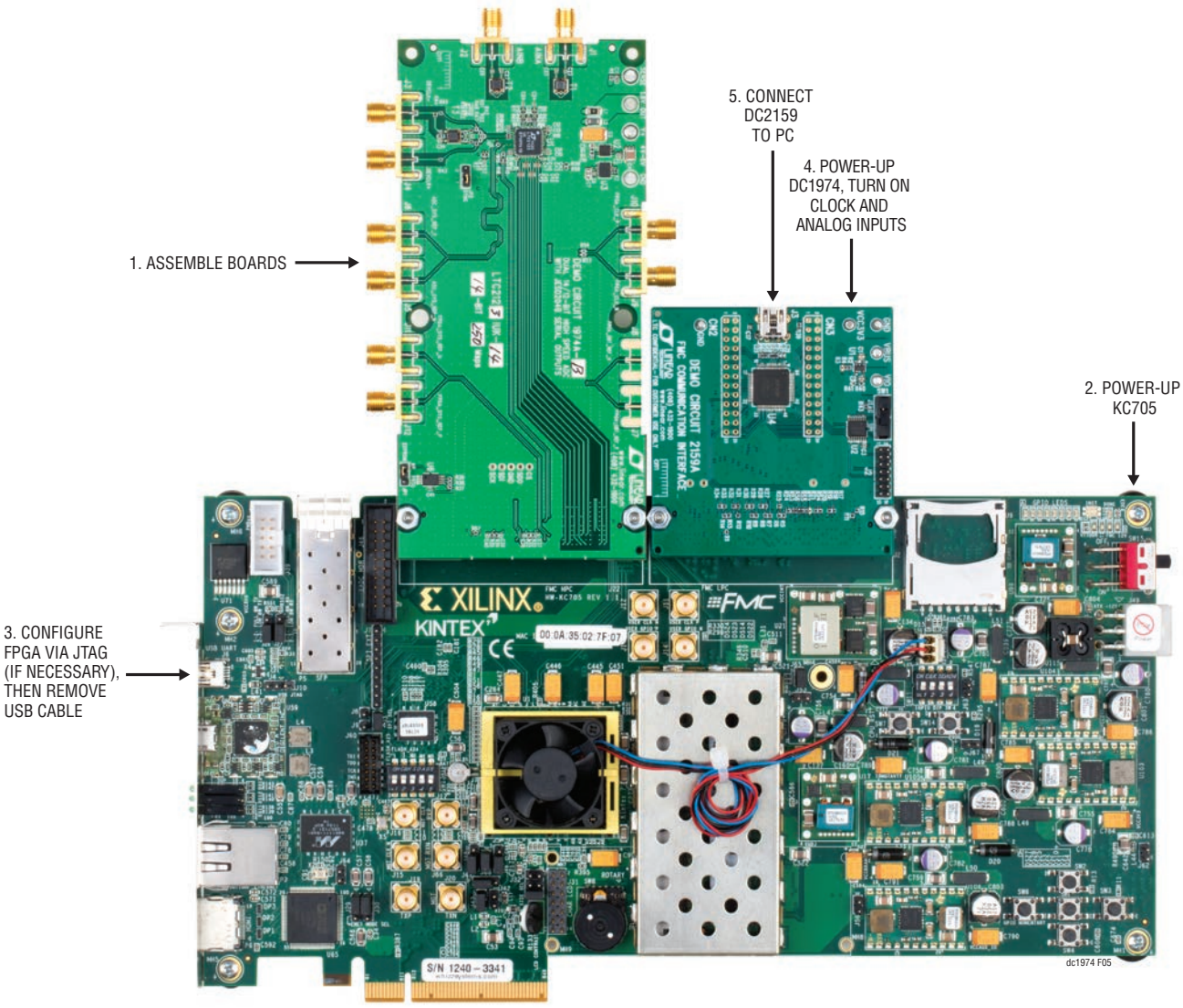


Figure 5. KC705 Based Demonstration System

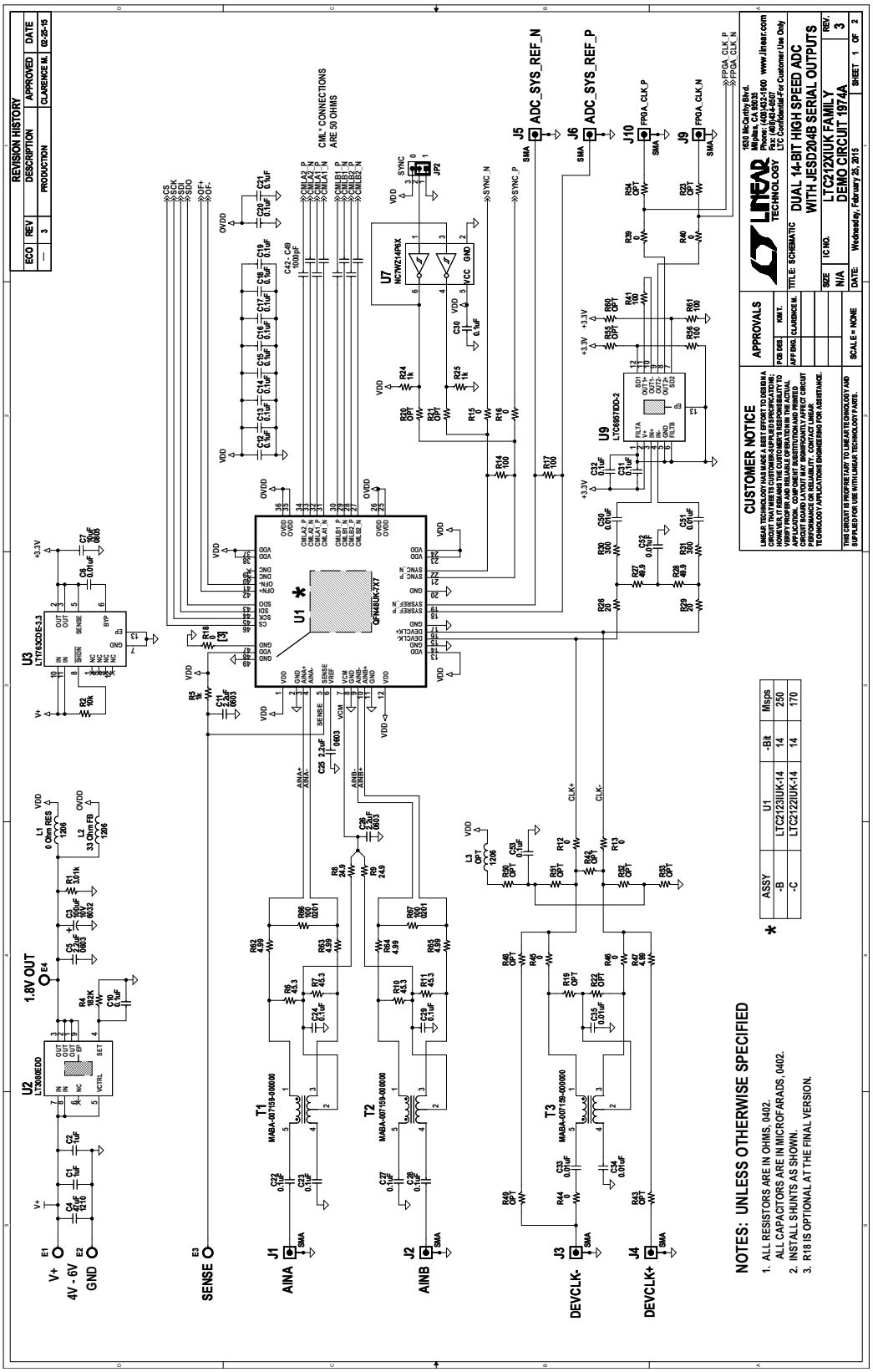
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART #
Required Circuit Components				
1	2	C1, C2	CAP., X5R, 1µF, 10V, 10%, 0402	AVX, 0402ZD105KAT2A
2	1	C3	CAP., TANT, 100µF, 10V, 10%, 6032	AVX, TAJW107K010RNJ
3	1	C4	CAP., X7R, 47µF,10V, 10%, 1210	MURATA, GRM32ER71A476KE15L
4	4	C5, C11, C25, C26	CAP., X5R, 2.2µF, 10V, 20%, 0603	AVX, 0603ZD225MAT2A
5	7	C6, C33-C35, C50-C52	CAP., X7R, 0.01µF, 16V, 10%, 0402	AVX, 0402YC103KAT2A
6	1	C7	CAP., X5R, 10µF, 6.3V, 20%, 0805	AVX, 08056D106MAT2A
7	22	C10, C12-C24, C27-C32, C41, C53	CAP., X5R, 0.1µF, 10V, 10%, 0402	AVX, 0402ZD104KAT2A
8	4	C37, C38, C39, C40	CAP., C0G, 47pF, 16V, 10%, 0402	AVX, 0402YA470KAT2A
9	8	C42-C49	CAP., X7R, 1000pF, 50V, 10%, 0402	AVX, 04025C102KAT2A
10	4	E1, E2, E3, E4	TESTPOINT, TURRET, 0.094"	MILL-MAX, 2501-2-00-80-00-00-07-0
11	2	JP1, JP2	HEADER, HD1X3-079	SULLINS, NRPN031PAEN-RC
12	10	J1-J6, J9-J12	CONN., SMA 50Ω, EDGE-LAUNCH	EF JOHNSON, 142-0701-851
13	0	J7, J8 (OPT)	CONN., SMA 50Ω, EDGE-LAUNCH	EF JOHNSON, 142-0701-851
14	1	J13	CONN., BGA 40X10	SAMTEC, SEAM-40-02.0-S-10-2-A-K-TR
15	1	L1	RES., CHIP, 0Ω, 1206	VISHAY, CRCW12060000Z0EA
16	1	L2	IND., FERRITE BEAD, 33Ω, 1206	MURATA, BLM31PG330SN1L
17	0	L3	RES., 1206	OPT
18	2	R1,R59	RES., CHIP, 3.01k, 1/16W, 1%, 0402	VISHAY, CRCW04023K01FKED
19	1	R2	RES., CHIP, 10k, 1/16W, 1%, 0402	VISHAY, CRCW040210K0FKED
20	1	R4	RES., CHIP, 182k, 1/16W, 1%, 0402	VISHAY, CRCW0402182KFKED
21	4	R5, R24, R25, R58	RES., CHIP, 1k, 1/16W, 1%, 0402	NIC, NRC04F1001TRF
22	10	R6-R11, R32-R35	RES., CHIP, 24.9Ω, 1/16W, 1%, 0402	VISHAY, CRCW040224R9FKED
23	11	R12, R13, R15, R16, R18, R39, R40, R44, R45, R46, R57	RES., CHIP, 0Ω, 1/16W, 0402	NIC, NRC04Z0TRF
24	5	R14, R17, R41, R56, R61	RES., CHIP, 100Ω, 1/16W, 1%, 0402	NIC, NRC04F1000TRF
25	0	R19-R23, R42, R43, R48-R53, R54, R55, R60	RES., 0402	OPT
26	2	R26, R29	RES., CHIP, 20Ω, 1/16W, 1%, 0402	NIC, NRC04F20R0TRF
27	2	R27, R28	RES., CHIP, 49.9Ω, 1/16W, 1%, 0402	VISHAY, CRCW040249R9FKED
28	2	R30, R31	RES., CHIP, 300Ω, 1/16W, 1%, 0402	NIC, NRC04F3000TRF
29	3	R36, R37,R38	RES., CHIP, 4.99k, 1/16W, 1%, 0402	VISHAY, CRCW04024K99FKED
30	5	R47, R62,R63,R64,R65	RES., CHIP, 4.99Ω, 1/16W, 1%, 0402	NIC, NRC04F4R99TRF
31	2	R66, R67	RES., CHIP, 100Ω, 1/20W, 1%, 0201	NIC, NRC02F1000TRF
32	3	T1, T2, T3	XFMR., MABA-007159-000000	M/A-COM, MABA-007159-000000
33	1	U2	I.C., LT3080EDD#PBF, DFN 3X3	LINEAR TECH., LT3080EDD#PBF
34	1	U3	I.C., LT1763CDE-3.3#PBF, DFN12DE-4X3	LINEAR TECH., LT1763CDE-3.3#PBF
35	1	U6	I.C. EEPROM 32KBIT 400KHz, TSSOP8	MICROCHIP, 24LC32A-I/ST

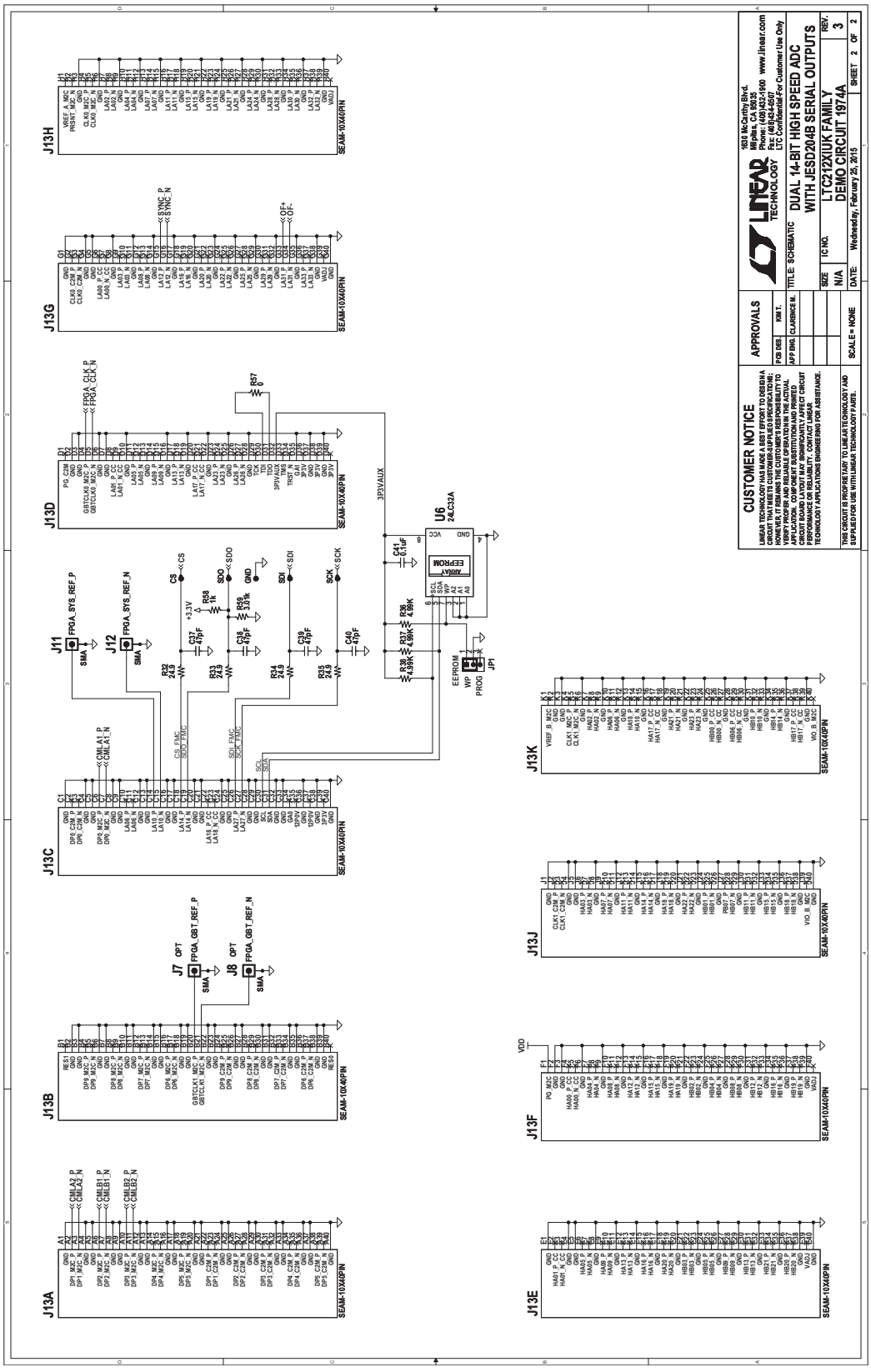
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART #
36	1	U7	I.C., NC7WZ14P6X, SC70-6	FAIRCHILD SEMI., NC7WZ14P6X
37	1	U9	I.C., LTC6957IDD-2#PBF, DFN12DD-3X3	LINEAR TECH., LTC6957IDD-2#PBF
38	1	SHUNTS FOR JP1 & JP2	SHUNT, 0.079" CENTER	SAMTEC, 2SN-BK-G
39	0	MH1, MH2	SCREW, M3 THREAD, #4-40x5/8"	KEYSTONE, 29316 (DO NOT INSTALL)
40	0	MH1, MH2	STAND-OFF, ALUM., M3 THREAD, 5.0 HEX, #4-40X1"	KEYSTONE, 24438 (DO NOT INSTALL)
41	2	STENCILS	STENCILS (TOP & BOTTOM)	STENCIL DC1974A-3
DC1974A-B Required Circuit Components				
1	1	DC1974A	GENERAL BOM	
2	1	U1	I.C., 14-BIT, 250Msps, QFN48UK-7X7	LINEAR TECH., LTC2123IUK#PBF
DC1974A-C Required Circuit Components				
1	1	DC1974A	GENERAL BOM	
2	1	U1	I.C., 14-BIT, 170Msps, QFN48UK-7X7	LINEAR TECH., LTC2122IUK#PBF

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



DEMONSTRATION BOARD IMPORTANT NOTICE

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If this evaluation kit does not meet the specifications recited in the DEMO BOARD manual the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY THE SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THIS INDEMNITY, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

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Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged**.

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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