EVALUATION KIT AVAILABLE

MAX77178/MAX77179

High-Bandwidth LTE/WCDMA PA Power Management ICs in a 1.75mm x 1.4mm, 0.4mm Pitch WLP

General Description

The MAX77178/MAX77179 step-down converters are optimized for powering the power amplifier (PA) in multimode/multiband handsets for 3G/4G applications such as LTE, WCDMA, as well as other RF PA applications such as Wi-Fi® and WiMAX®.

The 2.5V to 5.5V input supply range supports both current and future battery chemistries. The MAX77179 uses an analog input driven by an external DAC to control the output voltage linearly for continuous PA power adjustment. The output voltage range (0.5V to V_{IN}) supports operation with a wide variety of PAs. The MAX77178 uses a 2-bit GPIO interface with four selectable output voltage options to control the output voltage supply for PA power adjustment.

Fast switching frequency (8MHz, typ) allows the use of low value inductor and small ceramic output capacitors while maintaining low-ripple voltage. Efficiency is enhanced at light loads by switching to skip mode where the converter switches only as needed to service the load. Adaptive smart FET scaling further improves efficiency under all operating conditions.

Other features include overcurrent and overtemperature protection, and a very low-current (0.1µA, typ) shutdown mode.

WiMAX is a registered certification mark and service mark of WiMAX Forum.

Wi-Fi is a registered certification mark of Wi-Fi Alliance Corporation.

Features

- **Meet 3G/4G Timing and RF Spectrum Mask Requirements**
  - ✧ **20µs (typ) Settling Time for 0.5V to 3.4V Output Voltage Change**
  - ✧ **30µs (typ) Settling from Enable to 95% Output Voltage Regulation**
- **Four Selectable Output Voltages with Logic Inputs (MAX77178 Only)**
- **Analog Controlled Output Voltage Settings from 0.5V to V_{IN} (MAX77179 Only)**
- **1A Peak Output Current Capability**
- **±3% Output Voltage Accuracy**
- **Allows Use of Small (1210) 0.47µH Inductor**
- **100% Duty-Cycle Operation**
- **Simple Logic On/Off Controls**
- **< 1µA Shutdown Supply Current**
- **2.5V to 5.5V Supply Voltage Range**
- **Overcurrent and Overtemperature Protection**

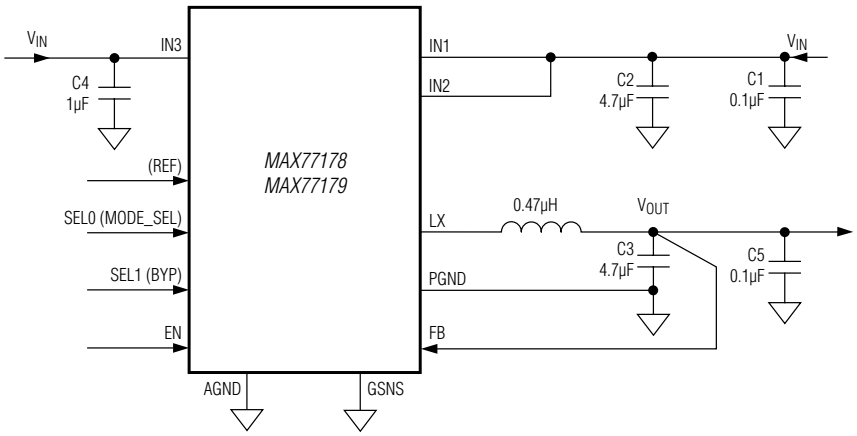
Applications

LTE, WCDMA Cell Phones/Smartphones/Tablets/Data Cards

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX77178.related.

Typical Operating Circuit



NOTE: ( ) FOR MAX77179

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6405; Rev 0; 3/13

ABSOLUTE MAXIMUM RATINGS

IN1, IN2 to PGND ..... -0.3V to +6.0V
IN3 to AGND ..... -0.3V to +6.0V
SEL0, SEL1, EN, FB to AGND (MAX77179) ..... -0.3V to (V_{IN3} + 0.3)
MODE_SEL, BYP, REF, EN, FB to AGND (MAX77178) ..... -0.3V to (V_{IN3} + 0.3)
REF to GSNS ..... -0.3V to (V_{IN3} + 0.3)
AGND to GSNS ..... -0.3V to +0.3V
AGND to PGND ..... -0.3V to +0.3V
I_{LX} Current ..... 1250mA_{RMS}
Continuous Power Dissipation (T_A = +70°C)
12-Bump, 1.75mm x 1.4mm WLP
(derate 13.7 mW/°C above +70°C) 1096mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 73°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Note 2: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board-level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN1} = V_{IN2} = V_{IN3} = 3.7V, V_{PGND} = V_{AGND} = 0V, L = 0.47µH, C_{OUT} = 4.7µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
IN1, IN2, IN3 Operating Voltage			2.5		5.5	V
IN1, IN2, IN3 Undervoltage Lockout (UVLO) Threshold	IN1, IN2, IN3 falling (enter power-down mode and disable the output)		2.10	2.20	2.30	V
IN1, IN2, IN3 UVLO Hysteresis				100		mV
IN1, IN2, IN3 Shutdown Supply Current	V_{EN} = V_{AGND} = 0V or $V_{IN\_}$ is below UVLO threshold	T_A = +25°C		0.1	1	µA
		T_A = +85°C		0.1		
STEP-DOWN DC-DC CONVERTER						
IN1, IN2, IN3 No-Load Supply Current	V_{OUT} = 0.5V, no load, skip mode operation			450		µA
	V_{OUT} = 0.5V, no load, PWM operation			3.5		mA
	V_{OUT} = 3V, no load, PWM operation			8		
Output Capacitance Required for Stability	V_{OUT} = 0.5V to V_{IN1}, I_{OUT} = 0A to 1A		0.1	0.47	10	µF
Output Inductance Required for Stability	V_{OUT} = 0.5V to V_{IN1}, I_{OUT} = 0A to 1A		0.22		1.0	µH
Startup Time from Shutdown	From V_{EN} = low to V_{EN} = high, V_{OUT} = 0.5V			30		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN2} = V_{IN3} = 3.7V, V_{PGND} = V_{AGND} = 0V, L = 0.47µH, C_{OUT} = 4.7µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Transition Time (MAX77179)	Rise time when V_{OUT} transitions from 0.5V to 3.4V, I_{OUT} = 1A, C_{OUT} = 4.7µF, L = 0.47µH			0.33		V/µs
Output Transition Time (MAX77178)	Rise time when V_{OUT} transitions from 0.8V to 3.4V, I_{OUT} = 500mA, C_{OUT} = 4.7µF, L = 0.47µH			0.33		V/µs
Maximum Output Current			1			A
High-Side Current-Limit Threshold			1.2		2.0	A
Low-Side Current-Limit Threshold			0.8		1.65	A
Low-Side Negative Current-Limit Threshold			0.7		1.8	A
Low-Side Zero-Cross Threshold				40		mA
LX High-Side On-Resistance	IN1/IN2 to LX, I_{LX} = -200mA	V_{OUT} > 1.6V, V_{MODE_SEL} = V_{IN3}		90	160	mΩ
		1V ≤ V_{OUT} ≤ 1.6V, V_{MODE_SEL} = V_{IN3}		135		
		V_{OUT} < 1V, V_{MODE_SEL} = V_{IN3}		192		
		V_{OUT} > 1.8V, V_{MODE_SEL} = V_{AGND}		135		
		V_{OUT} ≤ 1.8V, V_{MODE_SEL} = V_{AGND}		360		
LX Low-Side On-Resistance	LX to PGND, I_{LX} = -200mA	V_{OUT} > 1.6V, V_{MODE_SEL} = V_{IN3}		75	130	mΩ
		1V ≤ V_{OUT} ≤ 1.6V, V_{MODE_SEL} = V_{IN3}		110		
		V_{OUT} < 1V, V_{MODE_SEL} = V_{IN3}		150		
		V_{OUT} > 1.8V, V_{MODE_SEL} = V_{AGND}		110		
		V_{OUT} ≤ 1.8V, V_{MODE_SEL} = V_{AGND}		290		
LX Leakage Current	$V_{IN\_}$ = V_{LX} = 5.5V, V_{EN} = 0V	T_A = +25°C	-2.0	0.03	+2.0	µA
		T_A = +85°C		0.24		
Efficiency	V_{IN1} = 3.6V, V_{OUT} = 0.7V, I_{OUT} = 16mA			68		%
	V_{IN1} = 3.6V, V_{OUT} = 1.3V, I_{OUT} = 50mA			80		
	V_{IN1} = 3.6V, V_{OUT} = 2.2V, I_{OUT} = 300mA			89		
	V_{IN1} = 3.6V, V_{OUT} = 3.0V, I_{OUT} = 500mA			93		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN2} = V_{IN3} = 3.7V, V_{PGND} = V_{AGND} = 0V, L = 0.47µH, C_{OUT} = 4.7µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LX Rise Time				1		ns
Output-Voltage Line Regulation	V_{IN} = 2.5V to 5.5V, I_{OUT} = 100mA, V_{OUT} = 1.8V			1.3		%/V
Line Regulation Transient Response	V_{IN1}(DC) = 3.6V_{RMS}, V_{IN1}(AC) = 300mV_{P-P} ripple at 10Hz to 270kHz, I_{OUT} = 500mA, V_{OUT} = 3.0V			25		mV_{P-P}
Output-Voltage Load Regulation	I_{OUT} = 0 to 1A			-1.5		%/A
Load Regulation Transient Response	t_{RISE} = t_{FALL} = 1.5µs, I_{OUT} = 0.2A to 1A, V_{OUT} = 3.0V			25		mV_{P-P}
Operating Frequency	V_{OUT} = 1.8V, I_{OUT} = 0A, PWM		6	8	10	MHz
Automatic Bypass Mode Entry Threshold	V_{IN} - V_{OUT}, when the drop between V_{IN} and V_{OUT} becomes less than this threshold, high-side FET is turned on continuously			0.125		V
Automatic Bypass Mode Entry Hysteresis				40		mV
Automatic Bypass Mode Exit Debounce Time				5		µs
Minimum Duty Cycle	Skip mode			0		%
	PWM mode			10		
Maximum Duty Cycle					100	%
Output-Voltage Ripple	C_{OUT} = 4.7µF, ESR of C_{OUT} < 20mΩ, f_{SW} = 8MHz, I_{OUT} = 10mA to 1A, V_{OUT} = 1.8V, PWM mode			5		mV_{P-P}
	Skip mode, I_{OUT} = 0mA			45		
PROTECTION CIRCUITS						
Thermal Shutdown				160		°C
Thermal Shutdown Hysteresis				20		°C
CONTROL						
REF Input Voltage Range	MAX77179, analog control voltage		0		V_{IN3} - 0.3	V
REF to OUT Gain Accuracy	MAX77179, V_{REF} = 1V, gain = V_{OUT}/V_{REF}		-2.5		+2.5	%
REF to OUT Absolute Accuracy (MAX77179)	V_{REF} = 1V, I_{OUT} = 0	T_A = +25°C	-3		+3	%
		T_A = -40°C to +85°C	-3.5		+3.5	
Output Voltage Range (MAX77179)	Controlled by the REF input		0.5		V_{IN}	V
	V_{REF} = 0V, skip mode operation			0.1		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN2} = V_{IN3} = 3.7V, V_{PGND} = V_{AGND} = 0V, L = 0.47µH, C_{OUT} = 4.7µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Accuracy (MAX77178)	V_{SEL1} = 0, V_{SEL0} = 0, V_{OUT} = 2.9V	T_A = +25°C	-2		+2	%
		T_A = -40°C to +85°C		±3		
	V_{SEL1} = 0, V_{SEL0} = 1, V_{OUT} = 2.325V	T_A = +25°C	-2		+2	
		T_A = -40°C to +85°C		±3		
	V_{SEL1} = 1, V_{SEL0} = 1, V_{OUT} = 1.7V	T_A = +25°C	-2		+2	
		T_A = -40°C to +85°C		±3		
	V_{SEL1} = 1, V_{SEL0} = 0, V_{OUT} = 1.0V	T_A = +25°C	-2.5		+2.5	
		T_A = -40°C to +85°C		±3		
REF Input Current	MAX77179, V_{REF} = 1V	T_A = +25°C		0.1	1	µA
		T_A = +85°C		1		
REF Input Capacitance	MAX77179			5		pF
Analog Gain Setting Range	MAX77179 (Note 4)			2.5		V/V
Logic-Input High Voltage	$V_{IN\_}$ = 2.5V to 5.5V, $V_{SEL\_}$,V_{BYP}, V_{MODE_SEL}, V_{EN}		1.2			V
Logic-Input Low Voltage	$V_{IN\_}$ = 2.5V to 5.5V, $V_{SEL\_}$, V_{BYP}, V_{MODE_SEL}, V_{EN}				0.4	V
Logic-Input Pulldown Resistor	SEL0, SEL1, MODE_SEL, BYP			800		kΩ
Select Debounce Delay	$t_{EN\_DEBOUNCE}$, SEL0 or SEL1(MAX77178), BYP or MODE_SEL (MAX77179)			500		ns
Output Noise	Not production tested, 650MHz to 2.2GHz, 30kHz resolution bandwidth	V_{IN} = 3.6V, V_{OUT} = 3V; I_{OUT} = 200mA, 400mA, 600mA		-105		dBm/Hz

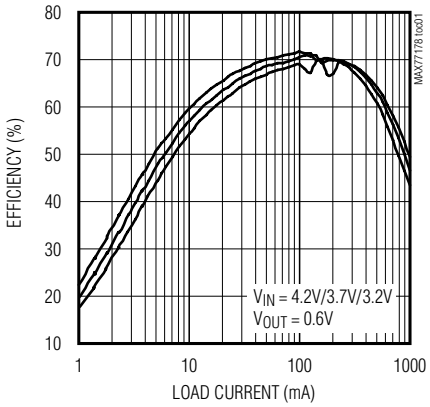
Note 3: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 4: Factory programmable parameter. Contact the factory for options.

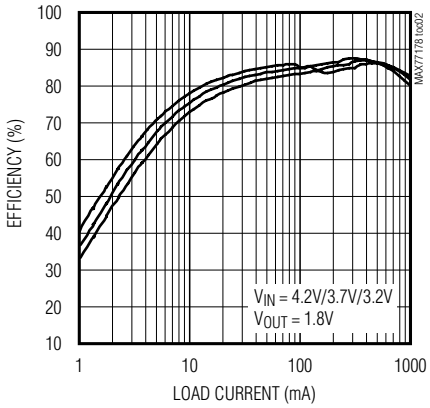
Typical Operating Characteristics

(*Typical Operating Circuits*, V_{IN} = 3.7V, I_{OUT} = 0.47µH, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)

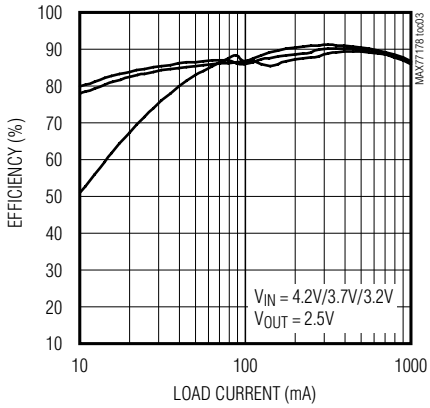
MAX77179
EFFICIENCY vs. LOAD CURRENT



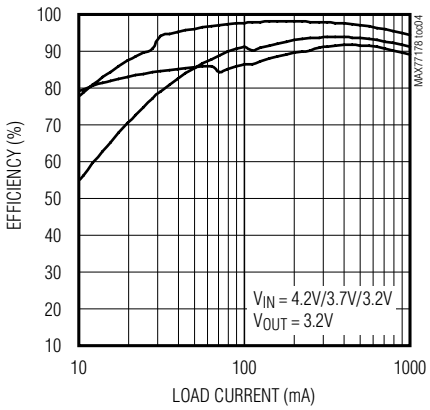
MAX77179
EFFICIENCY vs. LOAD CURRENT



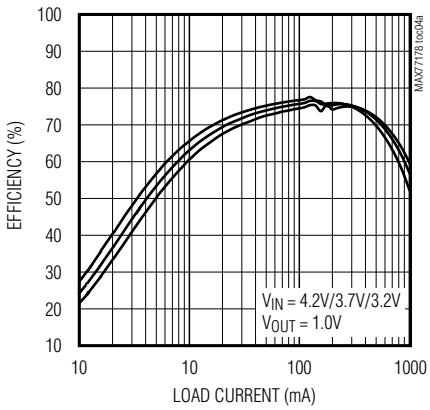
MAX77179
EFFICIENCY vs. LOAD CURRENT



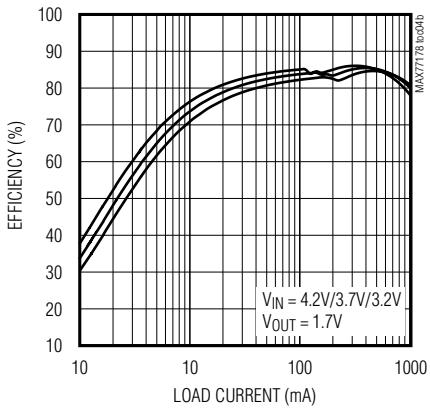
MAX77179
EFFICIENCY vs. LOAD CURRENT



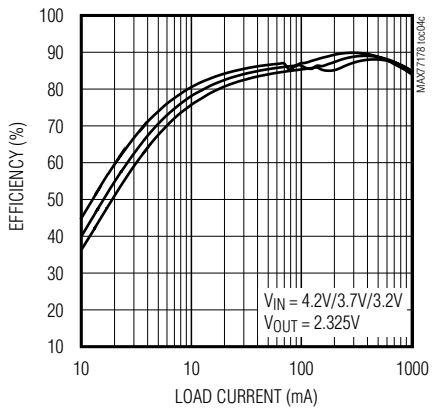
MAX77178
EFFICIENCY vs. LOAD CURRENT



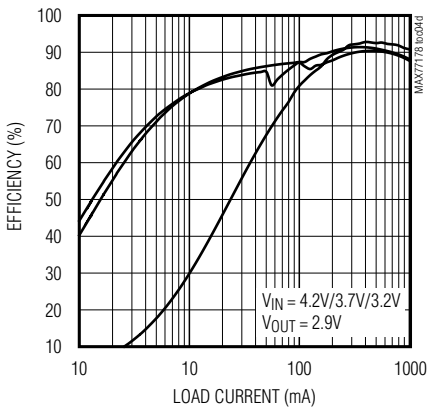
MAX77178
EFFICIENCY vs. LOAD CURRENT



MAX77178
EFFICIENCY vs. LOAD CURRENT



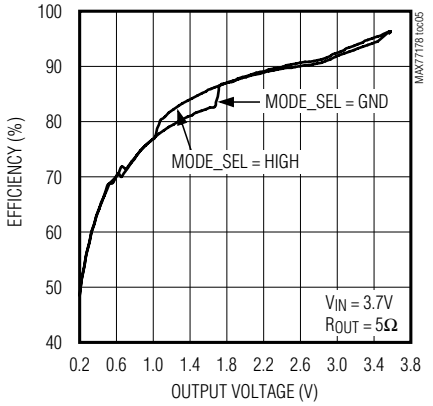
MAX77178
EFFICIENCY vs. LOAD CURRENT



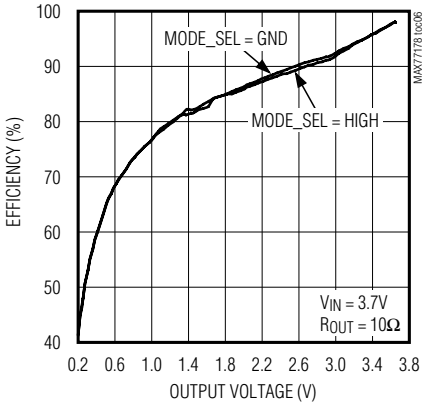
Typical Operating Characteristics (continued)

(*Typical Operating Circuits*, V_{IN} = 3.7V, I_{OUT} = 0.47µH, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)

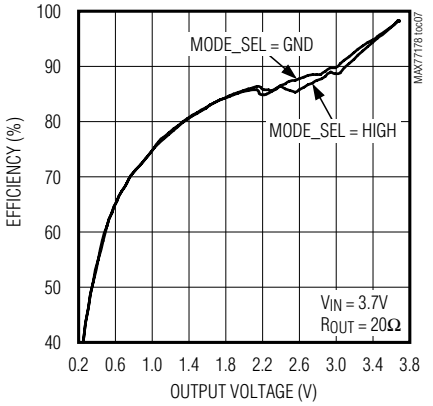
EFFICIENCY vs. OUTPUT VOLTAGE



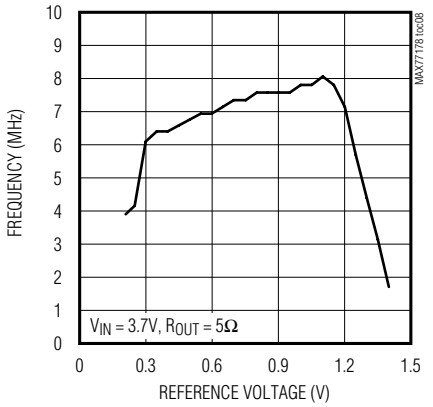
EFFICIENCY vs. OUTPUT VOLTAGE



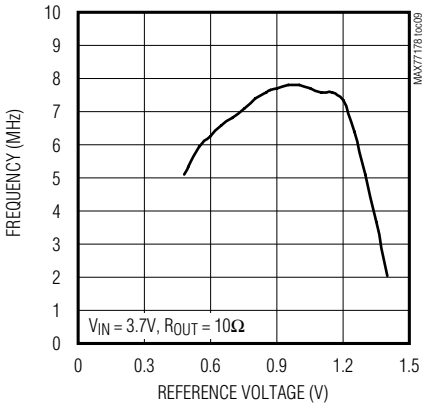
EFFICIENCY vs. OUTPUT VOLTAGE



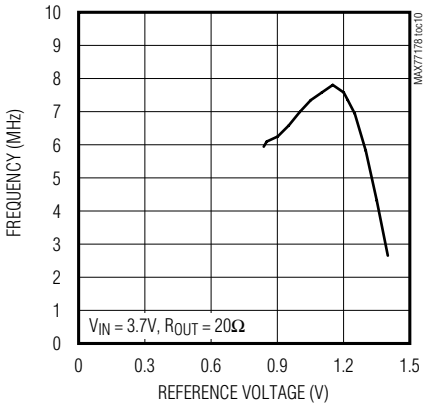
FREQUENCY vs. REFERENCE VOLTAGE



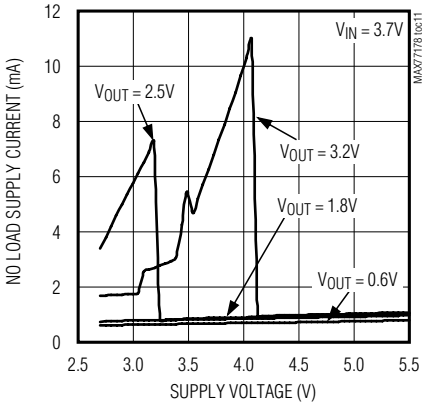
FREQUENCY vs. REFERENCE VOLTAGE



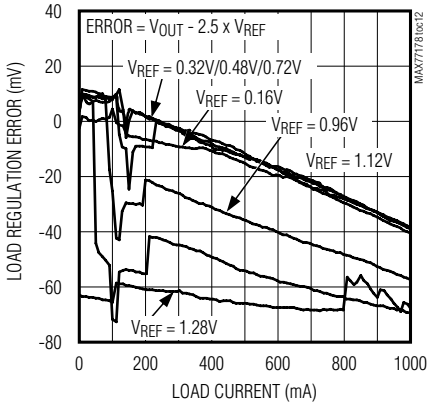
FREQUENCY vs. REFERENCE VOLTAGE



NO LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



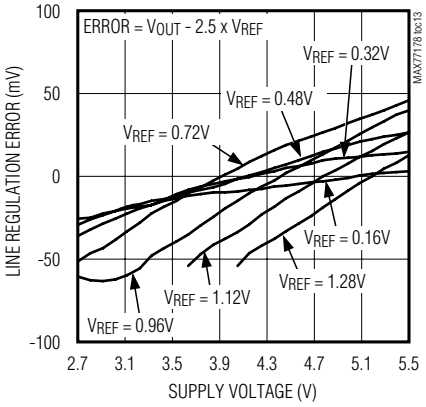
LOAD REGULATION ERROR vs. LOAD CURRENT



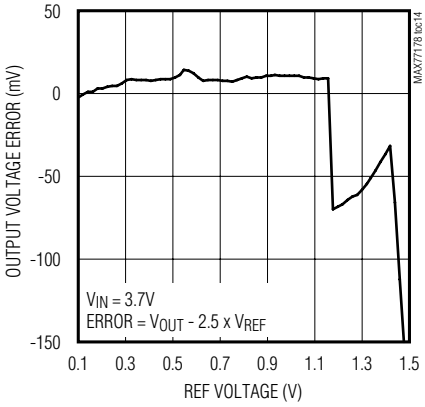
Typical Operating Characteristics (continued)

(*Typical Operating Circuits*, V_{IN} = 3.7V, I_{OUT} = 0.47µH, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)

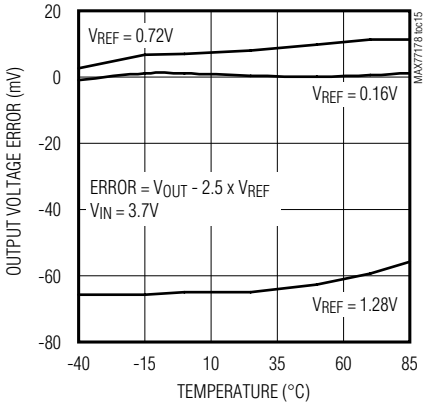
LINE REGULATION ERROR vs. SUPPLY VOLTAGE



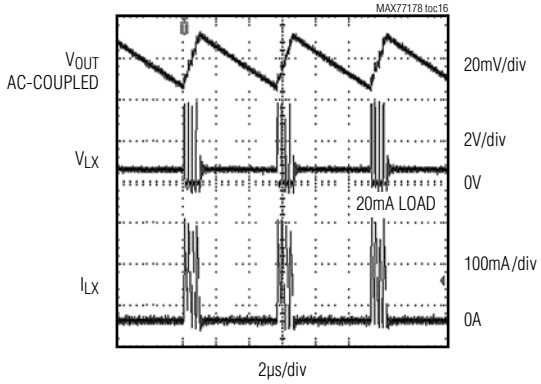
OUTPUT VOLTAGE ERROR vs. REF VOLTAGE



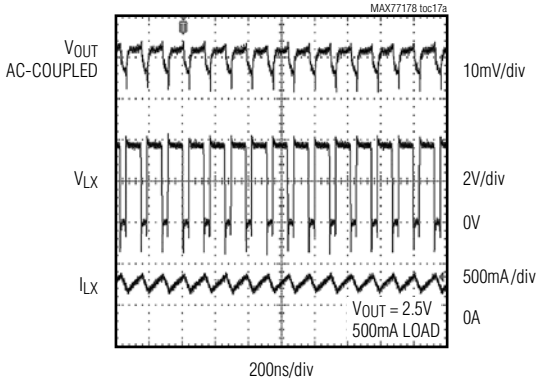
OUTPUT VOLTAGE ERROR vs. TEMPERATURE



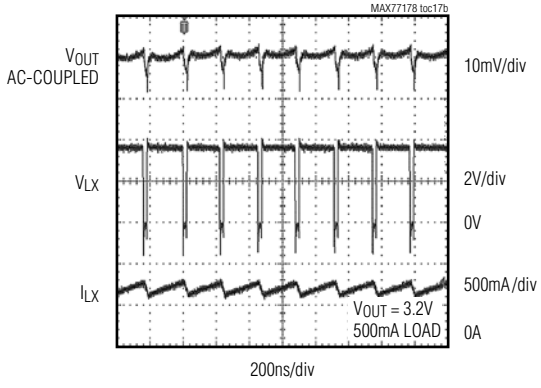
LIGHT LOAD SWITCHING WAVEFORM



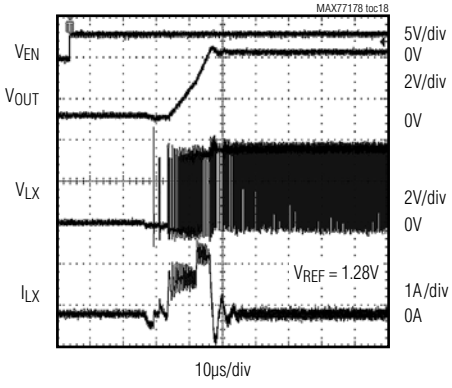
HEAVY LOAD SWITCHING WAVEFORM



HEAVY LOAD SWITCHING WAVEFORM



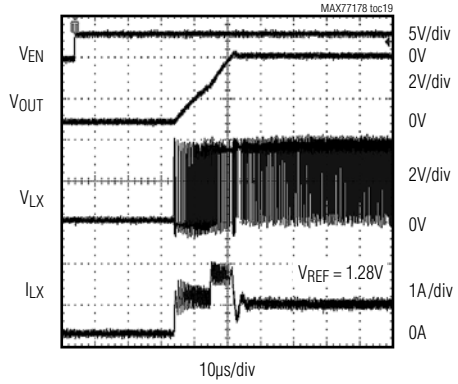
ENABLE WAVEFORM (NO LOAD)



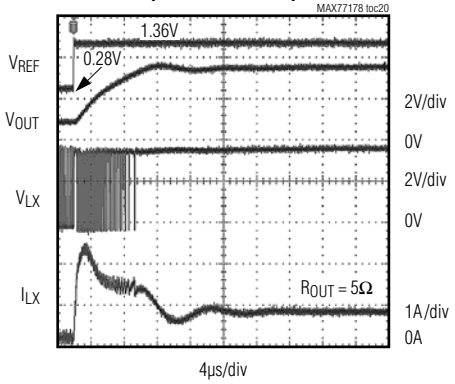
Typical Operating Characteristics (continued)

(*Typical Operating Circuits*, V_{IN} = 3.7V, I_{OUT} = 0.47µH, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)

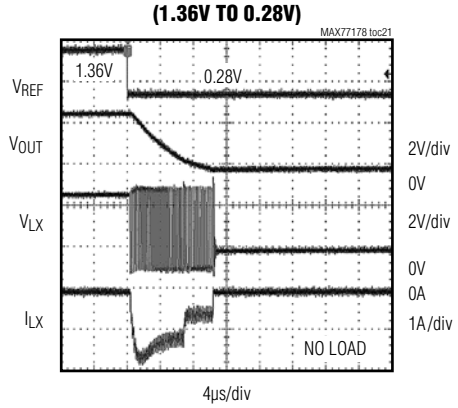
ENABLE WAVEFORM (5Ω LOAD)



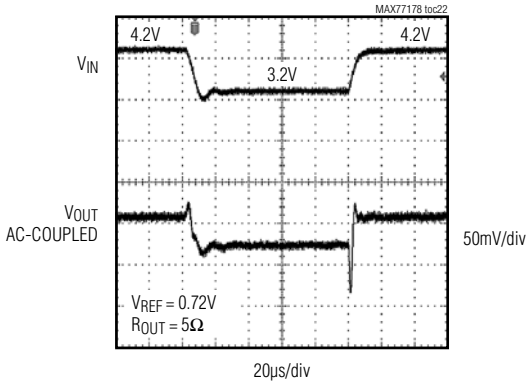
REF TRANSIENT RESPONSE (0.28V TO 1.36V)



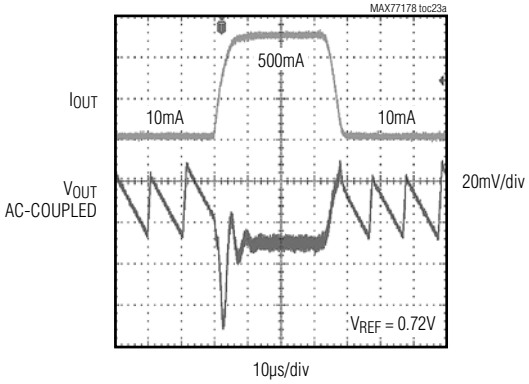
REFIN TRANSIENT RESPONSE (1.36V TO 0.28V)



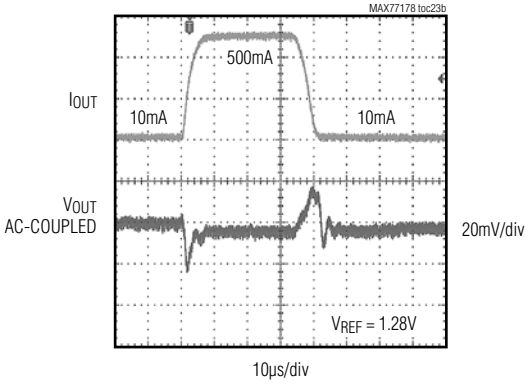
LINE TRANSIENT RESPONSE



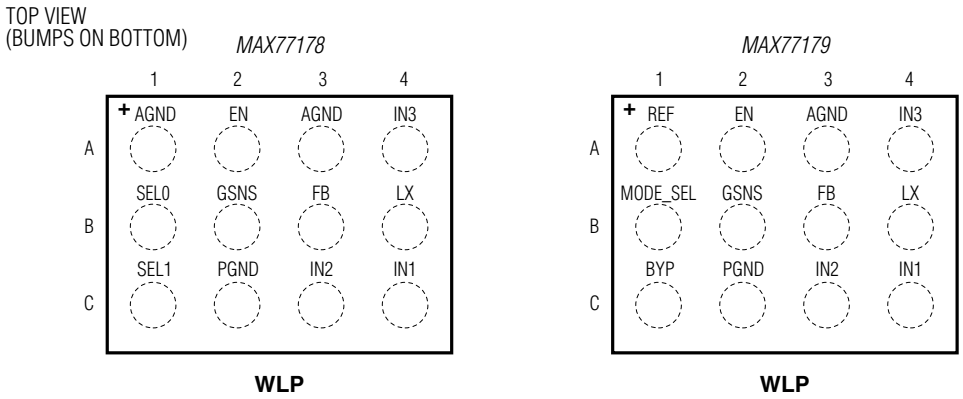
LOAD TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



Pin Configuration



Pin Description

PIN		NAME	FUNCTION
MAX77178	MAX77179		
A1	—	AGND	Ground Connection
—	A1	REF	DAC-Controlled Analog Input. It is used to set the PA voltage. Connect REF to a DAC for PA power control.
A2	A2	EN	Enable Input. Connect EN to IN_ or logic-high for normal operation. Connect EN to AGND or logic-low for shutdown mode.
A3	A3	AGND	Low-Noise Analog Ground. Connect AGND to the IN3 decoupling capacitor and then to PGND.
A4	A4	IN3	Analog Supply Voltage Input. Connect IN3 to a battery or supply voltage from 2.5V to 5.5V. Bypass IN3 to AGND with a 1µF ceramic capacitor as close as possible to the devices. Connect IN3 to the same source as IN1/IN2.
B1	—	SEL0	Output-Voltage Selection Input 0. Connect SEL0 and SEL1 to logic-high or logic-low to set the step-down converter output voltage to one of four voltage levels. See Table 1. SEL0 is internally connected to AGND through an 800kΩ pulldown resistor.
—	B1	MODE_SEL	Mode Selection Input. MODE_SEL adjusts the FET scaling threshold. MODE_SEL is internally connected to AGND through an 800kΩ pulldown resistor.
B2	B2	GSNS	Ground Sense Node. Connect GSNS to the same ground as the DAC used to control REF. Alternatively, GSNS can be connected directly to AGND.
B3	B3	FB	Output-Voltage Feedback Input. Connect FB directly to the load, ensuring that no current is running in FB trace.
B4	B4	LX	Inductor Connection. Connect an inductor from LX to the output of the DC-DC converter. LX is high impedance during shutdown.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX77178	MAX77179		
C1	—	SEL1	Output-Voltage Selection Input 1. Connect SEL0 and SEL1 to logic-high or logic-low to set the step-down converter output voltage to one of four voltage levels. See Table 1. SEL1 is internally connected to AGND through an 800kΩ pulldown resistor.
—	C1	BYP	Bypass Mode Selection Input. When BYP = GND, the IC is set for automatic bypass mode operation. When BYP = IN, the control circuitry forces the IC into bypass mode where the high-side FET is turned on continuously with all FET scaling segments enabled, regardless of the mode of operation. BYP is internally connected to AGND through an 800kΩ pulldown resistor.
C2	C2	PGND	Power Ground. Connect PGND and the input/output capacitor grounds through a star connection to the PCB ground plane.
C3, C4	C3, C4	IN2, IN1	Power-Supply Voltage Input. Connect IN1/IN2 to a battery or supply voltage from 2.5V to 5.5V. IN1/IN2 powers the internal p-channel and n-channel MOSFETs. Bypass IN1/IN2 to PGND with a 4.7µF ceramic capacitor as close as possible to the devices. Connect IN1/IN2 to the same source as IN3.

Detailed Description

The MAX77178/MAX77179 step-down converters are optimized for dynamically powering the PA in multiband 3G/4G mobile communications. They provide a single-device PA power-management solution that supports basic power control for WCDMA and LTE applications. The devices are high-bandwidth converters designed to meet the load-transient response requirements for large-signal polar transmitter architectures.

The MAX77178 provides two logic control inputs (SEL0 and SEL1) to program the DC-DC converter output voltage to one of four options (1.0V, 1.7V, 2.325V, or 2.9V). This method simplifies system implementation by minimizing changes to the existing baseband software. For other output voltage options, contact factory.

The MAX77179 provides an independent DAC-controlled analog input (REF) to support power control applications for WCDMA/LTE. Two other logic control inputs (BYP and MODE_SEL) select the DAC-controlled input source and the ICs' operational modes for multimode applications. The output voltage range (0.5V to V_{IN}) supports operation with a wide variety of PAs, and allows implementation of aggressive power-management schemes.

The 2.5V to 5.5V input supply range supports both current and future battery chemistries. Fast switching frequency allows the use of small ceramic input and output capacitors while maintaining low-ripple voltage. Efficiency is enhanced at light loads by switching to skip mode where the converter switches only as needed to service the load when the skip mode is enabled. Adaptive smart FET scaling further improves efficiency under all operating conditions.

Shutdown Mode

Connect EN to AGND or logic-low to place the ICs in shutdown mode. In shutdown, the control circuitry, internal switching MOSFET and synchronous rectifier turn off and LX becomes high impedance. Connect EN to IN_, or logic-high for normal operation.

SKIP Mode

The step-down converters feature skip mode to provide the highest possible efficiency during light load conditions. Skip mode is only activated when the output voltage is within 12% of the desired regulated value. This requirement maintains the proper slew-rate operation of the output voltage, particularly when the REF input is slewing down. Skip mode occurs when a zero-cross condition is detected on the inductor current.

FET Scaling Operation

The ICs include a FET scaling feature to improve efficiency over a wide range of operating conditions. The size of the power FET is adjusted based on the output-voltage setting of the DC-DC converter to provide optimal efficiency for different output power conditions. Since the ICs can drive multiple PAs, the load resistance and output power operating points can be different. For this reason, the MODE_SEL pin allows selection between two different FET scaling transition points.

Output Voltage Control

The MAX77178 has two digital inputs (SEL0 and SEL1) to set the output voltage to one of four options (1.0V, 1.7V, 2.325V, or 2.9V). See Table 1 for programmable output voltage settings. Contact factory for alternate output voltage settings.

The MAX77179 uses an analog input (REF) driven by an external DAC to control the output voltage linearly for continuous PA power adjustment. See Table 2 for details.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the device. If the junction temperature exceeds +160°C, the step-down converters turn off, allowing the ICs to cool. The step-down converters turn on and begin soft-start after the junction temperature cools by 20°C. This results in a pulsed output during continuous thermal-overload conditions.

Applications Information

Inductor Selection

The ICs operate with a switching frequency of 8MHz and uses a 0.47µH inductor. This operating frequency allows the use of physically small inductors while maintaining high efficiency. See Table 3 for the recommended inductors. The inductor's saturation current rating must meet or exceed the LX current limit. For optimum transient response and highest efficiency, use inductors with a low DC resistance.

Capacitor Selection

The input capacitor in a DC-DC converter reduces current peaks drawn from the input power sources and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency needs to be less than that of the input source so high-frequency switching currents do not pass through the input source. The DC-DC converter output filter capacitors keep output ripple small and ensure control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Ceramic capacitors with X5R, X7R, or better dielectric are recommended for stable operation over the entire operating temperature range.

The primary objective in power-tracking applications is to reduce ripple to approximately 1mV using minimum board space. Note that to minimize space taken, bypassing adjacent to the PA and the power trace between the device and the PA are relied upon to further reduce ripple. See the *PCB Layout* section. Note that since a secondary filter is relied upon to further reduce ripple and since power tracking often operates at high output voltage, reducing the ICs' operating frequency, high value capacitors with lower resonant frequency are recommended. Table 4 lists the recommended capacitor specification for power tracking.

Table 1. MAX77178 Output Voltage Selection

EN	SEL1	SEL0	OUTPUT VOLTAGE (V)
0	X	X	Off
1	0	0	2.9
1	0	1	2.325
1	1	0	1.0
1	1	1	1.7

X = Don't care.

Table 2. MAX77179 Mode Selection

EN	MODE_SEL	BYP	MODE
0	X	X	Off
1	0	0	On, MODE_SEL low mode $V_{OUT} = 2.5 \times V_{REF}$
1	0	1	On, forced bypass mode
1	1	0	On, MODE_SEL high mode $V_{OUT} = 2.5 \times V_{REF}$
1	1	1	On, forced bypass mode

X = Don't care.

Table 3. Suggested Inductors

MANUFACTURER	PART NUMBER	INDUCTANCE (µH)	ESR (mΩ)	CURRENT RATING (A)	DIMENSIONS (mm)
TDK	VLS201610ET-R47N	0.47	54	2.10	2.0 x 1.6 x 0.95
Taiyo Yuden	MAKK2016TR50M	0.50	38	3.2	2.0 x 1.6 x 1.0
Coilcraft	XPL 2010-331	0.33	54	2.75	2.0 x 1.6 x 0.95
TDK	VLS201610ET-R33N	0.33	46	2.50	2.0 x 1.6 x 0.95

Table 4. Recommended Capacitor Specification for Power Tracking

COMPONENT	PART NUMBER	PART DESCRIPTION
C1	Not needed	Less bypassing than envelope tracking needed
C2, C3	Taiyo Yuden JMK105BBJ475MV	4.7µF ±20%, 6.3V X5R ceramic capacitor (0402)
C4	Samsung CL03A105MQ3CSNH	1µF ±10%, 6.3V X5R ceramic capacitor (0201)
C5	Not needed	Replaced by bypassing at PA

PCB Layout

Due to fast-switching waveforms and high-current paths, careful PCB layout is required to achieve optimal performance. Of the current loops present in the ICs, the IN to PGND current loop has the highest AC current and dI/dts. The IN bypass capacitor should be placed as close as possible to the devices. In communication systems, the PA draws rapid pulses of current that can cause a significant transient during transmission. The IN line requires a low-frequency bypassing capacitance. To avoid high-frequency interference, high-frequency capacitor must be placed closer to the device than the low-frequency capacitor. At high frequencies, board layout is governed more by electromagnetic interactions, and less by electronic circuit theory. As an example a constant trace width has less reflection. Use rounded corners and avoid changes in trace width as much as possible.

Minimize trace lengths between the ICs and the inductor, the input capacitor and the output capacitor; keep these traces short, direct, and wide. The ground connections of C_{IN} and C_{OUT} should be as close together as possible and connected to PGND. Connect AGND and PGND directly to the ground plane. Refer to the EV kit for an example layout. See Figure 1.

One difficult aspect of reducing output voltage ripple is minimizing ripple components caused by ESR and ESL of the output capacitor. ESL is often the dominant factor in the output voltage ripple at 8MHz. A 1.5nH ESL causes a 12mV output ripple step based on the 0.47µH inductor to be used. Good layout practice such as placing the capacitor next to the device, using short and wide traces, and running traces over the uninterrupted ground plane can limit parasitic inductance to limit ESL to approximately 0.5nH. Note that above the capacitor's resonance frequency, the output filter's transfer function no longer rolls off with frequency. To reduce this to acceptable levels, it might be necessary to parallel smaller value output capacitors to reduce the ESL and reach the desired value of output capacitance.

It is possible to change the filter topology in an attempt to reduce switching ripple without having to increase the switching frequency or decrease the passband of the output filter. This is done by adding an additional stage to the output filter, called a secondary filter. In power-tracking applications, this can be accomplished by designing the DC-DC converter's output trace and choosing the PA's bypass to act as a filter. For example a 13mm long, 1mm wide trace over 14mils of FR4 has approximately 5nH of inductance. If the PA has 1.5µF of bypass capacitance under operating conditions, the secondary filter formed has a corner frequency of 1.8MHz. Assuming that the PA's bypass capacitance has an ESL of 0.5nH, up to 20dB of output ripple can be removed by this secondary filter.

Note that the ICs are not designed to respond to feedback with the additional phase shift inserted by the secondary filter. The FB terminal of the device should be connected to the output of the primary output filter.

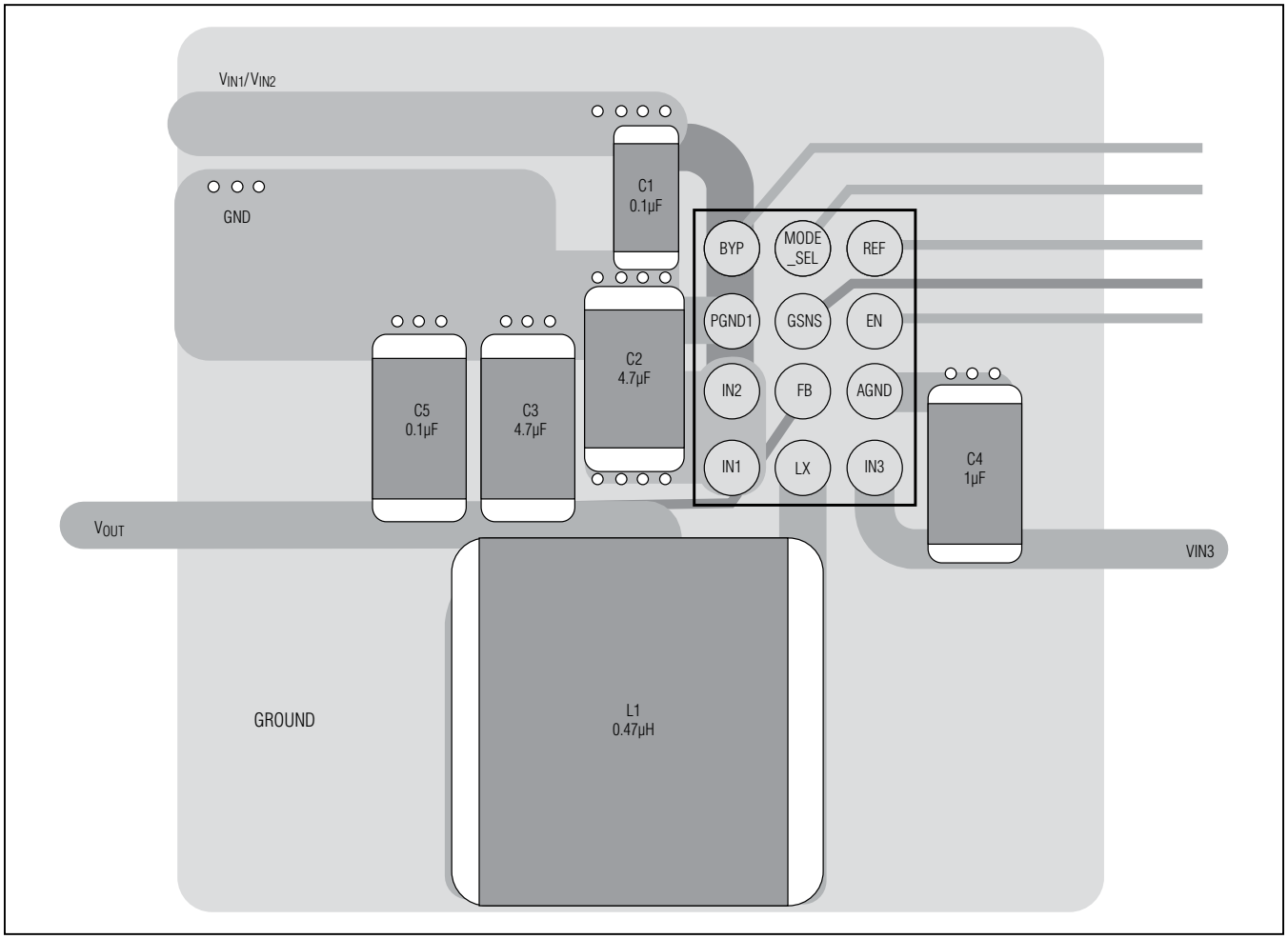
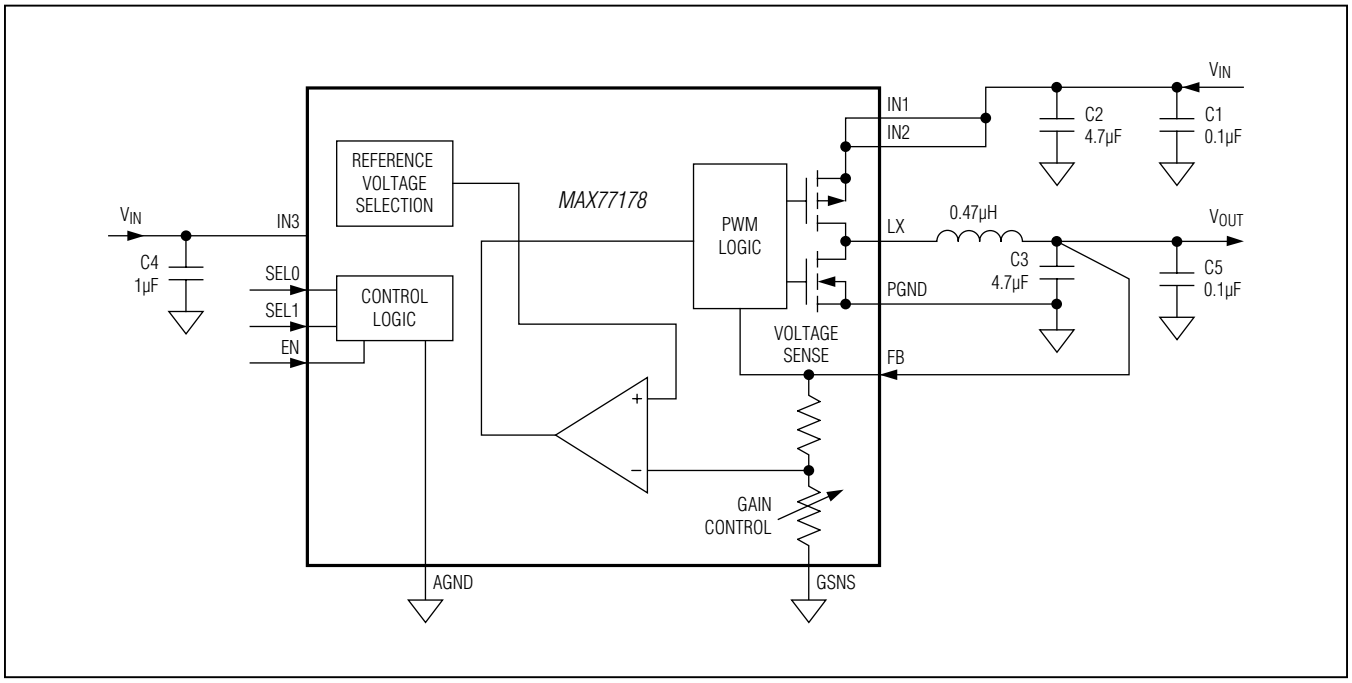
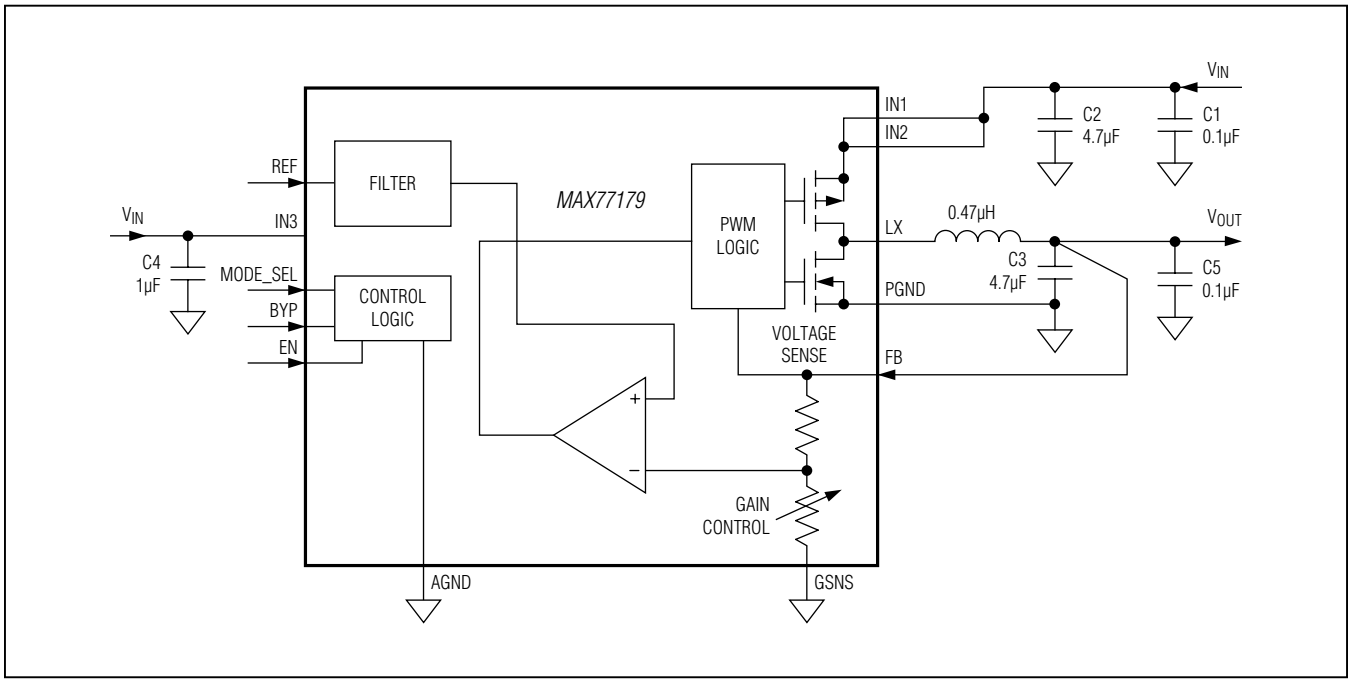


Figure 1. MAX77179 Recommended PCB Layout


VIN
IN1
IN2
C2
4.7µF
C1
0.1µF
REFERENCE
VOLTAGE
SELECTION
MAX77178
PWM
LOGIC
LX
0.47µH
VOUT
VIN
IN3
C4
1µF
SEL0
SEL1
EN
CONTROL
LOGIC
PGND
C3
4.7µF
C5
0.1µF
VOLTAGE
SENSE
FB
GAIN
CONTROL
AGND
GSNS


VIN
IN1
IN2
C2
4.7µF
C1
0.1µF
REF
FILTER
MAX77179
PWM
LOGIC
LX
0.47µH
VOUT
VIN
IN3
C4
1µF
MODE_SEL
BYP
EN
CONTROL
LOGIC
PGND
C3
4.7µF
C5
0.1µF
VOLTAGE
SENSE
FB
GAIN
CONTROL
AGND
GSNS

Ordering Information

PART	PIN-PACKAGE	PACKAGE CODE
MAX77178EWC+T	12 WLP, 0.4mm pitch	W121A1+1
MAX77179EWC+T	12 WLP, 0.4mm pitch	W121A1+1

All devices operate over the -40°C to +85°C temperature range.
+Denotes a lead(Pb)-free/RoHS compliant package.
T = *Tape and reel. These devices have a minimum order increment of 2500 pieces.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	OUTLINE NO.
12 WLP, 0.4mm pitch	W121A1+1	**21-0449**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/13	Initial release	—