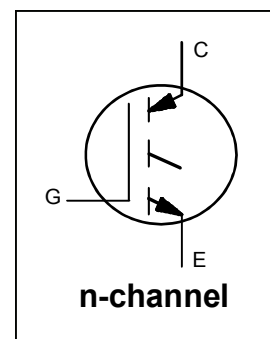


**INSULATED GATE BIPOLAR TRANSISTOR**

**Features**

- Low  $V_{CE(ON)}$  Trench IGBT Technology
- Low Switching Losses
- Maximum Junction Temperature 175 °C
- Short Circuit Rated
- Square RBSOA
- Positive  $V_{CE(ON)}$  Temperature Coefficient
- Tight Parameter Distribution



G	C	E
Gate	Collector	Emitter

**Benefits**

- High Efficiency in a Wide Range of Applications
- Suitable for a Wide Range of Switching Frequencies due to Low  $V_{CE(ON)}$  and Low Switching Losses
- Rugged Transient Performance for Increased Reliability
- Excellent Current Sharing in Parallel Operation

**Applications**

- UPS
- HEV Inverters
- Welding

Base part number	Package Type	Standard Pack		Orderable part number
		Form	Quantity	
IRGC4067B	Die on Film	Wafer	1	IRGC4067B

**Mechanical Parameters**

Die Size	6.528 x 9.144	mm <sup>2</sup>
Minimum Street Width	75	µm
Emitter Pad Size (Included Gate Pad)	See Die Drawing	mm <sup>2</sup>
Gate Pad Size	0.55 x 0.553	
Area Total / Active	59.69/ 44	
Thickness	70	µm
Wafer Size	150	mm
Flat Position	0	Degrees
Maximum-Possible Chips per Wafer	250pcs.	
Passivation Front side	Silicon Nitride	
Front Metal	Al (4µm), Si (1%)	
Backside Metal	Al (1kA°), Ti (1kA°), Ni (4kA°), Ag (6kA°)	
Die Bond	Electrically conductive epoxy or solder	
Reject Ink Dot Size	0.25mm min (black, center)	
Recommended Storage Environment	Store in original container, in dry Nitrogen, < 6 months at an ambient temperature of 23°C	
Reference Packaged Part	IRGPS4067DPbF	

**Maximum Ratings**

	Parameter	Max.	Units
$V_{CE}$	Collector-Emitter Voltage, $T_J=25^\circ\text{C}$	600	V
$I_C$	DC Collector Current	①	A
$I_{LM}$	Clamped Inductive Load Current ④	480	A
$V_{GE}$	Gate Emitter Voltage	$\pm 20$	V
$T_J, T_{STG}$	Operating Junction and Storage Temperature	-40 to +175	$^\circ\text{C}$

**Static Characteristics (Tested on wafers) .  $T_J=25^\circ\text{C}$**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	$V_{GE} = 0V, I_C = 500\mu\text{A}$ ⑤
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	1.7	2.05		$V_{GE} = 15V, I_C = 120A, T_J = 25^\circ\text{C}$
$V_{GE(th)}$	Gate-Emitter Threshold Voltage	4.0	—	6.5		$I_C = 5.6mA, V_{GE} = V_{CE}$
$I_{CES}$	Zero Gate Voltage Collector Current	—	1.0	50	$\mu\text{A}$	$V_{CE} = 600V, V_{GE} = 0V$
$I_{GES}$	Gate Emitter Leakage Current	—	—	$\pm 400$	nA	$V_{CE} = 0V, V_{GE} = \pm 20V$

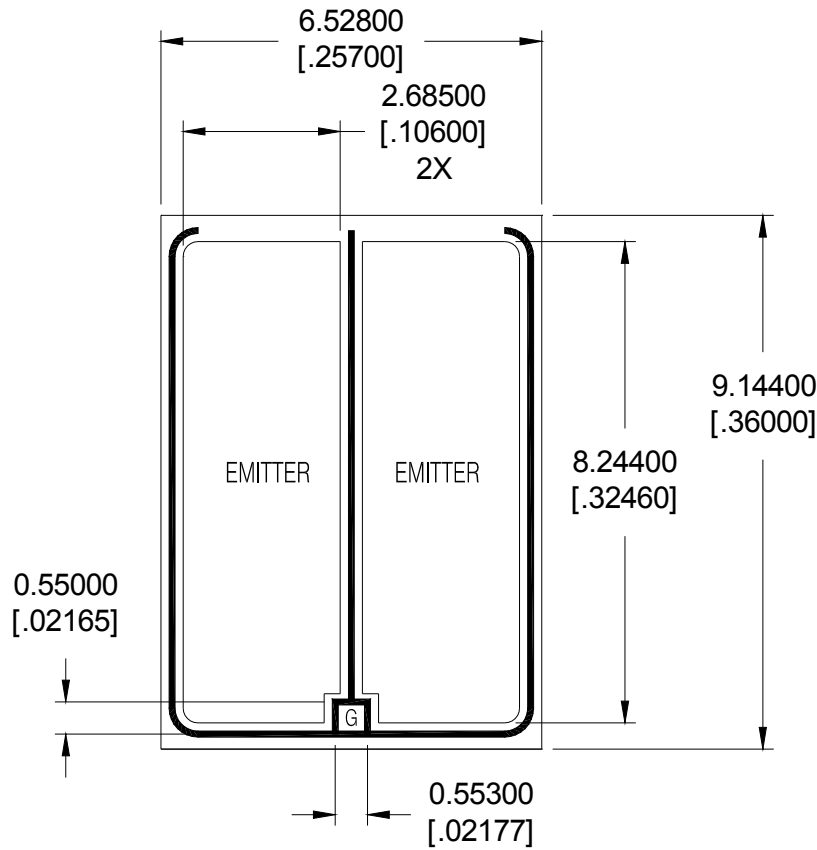
**Electrical Characteristics (Not subject to production test- Verified by design/characterization)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	1.7	2.05	V	$V_{GE} = 15V, I_C = 120A, T_J = 25^\circ\text{C}$
		—	2.2	—		$V_{GE} = 15V, I_C = 120A, T_J = 175^\circ\text{C}$
SCSOA	Short Circuit Safe Operating Area	5	—	—	$\mu\text{s}$	$V_{GE} = 15V, V_{CC} = 400V, \textcircled{2}$ $R_G = 4.7\Omega, V_P \leq 600V, T_J = 150^\circ\text{C}$
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				$T_J = 175^\circ\text{C}, I_C = 480A$ $V_{CC} = 480V, V_P \leq 600V$ $R_g = 4.7\Omega, V_{GE} = +20V \text{ to } 0V$
$C_{iss}$	Input Capacitance	—	7750	—	pF	$V_{GE} = 0V$
$C_{oss}$	Output Capacitance	—	550	—		$V_{CE} = 30V$
$C_{rss}$	Reverse Transfer Capacitance	—	225	—		$f = 1.0\text{MHz}$
$Q_g$	Total Gate Charge (turn-on)	—	240	—	nC	$I_C = 200A$ ⑥
$Q_{ge}$	Gate-to-Emitter Charge (turn-on)	—	69	—		$V_{GE} = 15V$
$Q_{gc}$	Gate-to-Collector Charge (turn-on)	—	90	—		$V_{CC} = 400V$

**Switching Characteristics (Inductive Load-Not subject to production test-Verified by design/characterization)**

	Parameter	Min.	Typ.	Max.	Units	Conditions ③
$t_{d(on)}$	Turn-On delay time	—	50	—	ns	$I_C = 120A, V_{CC} = 400V$ $R_G = 4.7\Omega, V_{GE} = 15V$ $T_J = 25^\circ\text{C}$
$t_r$	Rise time	—	130	—		
$t_{d(off)}$	Turn-Off delay time	—	160	—		
$t_f$	Fall time	—	130	—		
$t_{d(on)}$	Turn-On delay time	—	50	—		$I_C = 120A, V_{CC} = 400V$ $R_G = 4.7\Omega, V_{GE} = 15V$ $T_J = 175^\circ\text{C}$
$t_r$	Rise time	—	130	—		
$t_{d(off)}$	Turn-Off delay time	—	200	—		
$t_f$	Fall time	—	150	—		

# Die Drawing



**NOTES:**

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: MILLIMETERS
3. LETTER DESIGNATION:  
 S = SOURCE    SK = SOURCE KELVIN    E = EMITTER  
 G = GATE    IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:  
 BONDING PADS: < 0.635 TOLERANCE = +/- 0.013  
 WIDTH < [.0250] TOLERANCE = +/- [.0005]  
 & > 0.635 TOLERANCE = +/- 0.025  
 LENGTH > [.0250] TOLERANCE = +/- [.0010]  
 OVERALL DIE: < 1.270 TOLERANCE = +/- 0.102  
 WIDTH < [.050] TOLERANCE = +/- [.004]  
 & > 1.270 TOLERANCE = +/- 0.203  
 LENGTH > [.050] TOLERANCE = +/- [.008]
5. DIE THICKNESS = 0.070 [.0028]    TOL: = 0.007 [.0003]

REFERENCE: IRGC4067B  
 IRGPS4067PBF  
 IRGPS4067DPBF  
 AUIRGPS4067D

**Notes:**

- ① The current in the application is limited by  $T_{JMax}$  and the thermal properties of the assembly.
- ② Not subject to production test- Verified by design / characterization.
- ③ Values influenced by parasitic L and C in measurement.
- ④  $V_{CC} = 80\% (V_{CES})$ ,  $V_{GE} = 20V$ ,  $L = 9.0\mu H$ ,  $R_G = 4.7\Omega$ .
- ⑤ Refer to AN-1086 for guidelines for measuring  $V_{(BR)CES}$  safely
- ⑥ Die Level Characterization.

**Additional Testing and Screening**

For Customers requiring product supplied as Known Good Die (KGD) or requiring specific die level testing, please contact your local IR Sales

**Shipping**

Sawn Wafer on Film. Please contact your local IR sales office for non-standard shipping options

**Handling**

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

**Wafer/Die Storage**

- Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
- Note: To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.

**Further Information**

For further information please contact your local IR Sales office. <http://die.irf.com>

**Revision History**

Date	Comments
07/02/2015	<ul style="list-style-type: none"> <li>• Updated IFX logo on all pages</li> <li>• Removed Vcesat @ <math>I_C = 10A</math>, <math>V_{GE} = 15V</math> on page 2.</li> <li>• Added Vcesat @ <math>I_C = 170A</math>, <math>V_{GE} = 15V</math> on page 2.</li> </ul>