ZL30402

SONET/SDH Network Element PLL

Data Sheet

May 2006

Features

- Meets requirements of GR-253 for SONET stratum 3 and SONET Minimum Clocks (SMC)
- Meets requirements of GR-1244 for stratum 3
- Meets requirements of G.813 Option 1 and 2 for SDH Equipment Clocks (SEC)
- Generates clocks for ST-BUS, DS1, DS2, DS3, OC-3, E1, E2, E3, STM-1 and 19.44 MHz
- Holdover accuracy to $1x10^{-12}$ meets GR-1244 Stratum 3E and ITU-T G.812 requirements
- Continuously monitors Primary and Secondary reference clocks
- Provides “hit-less” reference switching
- Compensates for Master Clock Oscillator accuracy
- Detects frequency of both reference clocks and synchronizes to any combination of 8 kHz, 1.544 MHz, 2.048 MHz and 19.44 MHz reference frequencies.
- Allows Hardware or Microprocessor control
- Pin compatible with MT90401 device.

Applications

- Synchronization for SDH and SONET Network Elements
- Clock generation for ST-BUS and GCI backplanes

Ordering Information

ZL30402/QCC	80 Pin LQFP	Trays
ZL30402QCG1	80 Pin LQFP*	Trays, Bake & Drypack
	*Pb Free Matte Tin	

-40°C to +85°C

Description

The ZL30402 is a Network Element Phase-Locked Loop designed to synchronize SDH and SONET systems. In addition, it generates multiple clocks for legacy PDH equipment and provides timing for ST-BUS and GCI backplanes.

The ZL30402 operates in NORMAL (LOCKED), HOLDOVER and FREE-RUN modes to ensure that in the presence of jitter, wander and interruptions to the reference signals, the generated clocks meet international standards. The filtering characteristics of the PLL are hardware or software selectable and they do not require any external adjustable components. The ZL30402 uses an external 20 MHz Master Clock Oscillator to provide a stable timing source for the HOLDOVER operation.

The ZL30402 operates from a single 3.3 V power supply and offers a 5 V tolerant microprocessor interface.

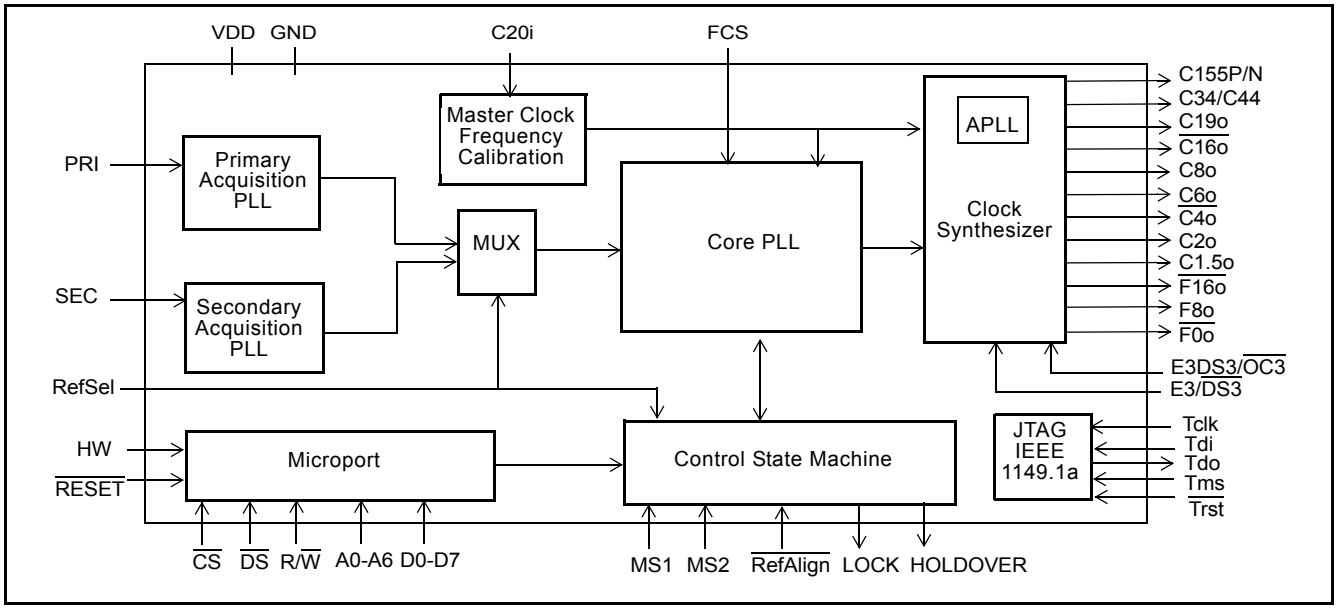

Figure 1 - Functional Block Diagram

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Change Summary

The following table captures the changes from the April 2005 issue.

Page	Item	Change
1		Updated Ordering Information.

1.0 ZL30402 Pinout

1.1 Pin Connections

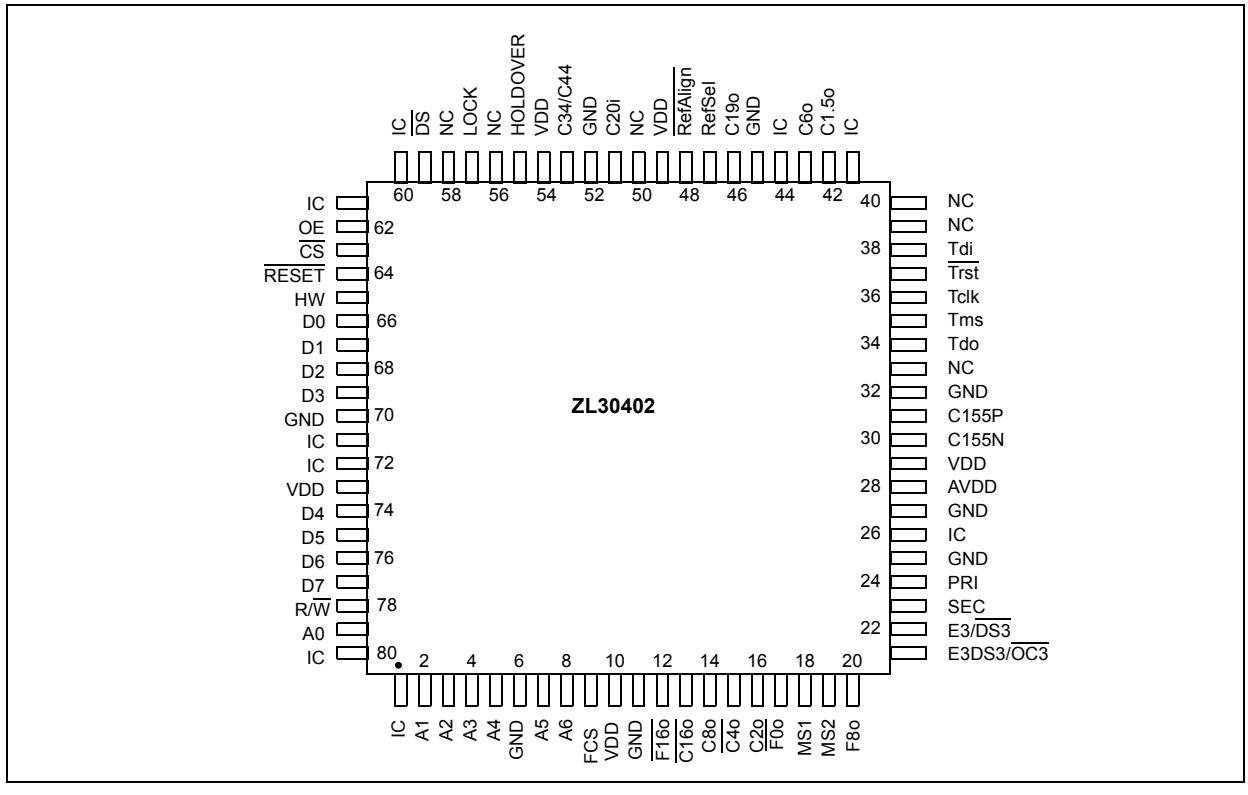


Figure 2 - Pin Connections for 80-pin LQFP package

Pin Description

Pin #	Name	Description
1	IC	**Internal Connection**. Leave unconnected.
2-5	A1-A4	**Address 1 to 4** (5 V tolerant input). Address inputs for the parallel processor interface. Connect to ground in Hardware Control.
6	GND	**Ground**. Negative power supply.
7-8	A5-A6	**Address 5 to 6** (5 V tolerant input). Address inputs for the parallel processor interface. Connect to ground in Hardware Control.
9	FCS	**Filter Characteristic Select (Input)**. In Hardware Control, FCS selects the filtering characteristics of the ZL30402. Set this pin high to have a loop filter corner frequency of 0.1 Hz and limit the phase slope to 885 ns per second. Set this pin low to have corner frequency of 1.1 Hz and limit the phase slope to 41 ns per 1.326 ms. Connect to ground in Software Control. This pin is internally pulled down to GND.
10	VDD	**Positive Power Supply.**
11	GND	**Ground**.
12	$\overline{\text{F16o}}$	**Frame Pulse ST-BUS 8.192 Mb/s** (CMOS tristate output). This is an 8 kHz, 61 ns wide, active low framing pulse, which marks beginning of a ST-BUS frame. This frame pulse is typically used for ST-BUS operation at 8.192 Mb/s
13	$\overline{\text{C16o}}$	**Clock 16.384 MHz** (CMOS tristate output). This clock is used for ST-BUS operation at 8.192 Mb/s.
14	C8o	**Clock 8.192 MHz** (CMOS tristate output). This clock is used for ST-BUS operation at 8.192 Mb/s.
15	$\overline{\text{C4o}}$	**Clock 4.096 MHz** (CMOS tristate output). This clock is used for ST-BUS operation at 2.048 Mb/s.
16	C2o	**Clock 2.048 MHz** (CMOS tristate output). This clock is used for ST-BUS operation at 2.048 Mb/s.
17	$\overline{\text{F0o}}$	**Frame Pulse ST-BUS 2.048 Mb/s** (CMOS tristate output). This is an 8 kHz, 244 ns, active low framing pulse, which marks the beginning of a ST-BUS frame. This is typically used for ST-BUS operation at 2.048 Mb/s and 4.096 Mb/s.
18	MS1	**Mode Select 1** (Input). The MS1 and MS2 pins select the ZL30402 mode of operation (Normal, Holdover or Free-run), see Table 1 on page 18 for details. The logic level at this input is sampled by the rising edge of the F8o frame pulse. Connect to ground in Software Control.
19	MS2	**Mode Select 2** (Input). The MS2 and MS1 pins select the ZL30402 mode of operation (Normal, Holdover or Free-run), see Table 1 on page 18 for details. The logic level at this input is sampled by the rising edge of the F8o frame pulse. Connect to ground in Software Control.

Pin Description (continued)

Pin #	Name	Description
20	F8o	**Frame Pulse ST-BUS/GCI 8.192 Mb/s** (CMOS tristate output). This is an 8 kHz, 122 ns, active high framing pulse, which marks the beginning of a ST-BUS/GCI frame. This is typically used for ST-BUS/GCI operation at 8.192 Mb/s. See Figure 13 for details.
21	E3DS3/$\overline{OC3}$	**E3DS3 or OC3 Selection** (Input). In Hardware Control, a logic low on this pin enables the C155P/N outputs (pin 30 and pin 31) and sets the C34/C44 output (pin 53) to provide C8 or C11 clocks. Logic high at this input disables the C155 clock outputs (high impedance) and sets C34/C44 output to provide C34 and C44 clocks. In Software Control connect this pin to ground.
22	E3/$\overline{DS3}$	**E3 or DS3 Selection** (Input). In Hardware Control, when the E3DS3/$\overline{OC3}$ pin is set high, logic low on E3/$\overline{DS3}$ pin selects a 44.736 MHz clock on C34/C44 output and logic high selects 34.368 MHz clock. When E3DS3/$\overline{OC3}$ pin is set low, logic low on E3/$\overline{DS3}$ pin selects 11.184 MHz clock on C34/C44 output and logic high selects 8.592 MHz clock. Connect this input to ground in Software Control.
23	SEC	**Secondary Reference** (Input). This input is used as a secondary reference source for synchronization. The ZL30402 can synchronize to the falling edge of the 8 kHz, 1.544 MHz or 2.048 MHz clocks and the rising edge of the 19.44 MHz clock. In Hardware Control, selection of the input reference is based upon the RefSel control input. This pin is internally pulled up to VDD.
24	PRI	**Primary Reference** (Input). This input is used as a primary reference source for synchronization. The ZL30402 can synchronize to the falling edge of the 8 kHz, 1.544 MHz or 2.048 MHz clocks and the rising edge of the 19.44 MHz clock. In Hardware Control, selection of the input reference is based upon the RefSel control input. This pin is internally pulled up to VDD.
25	GND	**Ground**.
26	IC	**Internal Connection**. Leave unconnected.
27	GND	**Ground**.
28	AVDD	**Positive Analog Power Supply**. Connect this pin to VDD.
29	VDD	**Positive Power Supply**.
30 31	C155N C155P	**Clock 155.52 MHz** (LVDS output). Differential outputs for a 155.52 MHz clock. These outputs are enabled by applying logic low to E3DS3/$\overline{OC3}$ input or they can be switched into high impedance state by applying logic high.
32	GND	**Ground**.
33	NC	**No internal bonding Connection**. Leave unconnected.
34	Tdo	**IEEE1149.1a Test Data Output** (CMOS output). JTAG serial data is output on this pin on the falling edge of Tclk clock. If not used, this pin should be left unconnected.

Pin Description (continued)

Pin #	Name	Description
35	Tms	**IEEE1149.1a Test Mode Selection** (3.3 V input). JTAG signal that controls the state transition on the TAP controller. This pin is internally pulled up to VDD. If not used, this pin should be left unconnected.
36	Tclk	**IEEE1149.1a Test Clock Signal** (5.5 V tolerant input). Input clock for the JTAG test logic. If not used, this pin should be pulled up to VDD.
37	$\overline{\text{Trst}}$	**IEEE1149.1a Reset Signal** (3.3 V input). Asynchronous reset for the JTAG TAP controller. This pin should be pulsed low on power-up to ensure that the device in the normal functional state. This pin is internally pulled up to VDD. If not used, this pin should be connected to GND.
38	Tdi	**IEEE1149.1a Test Data Input** (3.3 V input). Input for JTAG serial test instructions and data. This pin is internally pulled up to VDD. If not used, this pin should be left unconnected.
39	NC	**No internal bonding Connection.** Leave unconnected.
40	NC	**No internal bonding Connection.** Leave unconnected.
41	IC	**Internal Connection.** Leave unconnected.
42	C1.5o	**Clock 1.544 MHz** (CMOS tristate output). This output provides a 1.544 MHz DS1 rate clock.
43	C6o	**Clock 6.312 MHz** (CMOS tristate output). This output provides a 6.312 MHz DS2 rate clock.
44	IC	**Internal Connection**. Connect this pin to Ground.
45	GND	**Ground**.
46	C19o	**Clock 19.44 MHz** (CMOS tristate output). This output provides a 19.44 MHz clock.
47	RefSel	**Reference Source Select** (Input). A logic low selects the PRI (primary) reference source as the input reference signal and logic high selects the SEC (secondary) input. The logic level at this input is sampled at the rising edge of F8o. This pin is internally pulled down to GND.
48	$\overline{\text{RefAlign}}$	**Reference Align** (Input). In Hardware Control a high to low transition at this input initiates phase realignment between the input reference and the generated output clocks. This pin is internally pulled down to GND.
49	VDD	**Positive Power Supply**.
50	NC	**No internal bonding Connection.** Leave unconnected.
51	C20i	**Clock 20 MHz** (5.5 V tolerant input). This pin is the input for the 20 MHz Master Clock Oscillator.
52	GND	**Digital Ground**.

Pin Description (continued)

Pin #	Name	Description
53	C34/C44	**Clock 34.368 MHz / clock 44.736 MHz** (CMOS Output). This clock is programmable to be either 34.368 MHz (for E3 applications) or 44.736 MHz (for DS3 applications) when E3DS3/OC3 is high, or to be either 8.592MHz or 11.184 MHz when E3DS3/OC3 is low. See description of E3DS3/OC3 and E3/DS3 inputs for details. In Software Control the functionality of this output is controlled by Control Register 2 (Table 7 "Control Register 2 (R/W)").
54	VDD	**Positive Power Supply**.
55	HOLDOVER	**Holdover Indicator** (CMOS output). Logic high at this output indicates that the device is in Holdover mode.
56	NC	**No internal bonding Connection**. Leave unconnected.
57	LOCK	**Lock Indicator** (CMOS output). Logic high at this output indicates that ZL30402 is locked to the input reference.
58	NC	**No internal bonding Connection.** Leave unconnected.
59	$\overline{DS}$	**Data Strobe** (5 V tolerant input). This input is the active low data strobe of the processor interface.
60	IC	**Internal Connection**. Connect to ground.
61	IC	**Internal Connection.** Leave unconnected.
62	OE	**Output Enable** (Input). Logic high on this input enables C19, $\overline{F16}$, $\overline{C16}$, C8, C6, C4, C2, C1.5, F8 and F0 signals. Pulling this input low will force the output clocks pins into a high impedance state.
63	$\overline{CS}$	**Chip Select** (5 V tolerant input). This active low input enables the microprocessor interface. When $\overline{CS}$ is set to high, the microprocessor interface is idle and all Data Bus I/O pins will be in a high impedance state.
64	$\overline{RESET}$	**$\overline{RESET}$** (5 V tolerant input). This active low input forces the ZL30402 into a RESET state. The $\overline{RESET}$ pin must be held low for a minimum of 1µs to reset the device properly. The ZL30402 must be reset after power-up.
65	HW	**Hardware/Software Control** (Input). If this pin it tied low, the ZL30402 is controlled via the microport. If it is tied high, the ZL30402 is controlled via the control pins MS1, MS2, FCS, RefSel, RefAlign, E3/DS3 and E3DS3/OC3.
66-69	D0 - D3	**Data 0 to Data 3** (5 V tolerant three-state I/O). These signals combined with D4 - D7 form the bi-directional data bus of the microprocessor interface (D0 is the least significant bit).
70	GND	**Ground**.
71	IC	**Internal Connection** (Input). Connect this pin to ground.
72	IC	**Internal Connection** (Input). Connect this pin to ground.
73	VDD	**Positive Power Supply**.

Pin Description (continued)

Pin #	Name	Description
74 - 77	D4 - D7	**Data 4 to Data 7** (5 V tolerant three-state I/O). These signals combine with D0 - D3 form the bi-directional data bus of the processor interface (D7 is the most significant bit).
78	R/$\overline{W}$	**Read/Write Strobe** (5 V tolerant input). This input controls the direction of the data bus D[0-7] during a microprocessor access. When R/$\overline{W}$ is high, the parallel processor is reading data from the ZL30402. When low, the parallel processor is writing data to the ZL30402.
79	A0	**Address 0** (5 V tolerant input). Address input for the microprocessor interface. A0 is the least significant input.
80	IC	**Internal Connection** (Input). Connect this pin to ground.

2.0 Functional Description

The ZL30402 is a Network Element PLL designed to provide timing for SDH and SONET equipment conforming to ITU-T, ANSI, ETSI and Telcordia recommendations. In addition, it generates clocks for legacy PDH equipment operating at DS1, DS2, DS3, E1, and E3 rates. The ZL30402 provides clocks for industry standard ST-BUS and GCI backplanes, and it also supports H.110 timing requirements. The functional block diagram of the ZL30402 is shown in Figure 1 "Functional Block Diagram" and its operation is described in the following section.

2.1 Acquisition PLLs

The ZL30402 has two Acquisition PLLs for monitoring availability and quality of the Primary (PRI) and Secondary (SEC) reference clocks. Each Acquisition PLL operates independently and locks to the falling edges of one of the three input reference frequencies: 8 kHz, 1.544 MHz, 2.048 MHz or to the rising edge of 19.44 MHz. The reference frequency can be determined from reading the Acquisition PLL Status Register bits InpFreq1 and InpFreq0 (see Table 16 "Primary Acquisition PLL Status Register (R)" and Table 17 "Secondary Acquisition PLL Status Register (R)").

The Primary and Secondary Acquisition PLLs are designed to provide status information that identifies two levels of reference clock quality. For clarity, only the Primary Acquisition PLL is referenced in the text, but the same applies to the Secondary Acquisition PLL.

- Reference frequency drifts more than ±30000 ppm or is lost completely. In response, the Primary Acquisition PLL enters its own Holdover mode and indicates this by asserting the HOLDOVER bit in the Primary Acquisition PLL Status Register (Table 16 "Primary Acquisition PLL Status Register (R)"). Entry into Holdover forces the Core PLL into the Auto Holdover state.
- Reference frequency drifts more than ±104 ppm. In response the Primary Acquisition PLL asserts the Frequency Limit bit PAFL in its Primary Acquisition PLL Status Register (Table 16) indicating that the reference frequency crossed the boundary of the capture range.

Outputs of both Acquisition PLLs are connected to a multiplexer (MUX), which allows selecting a reference signal that guarantees better traceability to the Primary Reference Clock. This multiplexer channels binary words to the Core PLL digital phase detector (instead of analog signals). Application of the digital phase detector in the Core PLL eliminates quantization errors and improves phase alignment accuracy.

The bandwidth of the Acquisition PLL is much wider than the bandwidth of the following Core PLL. This feature allows cascading Acquisition and Core PLLs without changing the transfer function of the Core PLL.

2.2 Core PLL

The most critical element of the ZL30402 is its Core PLL, which generates a phase-locked clock, filters jitter and wander and suppresses input phase transients. All of these features are in agreement with international standards:

- G.813 Option 1 and 2 clocks for SDH equipment
- GR-253 for SONET stratum 3 and SONET Minimum Clocks (SMC)
- GR-1244 for stratum 3 Clocks

The Core PLL supports three mandatory modes of operation: Free-run, Normal (Locked) and Holdover. Each of these modes places specific requirements on the building blocks of the Core PLL.

- In Free-run Mode, the Core PLL locks to the 20 MHz Master Clock Oscillator connected to pin C20i. The stability of the generated clock remains the same as the stability of the Master Clock Oscillator but frequency accuracy is greatly improved by the Master Clock Frequency Calibration register. This register compensates oscillator frequency, practically eliminating manufacturing tolerances.
- In Normal Mode, the Core PLL locks to one of the Acquisition PLLs. Both Acquisition PLLs provide preprocessed phase data to the Core PLL including detection of reference clock quality. This preprocessing reduces the load on the Core PLL and improves quality of the generated clock.
- In Holdover mode, the Core PLL generates a clock based on data collected from past reference signals. The Core PLL enters Holdover mode if the attached Acquisition PLL switches into the Holdover state or under external software or hardware control.

Some of the key elements of the Core PLL are shown in Figure 3 "Core PLL Functional Block Diagram".

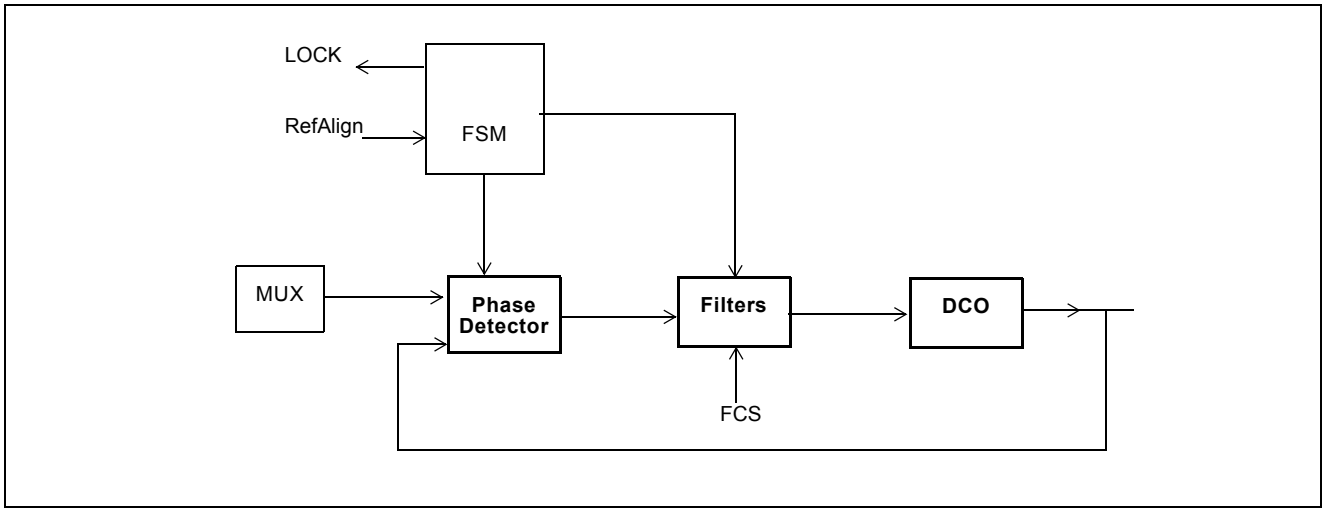


Figure 3 - Core PLL Functional Block Diagram

Digitally Controlled Oscillator (DCO): The DCO is an arithmetic unit that continuously generates a stream of numbers that represent the phase-locked clock. These numbers are passed to the Clock Synthesizer (see section 2.3) where they are converted into electrical clock signals of different frequencies.

Filters: In Normal mode, the clock generated by the DCO is phase-locked to the input reference signal and band-limited to meet network synchronization standards. The ZL30402 provides two software programmable (Control Reg 1) and two hardware selectable (FCS pin) filtering options. The filtering characteristics are similar to a first order low pass filter with corner frequencies that support international standards:

- **0.1 Hz** filter: supports G.813 Option 2 Clock, GR-253 SONET stratum 3 and GR-253 SONET Minimum clock
- **1.1 Hz** filter: supports G.813 Option 1 and GR-1244 stratum 3 clock

Lock Indicator: Entry into Normal mode is flagged by the LOCK status bit or pin. Lock is declared when the Acquisition PLL is locked to the reference clock and the Core PLL is locked to the Acquisition PLL. Frequency lock means that the center frequency of the PLL is identical to the reference frequency and phase error excursions caused by jitter and wander are symmetrical around some long-term phase error average.

Reference Re-alignment: Reference realignment is performed to erase a residual phase error that has been accumulated between the reference and output clocks as a result of reference switching. A high to low transition on the $\overline{\text{RefAlign}}$ pin (or bit) initiates phase realignment with a phase slope on the output clocks limited to 41 ns in 1.326 ms for the 1.1 Hz filter and to 885 ns in 1 s for 0.1 Hz filter. Please refer to the ZLAN-27 "Phase Alignment between 8 kHz output and 8 kHz Input Reference on ZL30402" Application Note for details.

2.3 Clock Synthesizer

The output of the Core PLL is connected to the Clock Synthesizer that generates twelve clocks and three frame pulses.

2.4 Output Clocks

The ZL30402 provides the following clocks (see Figure 13 "ST-BUS and GCI Output Timing", Figure 14 "DS1, DS2 and C19o Clock Timing", Figure 15 "C155o and C19o Timing", and Figure 18 "E3 and DS3 Output Timing" for details):

- C1.5o : 1.544 MHz clock with nominal 50% duty cycle
- C2o : 2.048 MHz clock with nominal 50% duty cycle
- $\overline{\text{C4o}}$: 4.096 MHz clock with nominal 50% duty cycle
- C6o : 6.312 MHz clock with nominal 50% duty cycle
- C8o : 8.192 MHz clock with nominal 50% duty cycle
- C8.5o : 8.592 MHz clock with duty cycle from 30 to 70%.
- C11o : 11.184 MHz clock with duty cycle from 30 to 70%.
- $\overline{\text{C16o}}$: 16.384 MHz clock with nominal 50% duty cycle
- C19o : 19.44 MHz clock with nominal 50% duty cycle (with optional dejittering)
- C34o : 34.368 MHz clock with nominal 50% duty cycle
- C44o : 44.736 MHz clock with nominal 50% duty cycle
- C155 : 155.52 MHz clock with nominal 50% duty cycle.

The ZL30402 provides the following frame pulses (see Figure 13 "ST-BUS and GCI Output Timing" for details). All frame pulses have the same 125 µs period (8kHz frequency):

- $\overline{\text{F0o}}$: 244 ns wide, logic low frame pulse
- F8o : 122 ns wide, logic high frame pulse
- $\overline{\text{F16o}}$: 61 ns wide, logic low frame pulse

The Clock Synthesizer has an internal analog PLL (APLL) that can be placed in the path of the digitally generated clocks to multiply frequencies and reduce jitter. The combination of two pins, E3DS3/$\overline{\text{OC3}}$ and $\overline{\text{E3DS3}}$, controls the placement of the APLL and allows for selection of different clock configurations e.g., if E3DS3/$\overline{\text{OC3}}$ pin is low the 19.44 MHz clock is derived from 155.52 MHz clock with very low jitter. The same APLL can be used to generate clocks with E3, DS3 or OC3 rates (see Figure 4 "C19o, C155o, C34/C44 Clock Generation Options" for details).

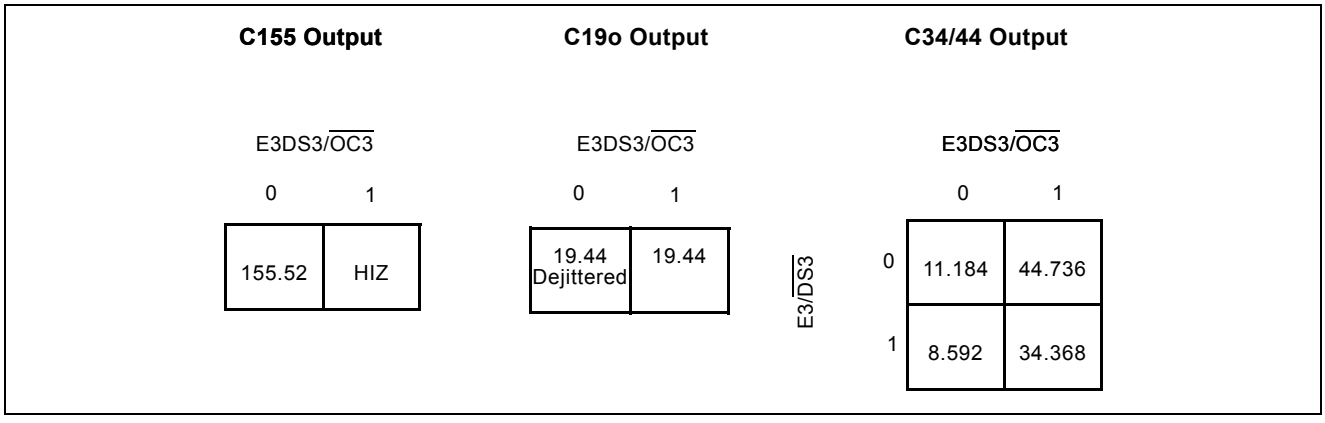


Figure 4 - C19o, C155o, C34/C44 Clock Generation Options

All clocks and frame pulses except the C155 are output with CMOS logic levels. The C155 clock (155.52MHz) is output in a standard LVDS format.

2.5 Output Clocks Phase Adjustment

The ZL30402 provides three control registers dedicated to programming the output clock phase offset. Clocks C16o, C8o, C4o and C2o and frame pulses F16o, F8o, F0o are derived from 16.384 MHz and can be jointly shifted with respect to an active reference clock by up to 125 µs with a step size of 61 ns. The required phase shift of clocks is programmable by writing to the Phase Offset Register 2 ("Table 8") and to the Phase Offset Register 1 ("Table 9"). The C1.5o clock can be shifted as well in step sizes of 81ns by programming C1.5POA bits in Control Register 3 ("Table 11").

The coarse phase adjustment is augmented with a very fine phase offset control on the order of 477 ps per step. This fine adjustment is programmable by writing to the Fine Phase Offset Register (Table 15 "Fine Phase Offset Register (R/W)"). The offset moves all clocks and frame pulses generated by ZL30402 including C155 clock.

2.6 Control State Machine

2.6.1 Clock Modes

Any Network Element that operates in a synchronous network must support three Clock Modes: Free-run, Normal (Locked) and Holdover. These clock modes determine behavior of a Network Element to the unforeseen changes in the network synchronization hierarchy. Requirements for Clock Modes are defined in the international standards e.g.: G.813, GR-1244-CORE and GR-253-CORE and they are very strictly enforced by network operators. The ZL30402 supports all clock modes and each of these modes have a corresponding state in the Control State Machine.

2.6.2 ZL30402 State Machine

The ZL30402 Control State Machine is a complex combination of many internal states supporting the three mandatory clock modes. The simplified version of this state machine is shown in Figure 5 and it includes the mandatory states: Free-run, Normal and Holdover. These three states are complemented by two additional states: Reset and Auto Holdover, which are critical to the ZL30402 operation under the changing external conditions.

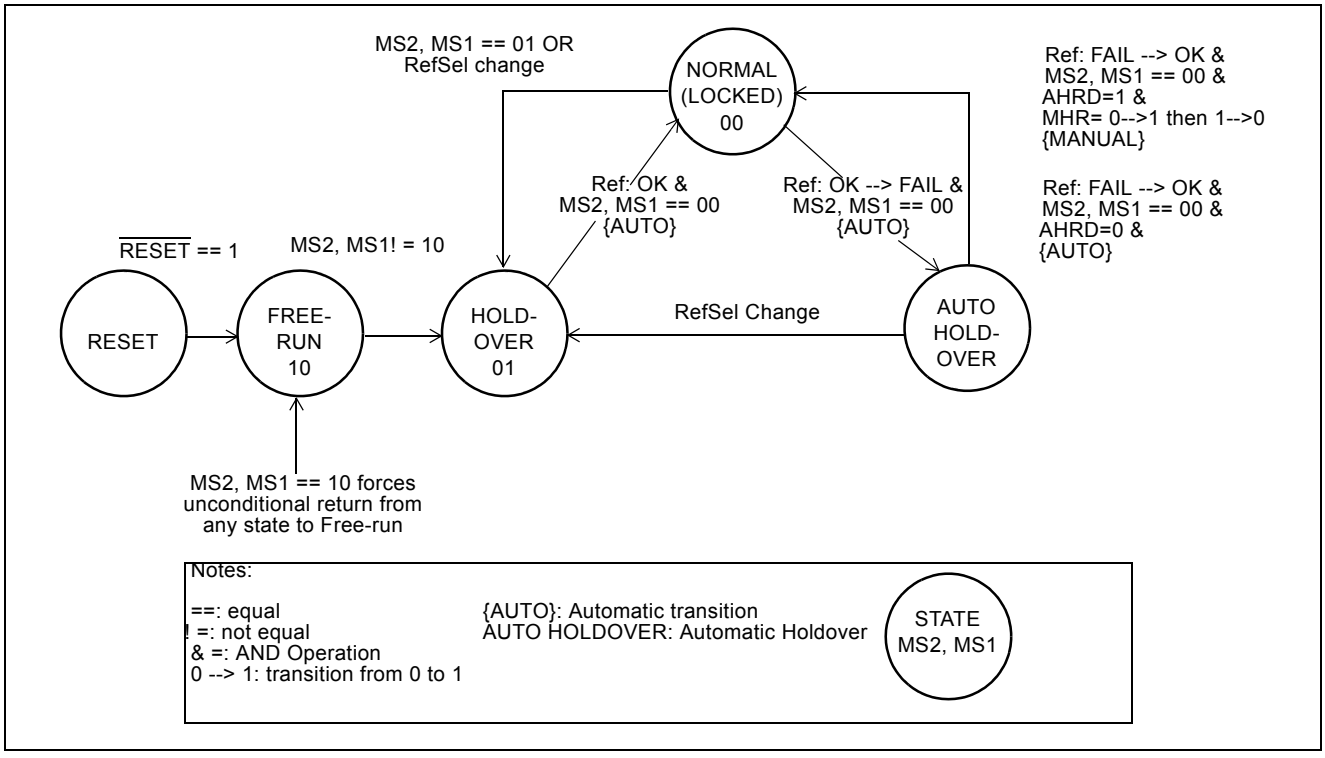


Figure 5 - ZL30402 State Machine

2.6.3 Reset State

The Reset State must be entered when ZL30402 is powered-up. In this state, all arithmetic calculations are halted, clocks are stopped, the microprocessor port is disabled and all internal registers are reset to their default values. The Reset state is entered by pulling the $\overline{\text{RESET}}$ pin low for a minimum of 1 µs. When the $\overline{\text{RESET}}$ pin is pulled back high, internal logic starts a 500 µs initialization process before switching into the Free-run state (MS2, MS1 = 10).

2.6.4 Free-Run State (Free-Run mode)

The Free-run state is entered when synchronization to the network is not required or is not possible. Typically this occurs during installation, repairs or when a Network Element operates as a master node in an isolated network. In the Free-run state, the accuracy of the generated clocks is determined by the accuracy and stability of the ZL30402 Master Crystal Oscillator. When equipment is installed for the first time (or periodically maintained) the accuracy of the Free-run clocks can be adjusted to within $1x10^{-12}$ by setting the offset frequency in the Master Clock Frequency Calibration Register.

2.6.5 Normal State (Normal Mode or Locked Mode)

The Normal State is entered when a good quality reference clock from the network is available for synchronization. The ZL30402 automatically detects the frequency of the reference clock (8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz) and sets the LOCK status bit and pin high after acquiring synchronization. In the Normal state all generated clocks (C1.5o, C2o, C4o, C6o, C8o, C16o, C19o, C34/C44 and C155) and frame pulses (F0o, F8o, $\overline{\text{F16o}}$) are derived from network timing. To guarantee uninterrupted synchronization, the ZL30402 has two Acquisition PLLs that continuously monitor the quality of the incoming reference clocks. This dual architecture enables quick replacement of a poor or failed reference and minimizes the time spent in other states.

2.6.6 Holdover State (Holdover Mode)

The Holdover State is typically entered for short durations while network synchronization is temporarily disrupted. In Holdover Mode, the ZL30402 generates clocks, which are not locked to an external reference signal but their frequencies are based on stored coefficients in memory that were determined while the PLL was in Normal Mode and locked to an external reference signal.

The initial frequency offset of the ZL30402 in Holdover Mode is $1x10^{-12}$. This is more accurate than Telcordia's GR-1244-CORE stratum 3E requirement of $\pm 1x10^{-9}$. Once the ZL30402 has transitioned into Holdover Mode, holdover stability is determined by the stability of the 20MHz Master Clock Oscillator. Selection of the oscillator requires close examination of the crystal oscillator temperature sensitivity and frequency drift caused by aging.

2.6.7 Auto Holdover State

The Auto Holdover state is a transitional state that the ZL30402 enters automatically when the active reference fails unexpectedly. When the ZL30402 detects loss of reference it sets the HOLDOVER status bit and waits in Auto Holdover state until the failed reference recovers. The HOLDOVER status may alert the control processor about the failure and in response the control processor may switch to the secondary reference clock. The Auto Holdover and Holdover States are internally combined together and they are output as a HOLDOVER status on pin 55 and bit 4 in Status Register 1 (Table 6 on page 22).

2.6.8 State Transitions

In a typical Network Element application, the ZL30402 will typically operate in Normal mode (MS2, MS1 == 00) generating synchronous clocks. Its two Acquisition PLLs will continuously monitor the input references for signs of degraded quality and output status information for further processing. The status information from the Acquisition PLLs and the CORE PLL combined with status information from line interfaces and framers (as listed below) forms the basis for creating reliable network synchronization.

- Acquisition PLLs (PAH, PAFL, SAH, SAFL) and
- Core PLL (LOCK, HOLDOVER, FLIM)
- Line interfaces (e.g. LOS - Loss of Signal, AIS - Alarm Indication Signal) and
- Framers (e.g. LOF - Loss of frame or Synchronization Status Messages carried over SONET S1 byte or ESF-DS1 Facility Data Link).

The ZL30402 State Machine is designed to perform some transitions automatically, leaving other less time dependent tasks to the control processor. The state machine includes two stimulus signals which are critical to automatic operation: "OK --> FAIL" and "FAIL --> OK" that represent loss (and recovery) of reference signal or its drift by more than ±30000 ppm. Both of them force the Core PLL to transition into and out of the Auto Holdover state. The ZL30402 State Machine may also be driven by controlling the mode select pins or bits MS2, MS1. In order to avoid network synchronization problems, the State Machine has built-in basic protection that does not allow switching the Core PLL into a state where it cannot operate correctly e.g. it is not possible to force the Core PLL into Normal mode when all references are lost.

3.0 Master Clock Frequency Calibration Circuit

In an ordinary timing generation module, the Free-run mode accuracy of generated clocks is determined by the accuracy of the Master Crystal Oscillator. If the Master Crystal Oscillator has a manufacturing tolerance of +/- 4.6 ppm, the generated clocks will have no better accuracy.

The ZL30402 eliminates tolerance problems by providing a programmable Master Clock Frequency Calibration circuit, which can reduce oscillator manufacturing tolerance to near zero. This feature eliminates the need for high precision 20 MHz crystal oscillators, which could be very expensive for equipment that has to maintain accuracy over a very long period of time (e.g., 20 years in some applications).

The compensation value for the Master Clock Calibration Register (MCFC3 to MCFC0) can be calculated from the following equation:

$$MCFC = 45036 * (- f_{offset}) \quad \text{where:} \quad f_{offset} = f_m - 20\,000\,000 \text{ Hz}$$

The f_m frequency should only be measured after the Master Crystal Oscillator has been mounted inside a system and powered long enough for the Master Crystal Oscillator to reach a steady operating temperature. Section 5.2 on page 31 provides two examples of how to calculate an offset frequency and convert the decimal value to a binary format. The maximum frequency compensation range of the MCFC register is equal to ±2384 ppm (±47680 Hz).

3.1 Microprocessor Interface

The ZL30402 can be controlled by a microprocessor or by an ASIC type of device that is connected directly to the hardware control pins. If the HW pin is tied low (see Figure 6 "Hardware and Software Control options"), an 8-bit Motorola type microprocessor may be used to control PLL operation and check its status. Under software control, the control pins MS2, MS1, FCS, RefSel, RefAlign are disabled and they are replaced by the equivalent control bits. The output pins LOCK and HOLDOVER are always active and they provide current status information whether the device is in microprocessor or hardware control. Software (microprocessor) control provides additional functionality that is not available in hardware control such as output clock phase adjustment, master clock frequency calibration and extended access to status registers. These registers are also accessible when the ZL30402 operates under Hardware control.

3.2 JTAG Interface

The ZL30402 JTAG (Joint Test Action Group) interface conforms to the Boundary-Scan standard IEEE1149.1-1990, which specifies a design-for-testability technique called Boundary-Scan Test (BST). The BST architecture is made up of four basic elements, Test Access Port (TAP), TAP Controller, Instruction Register (IR) and Test Data Registers (TDR) and all these elements are implemented on the ZL30402.

Zarlink Semiconductor provides a Boundary Scan Description Language (BSDL) file that contains all the information required for a JTAG test system to access the ZL30402's boundary scan circuitry. The file is available for download from the Zarlink Semiconductor web site: www.zarlink.com.

4.0 Hardware and Software Control

The ZL30402 offers Hardware and Software Control options that simplify design of basic or complex clock synchronization modules. Hardware control offers fewer features but still allows for building of sophisticated timing cards without extensive programming. The complete set of control and status functions for each mode are shown in Figure 6 "Hardware and Software Control options".

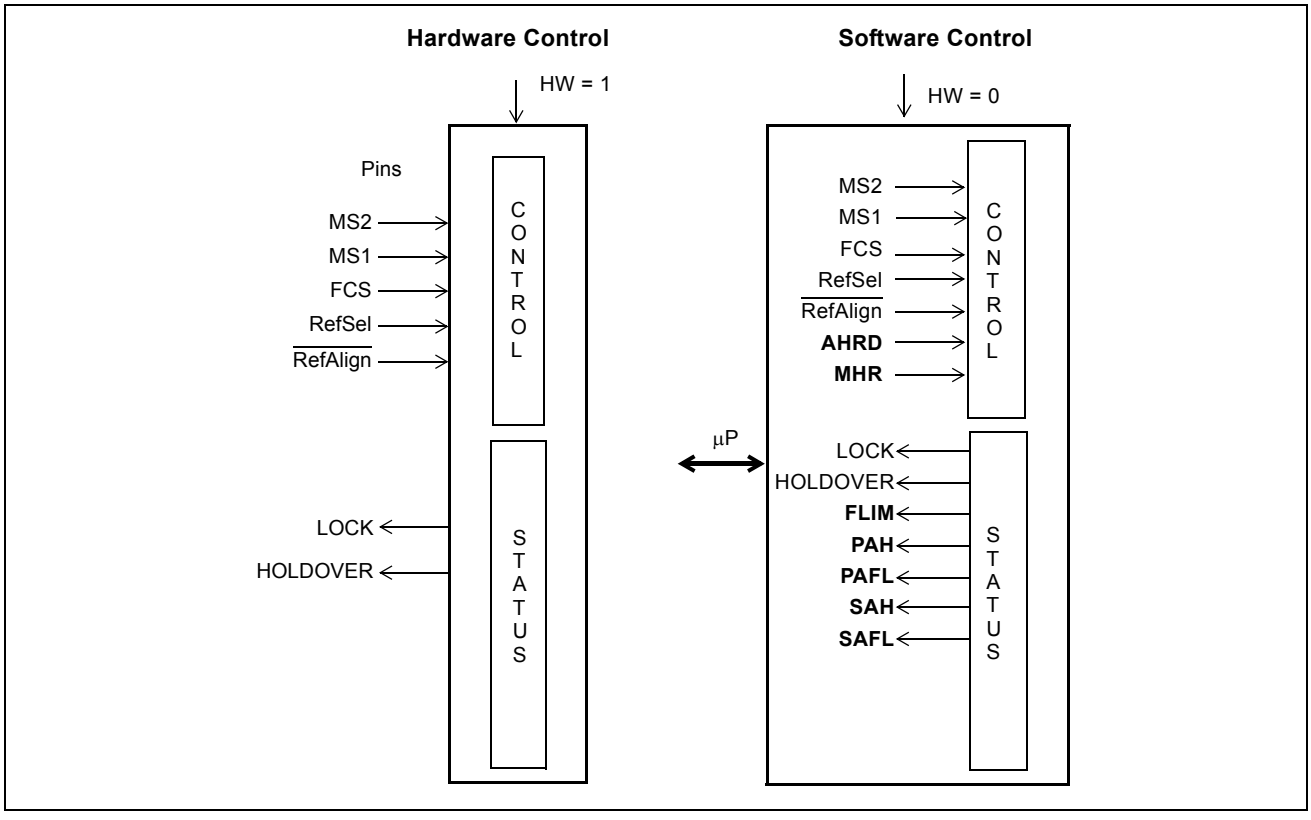


Figure 6 - Hardware and Software Control options

4.1 Hardware Control

The Hardware control is a subset of software control and it will only be briefly described with cross-referencing to Software control programmable registers.

4.1.1 Control Pins

The ZL30402 has six dedicated control pins for selecting modes of operation and activating different functions. These pins are listed below:

MS2 and MS1 pins: **Mode Select**: The MS2 (pin 19) and MS1 (pin 18) inputs select the PLL mode of operation. See Table 1 for details. The logic level at these inputs is sampled by the rising edge of the F8o frame pulse.

FCS pin: **Filter Characteristic Select**. The FCS (pin 9) input is used to select the filtering characteristics of the Core PLL. See Table 2 on page 19 for details.

MS2	MS1	Mode of Operation
0	0	Normal mode
0	1	Holdover mode
1	0	Free-run
1	1	Reserved

Table 1 - Operating Modes and States

FCS	Filtering Characteristic	Phase Slope
0	**Filter corner frequency set to 1.1 Hz.** This selection meets requirements of G.813 Option 1 and GR-1244 stratum 3 clocks.	41ns in 1.326ms
1	**Filter corner frequency set to 0.1 Hz.** This selection meets requirements of G.813 Option 2, GR-253 for SONET stratum 3 and GR-253 for SONET Minimum Clocks (SMC).	885ns/s

Table 2 - Filter Characteristic Selection

RefSel: **Reference Source Select**. The RefSel (pin 47) input selects the PRI (primary) or SEC (secondary) input as the reference clock for the Core PLL. The logic level at this input is sampled by the rising edge of F8o.

RefSel	Input Reference
0	Core PLL connected to the Primary Acquisition PLL
1	Core PLL connected to the Secondary Acquisition PLL

Table 3 - Reference Source Select

$\overline{\text{RefAlign}}$: Reference Align. The $\overline{\text{RefAlign}}$ (pin 48) input controls phase realignment between the input reference and the generated output clocks.

4.1.2 Status Pins

The ZL30402 has two dedicated status pins for indicating modes of operation. These pins are listed below:

LOCK. This output goes high when the core PLL is locked to the selected Acquisition PLL.

HOLDOVER - This output goes high when the Core PLL enters Holdover mode. The Core PLL will switch to Holdover mode if the respective Acquisition PLL enters Holdover mode or if the mode select pins or bits are set to Holdover (MS2, MS1 = 01).

4.2 Software Control

Software control is enabled by setting the HW pin to logic zero (HW = 0). In this mode all hardware control pins (inputs) are disabled and status bits (outputs) are enabled. The ZL30402 has seventeen registers that provide all the functionality available in Hardware control and in addition they offer advanced control and monitoring that is only available in Software control (see Figure 6 "Hardware and Software Control options").

4.2.1 Control Bits

The ZL30402 has seven control bits as is shown in Figure 6 "Hardware and Software Control options". The first five bits replace the five hardware control pins: MS2, MS1, FCS, RefSel and $\overline{\text{RefAlign}}$ and the last two bits support recovery from Auto Holdover mode: AHRD and MHR. These bits are described in section 3.2.4.

In addition to the Control bits shown in Figure 6 "Hardware and Software Control options", the ZL30402 has a number of bits and registers that are accessed infrequently or during configuration only e.g., Phase Offset Adjustment or Master Clock Frequency Calibration.

4.2.2 Status Bits

The ZL30402 has seven status bits (see Figure 6 "Hardware and Software Control options"). The first two bits perform the same function as their equivalent status pins. The last five bits perform two functions. Bits FLIM, PAFL, SAFL indicate drift of the reference clock frequencies beyond the capture range of Acquisition and Core PLLs and bits PAH and SAH show entry of Primary and Secondary Acquisition PLLs into Holdover mode. These bits are described in detail in section 3.2.4. The status pins are enabled when the ZL30402 operates in software control and they can be used to trigger interrupts.

4.2.3 ZL30402 Register Map

Addresses: 00H to 6FH

Address hex	Register	Read Write	Function
00	Control Register 1	R/W	RefSel, 0, 0, MS2, MS1, FCS, 0, $\overline{\text{RefAlign}}$
01	Status Register 1	R	rsv, rsv, LOCK, HOLDOVER, rsv, FLIM, rsv, rsv
04	Control Register 2	R/W	E3DS3/$\overline{\text{OC3}}$, E3/$\overline{\text{DS3}}$, 0, 0, 0, 0, 0, 0,
06	Phase Offset Register 2	R/W	0, 0, 0, 0, OffEn, C16POA10, C16POA9, C16POA8
07	Phase Offset Register 1	R/W	C16POA7, C16POA6, C16POA5, C16POA4, C16POA3, C16POA2, C16POA1, C16POA0
0F	Device ID Register	R	0010 0001
11	Control Register 3	R/W	rsv, rsv, C1.5POA2, C1.5POA1, C1.5POA0, 0, 0, 0
13	Clock Disable Register 1	R/W	0, 0, C16dis, C8dis, C4dis, C2dis, C1.5dis,0
14	Clock Disable Register 2	R/W	0, 0, 0, F8odis, F0odis, F16odis, C6dis, C19dis
19	Core PLL Control Register	R/W	0, 0, 0, 0, 0, 0, MHR, AHRD, 0
1A	Fine Phase Offset Register	R/W	FPOA7, FPOA6, FPOA5, FPOA4, FPOA3, FPOA2, FPOA1, FPOA0
20	Primary Acquisition PLL Status Register	R	rsv, rsv, rsv, rsv, InpFreq1, InpFreq0, rsv, PAH,PAFL
28	Secondary Acquisition PLL Status Register	R	rsv, rsv, rsv, rsv, InpFreq1, InpFreq0, rsv, SAH, SAFL
40	Master Clock Frequency Calibration Register - Byte 4	R/W	MCFC31, MCFC30, MCFC29, MCFC28, MCFC27, MCFC26, MCFC25, MCFC24,
41	Master Clock Frequency Calibration Register - Byte 3	R/W	MCFC23, MCFC22, MCFC21, MCFC20, MCFC19, MCFC18, MCFC17, MCFC16
42	Master Clock Frequency Calibration Register - Byte 2	R/W	MCFC15, MCFC14, MCFC13, MCFC12, MCFC11, MCFC10, MCFC9, MCFC8
43	Master Clock Frequency Calibration Register - Byte 1	R/W	MCFC7, MCFC6, MCFC5, MCFC4, MCFC3, MCFC2, MCFC1, MCFC0

Table 4 - ZL30402 Register Map

Note: The ZL30402 uses address space from 00h to 6Fh. Registers at address locations not listed above must not be written or read.

4.2.4 Register Description

Address: 00 H

Bit	Name	Functional Description	Default
7	RefSel	**Reference Select**. A zero selects the PRI (Primary) reference source as the input reference signal and a one selects the SEC (secondary) reference.	0
6-5	RSV	**Reserved**.	00
4-3	MS2, MS1	**Mode Select** - MS2 = 0 MS1 = 0 Normal Mode (Locked Mode) - MS2 = 0 MS1 = 1 Holdover Mode - MS2 = 1 MS1 = 0 Free-run Mode - MS2 = 1 MS1 = 1 Reserved	10
2	FCS	**Filter Characteristic Select** FCS = 0 Filter corner frequency set to 1.1 Hz. This selection meets requirements of G.813 Option 1 and GR-1244 stratum 3 clocks. FCS = 1 Filter corner frequency set to 0.1 Hz. This selection meets requirements of G.813 Option 2, GR-253 for SONET stratum 3 and GR-253 for SONET Minimum Clocks (SMC).	0
1	RSV	**Reserved**.	0
0	$\overline{\text{RefAlign}}$	**$\overline{\text{Reference Align}}$**. A high-to-low transition aligns the generated output clocks to the input reference signal. The maximum phase slope depends on the Filter Characteristic selected and is limited to: - 41ns in 1.326ms for FCS = 0 - 885 ns in 1s for FCS = 1	1

Table 5 - Control Register 1 (R/W)

Address: 01 H

Bit	Name	Functional Description
7	RSV	**Reserved.**
6	RSV	**Reserved.**
5	LOCK	**Lock**. This bit goes high when the Core PLL is locked to the selected Acquisition PLL.
4	HOLDOVER	**Holdover**. This bit goes high when the Core PLL enters Holdover mode. Detection of reference failure and subsequent transition from Normal to Holdover state takes approximately: 0.750 μs for 19.44 MHz reference, 0.850 μs for 2.048 MHz reference, 1.1 μs for 1.544 MHz reference and 130 μs for 8 kHz reference.
3	RSV	**Reserved**.
2	FLIM	**Frequency Limit**. This bit goes high when the Core PLL is pulled by the input reference signal to the edge of its frequency tracking range set at ±104 ppm. This bit may change state momentarily in the event of large jitter or wander excursions occurring when the input reference is close to the frequency limit range.
1	RSV	**Reserved**.
0	RSV	**Reserved**.

Table 6 - Status Register 1 (R)

Address: 04 H

Bit	Name	Functional Description	Default
7	E3DS3/$\overline{\text{OC3}}$	**E3, DS3 or OC-3 clock select**. Setting this bit to zero enables the C155P/N outputs (pin 30 and pin 31) and enables the C34/C44 output (pin 53) to provide C8 or C11 clocks. Logic high sets the C155 clock outputs into high impedance and enables the C34/C44 output to provide a C34 or C44 clock.	0
6	E3/$\overline{\text{DS3}}$	**E3 or DS3 clock select**. When E3DS3/$\overline{\text{OC3}}$ bit is set high, a logic low on the E3/$\overline{\text{DS3}}$ bit selects a 44.736 MHz clock on the C34/C44 output and logic high selects a 34.368 MHz clock. When the E3DS3/$\overline{\text{OC3}}$ bit is set low, a logic low on the E3/$\overline{\text{DS3}}$ bit selects an 11.184 MHz clock on the C34/C44 output and a logic high selects an 8.592 MHz clock.	0
5-0	RSV	**Reserved.**	000000

Table 7 - Control Register 2 (R/W)

Address: 06 H

Bit	Name	Functional Description	Default
7-4	RSV	**Reserved**.	0000
3	OffEn	**Offset Enable**. Set high to enable programmable phase offset adjustments (C16 Phase Offset Adjustment and C1.5 Phase Offset Adjustment) between the input reference and the generated clocks.	0
2 - 0	C16POA10 to C16POA8	**C16 Phase Offset Adjustment**. These three bits (most significant) in conjunction with the eight bits of Phase Offset Register 1 allow for phase shifting of all clocks and frame pulses that are derived from the C16 clock (C8o, C4o, C2o, F16o, F8o, F0o). The phase offset is an unsigned number in a range from 0 to 2047. Each increment by one represents phase-offset advancement by 61.035 ns with respect to the input reference signal. The phase offset is a two-byte value and it must be written in one step increments. For example: four writes are required to advance clocks by 244 ns from its current position of 22H: write 23H, 24H, 25H, 26H. Writing numbers in reverse order will delay clocks from their present position.	000

Table 8 - Phase Offset Register 2 (R/W)

Address: 07 H

Bit	Name	Functional Description	Default
7-0	C16POA7 to C16POA0	**C16 Phase Offset Adjustment**. The eight least significant bits of the phase offset adjustment word. See the Phase Offset Register 2 for details.	0000 0000

Table 9 - Phase Offset Register 1 (R/W)

Address: 0F H

Bit	Name	Functional Description
7-4	ID7 - 4	**Device Identification Number**. These four bits represent the device part number. The ID number for ZL30402 is 0010.
3-0	ID3 - 0	**Device Revision Number**. These bits represent the revision number. Number starts from 0001.

Table 10 - Device ID Register (R)

Address: 11 H

Bit	Name	Functional Description	Default
7	RSV	**Reserved**.	0
6	RSV	**Reserved.**	0
5-3	C1.5POA2 to C1.5POA0	**C1.5 Phase Offset Adjustment**. These three bits allow for changing of the phase offset of the C1.5o clock relative to the active input reference. The phase offset is an unsigned number in a range from 0 to 7. Each increment by one represents phase-offset advancement by 80.96 ns. Example: Writing 010 advances C1.5 clock by 162 ns. Successive writing of 001 delays this clock by 80.96 ns from its present position	000
2-0	RSV	**Reserved**.	000

Table 11 - Control Register 3 (R/W)

Address: 13 H

Bit	Name	Functional Description	Default
7	RSV	**Reserved**.	0
6	RSV	**Reserved**.	0
5	C16dis	**16.384 MHz Clock Disable**. When set high, this bit tristates the 16.384 MHz clock output.	0
4	C8dis	**8.192 MHz Clock Disable.** When set high, this bit tristates the 8.192 MHz clock output.	0
3	C4dis	**4.096 MHz Clock Disable**. When set high, this bit tristates the 4.096 MHz clock output.	0
2	C2dis	**2.048 MHz Clock Disable**. When set high, this bit tristates the 2.048 MHz clock output.	0
1	C1.5dis	**1.544 MHz Clock Disable**. When set high, this bit tristates the 1.544 MHz clock output.	0
0	RSV	**Reserved**.	0

Table 12 - Clock Disable Register 1 (R/W)

Address: 14 H

Bit	Name	Functional Description	Default
7-5	RSV	**Reserved**.	000
4	F8odis	**F8o Frame Pulse Disable**. When set high, this bit tristates the 8 kHz 122 ns active high framing pulse output.	0
3	F0odis	**$\overline{\text{F0o}}$ Frame Pulse Disable**. When set high, this bit tristates the 8 kHz 244 ns active low framing pulse output.	0
2	F16odis	**$\overline{\text{F16o}}$ Frame Pulse Disable**. When set high, this bit tristates the 8 kHz 61 ns active low framing pulse output.	0
1	C6dis	**6.312 MHz Clock Disable**. When set high, this bit tristates the 6.312 MHz clock output.	0
0	C19dis	**19.44 MHz Clock Disable**. When set high, this bit tristates the 19.44 MHz clock output.	0

Table 13 - Clock Disable Register 2 (R/W)

Address: 19 H

Bit	Name	Functional Description	Default
7-3	RSV	**Reserved**.	00000
2	MHR	**Manual Holdover Release**. A change form 0 to 1 on the MHR bit will release the Core PLL from Auto Holdover to Normal when automatic return from Holdover is disabled (AHRD is set to 1). This bit is level sensitive and it must be cleared immediately after it is set to 1 (next write operation). This bit has no effect if AHRD is set to 0.	0
1	AHRD	**Automatic Holdover Return Disable**. When set high, this bit inhibits the Core PLL from automatically switching back to Normal mode from Auto Holdover state when the active Acquisition PLL regains lock to input reference. The active Acquisition PLL is the Acquisition PLL to which the Core PLL is currently connected.	0
0	RSV	**Reserved**.	0

Table 14 - Core PLL Control Register (R/W)

Address: 1A H

Bit	Name	Functional Description	Default
7-0	FPOA7 - 0	**Fine Phase Offset Adjustment**. This register allows phase offset adjustment of all output clocks and frame pulses (C16o, C8o, C4o, C2o, F16o, F8o, F0o, C155, C19o, C34/44, C1.5o, C6o) relative to the active input reference. The adjustment can be positive (advance) or negative (delay) with a nominal step size of 477 ps (61.035 ns / 128). The rate of phase change is limited to 885 ns/s for FCS = 1 and 41 ns in 1.326 ms for FCS = 0 selections. The phase offset value is a signed 2's complement number e.g.: Advance: +1 step = 01H, +2 steps = 02H, +127 steps = EFH Delay: -1 step = FFH, -2 steps = FEH, -128 steps = 80H Example: Writing 08H advances all clocks by 3.8 ns and writing F3H delays all clocks	00000000

Table 15 - Fine Phase Offset Register (R/W)

Address: 20 H

Bit	Name	Functional Description
7-5	RSV	**Reserved**.
4-3	InpFreq1-0	**Input Frequency**. These two bits identify the Primary Reference Clock frequency. - 00 = 19.44 MHz - 01 = 8 kHz - 10 = 1.544 MHz - 11 = 2.048 MHz
2	RSV	**Reserved**.
1	PAH	**Primary Acquisition PLL Holdover**. This bit goes high whenever the Acquisition PLL enters Holdover mode. Holdover mode is entered when the reference frequency is - lost completely - drifts more than ±30 000 ppm off from the nominal frequency - a large phase hit occurs on the reference clock.
0	PAFL	**Primary Acquisition PLL Frequency Limit**. This bit goes high whenever the Acquisition PLL exceeds its capture range of ±104 ppm. This bit can flicker high in the event of a large excursion of still tolerable input jitter.

Table 16 - Primary Acquisition PLL Status Register (R)

Address: 28 H

Bit	Name	Functional Description
7-5	RSV	**Reserved**.
4-3	InpFreq1-0	**Input Frequency**. These two bits identify the Secondary Reference Clock frequency. - 00 = 19.44 MHz - 01 = 8 kHz - 10 = 1.544 MHz - 11 = 2.048 MHz
2	RSV	**Reserved**.
1	SAH	**Secondary Acquisition PLL Holdover**. This bit goes high whenever the Acquisition PLL enters Holdover mode. Holdover mode is entered when reference frequency is: - lost completely - drifts more than ±30 000 ppm off the nominal frequency - a large phase hit occurs on the reference clock.
0	SAFL	**Secondary Acquisition PLL Frequency Limit**. This bit goes high whenever the Acquisition PLL exceeds its capture range of ±104 ppm. This bit can flicker high in the event of a large excursion of still tolerable input jitter.

Table 17 - Secondary Acquisition PLL Status Register (R)

Address: 40 H

Bit	Name	Functional Description	Default
7-0	MCFC31 - 24	**Master Clock Frequency Calibration**. This most significant byte contains the 31st to 24th bit of the Master Clock Frequency Calibration Register. See Applications section 4.2 for a detailed description of how to calculate the MCFC value.	00000000

Table 18 - Master Clock Frequency Calibration Register 4 (R/W)

Address: 41 H

Bit	Name	Functional Description	Default
7-0	MCFC23 - 16	**Master Clock Frequency Calibration**. This byte contains the 23rd to 16th bit of the Master Clock Frequency Calibration Register.	00000000

Table 19 - Master Clock Frequency Calibration Register 3 (R/W)

Address: 42 H

Bit	Name	Functional Description	Default
7-0	MCFC15 - 8	**Master Clock Frequency Calibration**. This byte contains the 15th to 8th bit of the Master Clock Frequency Calibration Register.	00000000

Table 20 - Master Clock Frequency Calibration Register 2 (R/W)

Address: 43 H

Bit	Name	Functional Description	Default
7-0	MCFC7 - 0	**Master Clock Frequency Calibration**. This byte contains bit 7 to bit 0 of the Master Clock Frequency Calibration Register.	00000 000

Table 21 - Master Clock Frequency Calibration Register 1 (R/W)

5.0 Applications

This section contains application specific details for Mode Switching and Master Clock Oscillator calibration.

5.1 ZL30402 Mode Switching - Examples

The ZL30402 is designed to transition from one mode to the other driven by the internal State Machine or by manual control. The following examples present a couple of typical scenarios of how the ZL30402 can be employed in network synchronization equipment (e.g., timing modules, line cards or stand alone synchronizers).

5.1.1 System Start-up Sequence: FREE-RUN --> HOLDOVER --> NORMAL

The FREE-RUN to HOLDOVER to NORMAL transition represents a sequence of steps that will most likely occur during a new system installation or scheduled maintenance of timing cards. The process starts from the RESET state and then transitions to Free-run mode where the system (card) is being initialized. At the end of this process the ZL30402 should be switched into Normal mode (with MS2, MS1 set to 00) instead of Holdover mode. If the reference clock is available, the ZL30402 will transition briefly into Holdover to acquire synchronization and switch automatically to Normal mode. If the reference clock is not available at this time, as it may happen during new system installation, then the ZL30402 will stay in Holdover indefinitely. While in Holdover mode, the Core PLL will continue generating clocks with the same accuracy as in the Free-run mode, waiting for a good reference clock. When the system is connected to the network (or timing card switched to a valid reference) the Acquisition PLL will quickly synchronize and clear its own Holdover status (PAH bit). This will enable the Core PLL to start the synchronization process. After acquiring lock, the ZL30402 will automatically switch from Holdover into Normal mode without system intervention. This transition to the Normal mode will be flagged by the LOCK status bit and pin.

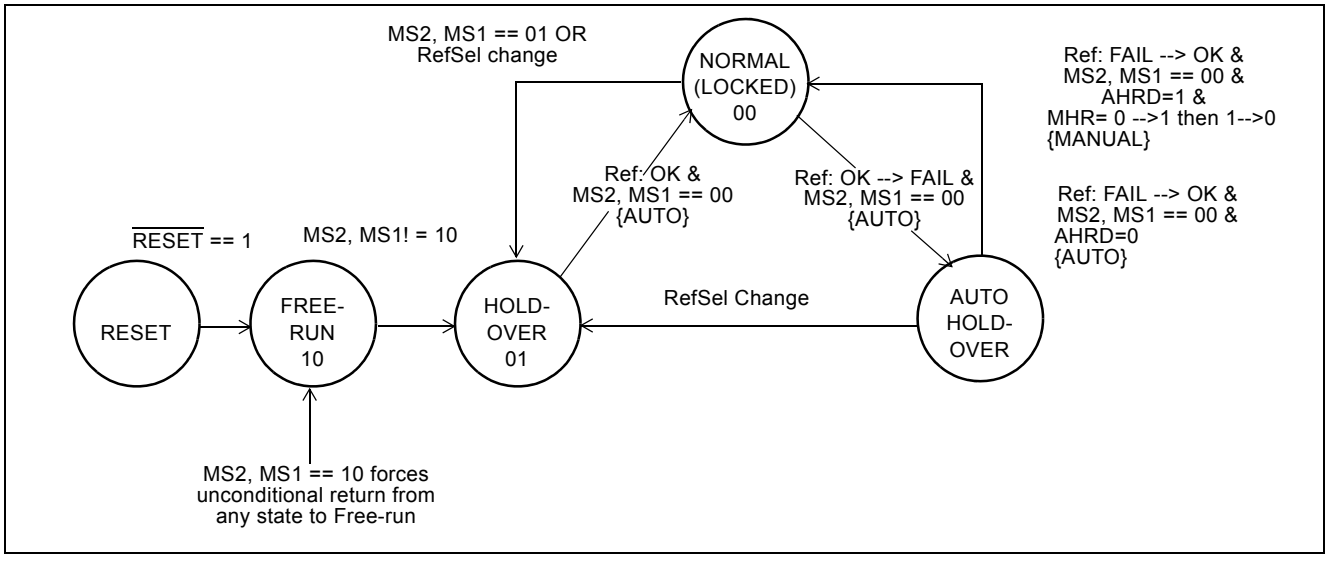


Figure 7 - Transition from Free-Run to Normal Mode

5.1.2 Single Reference Operation: NORMAL --> AUTO HOLDOVER --> NORMAL

The NORMAL to AUTO-HOLDOVER to NORMAL transition will usually happen when the Network Element loses its single reference clock unexpectedly or when it has two references but switching to the secondary reference is not a desirable option (unless primary reference is lost without chance of quick recovery).

The sequence starts with the unexpected failure of a reference signal shown as transition OK --> FAIL in Figure 7 "Transition from Free-Run to Normal Mode" at a time when ZL30402 operates in Normal mode. This failure is detected by the active Acquisition PLL based on the following FAIL criteria:

- Frequency offset on 8 kHz, 1.544 MHz, 2.048 MHz and 19.44 MHz reference clocks exceeds ±30000 ppm (±3%).
- Single phase hit on 1.544 MHz, 2.048 MHz and 19.44 MHz exceeds half of the cycle of the reference clock.

After detecting any of these anomalies on a reference clock the Acquisition PLL will switch itself into Holdover mode forcing the Core PLL to automatically switch into the Auto Holdover state. This condition is flagged by LOCK = 0 and HOLDOVER = 1.

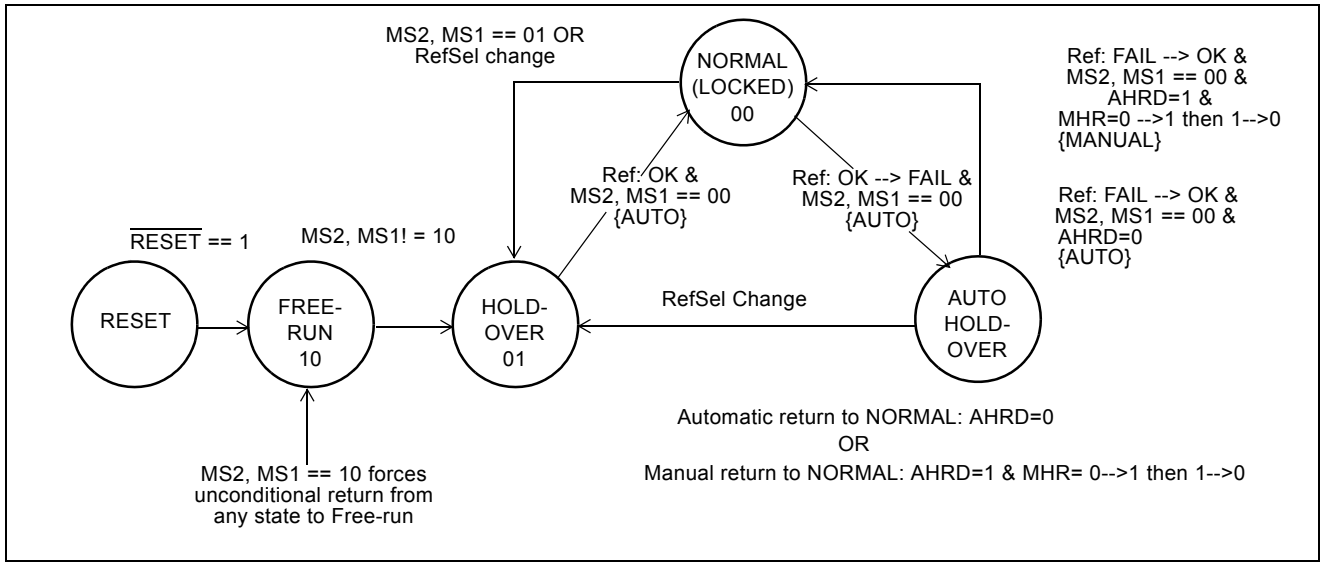


Figure 8 - Automatic Entry into Auto Holdover State and Eecovery into Normal mode

There are two possible returns to Normal mode after the reference signal is restored:

- With the AHRD (Automatic Holdover Return Disable) bit set to 0. In this case the Core PLL will automatically return to the Normal state after the reference signal recovers from failure. This transition is shown on the state diagram as a FAIL --> OK change. This change becomes effective when the reference is restored and there have been no phase hits detected for at least 64 clock cycles for 1.544/2.048 MHz reference, 512 clock cycles for 19.44 MHz reference and 1 clock cycle for 8 kHz reference.
- With the AHRD bit set to high to disable automatic return to Normal and the change of MHR (Manual Holdover Release) bit from 0 to 1 to trigger the transition from Auto Holdover to Normal. This option is provided to protect the Core PLL against toggling between Normal and Auto Holdover states in case of an intermittent quality reference clock. In the case when MHR has been changed when the reference is still not available (Acquisition PLL in Holdover mode) the transition to Normal state will not occur and MHR 0 to 1 transition must be repeated.

This transition from Auto Holdover to Normal mode is performed as “hitless” reference switching.

5.1.3 Dual Reference Operation: NORMAL --> AUTO HOLDOVER--> HOLDOVER --> NORMAL

The NORMAL to AUTO-HOLDOVER to HOLDOVER to NORMAL sequence represents the most likely operation of ZL30402 in Network Equipment.

The sequence starts from the Normal state and transitions to Auto Holdover state due to an unforeseen loss of reference. The failure conditions triggering this transition were described in section 4.1.2. When in the Auto Holdover state, the ZL30402 can return to Normal mode automatically if the lost reference is restored and the ADHR bit is set to 0. If the reference clock failure persists for a period of time that exceeds the system design limit, the system control processor may initiate a reference switch. If the secondary reference is available the ZL30402 will briefly switch into Holdover mode and then transition to Normal mode.

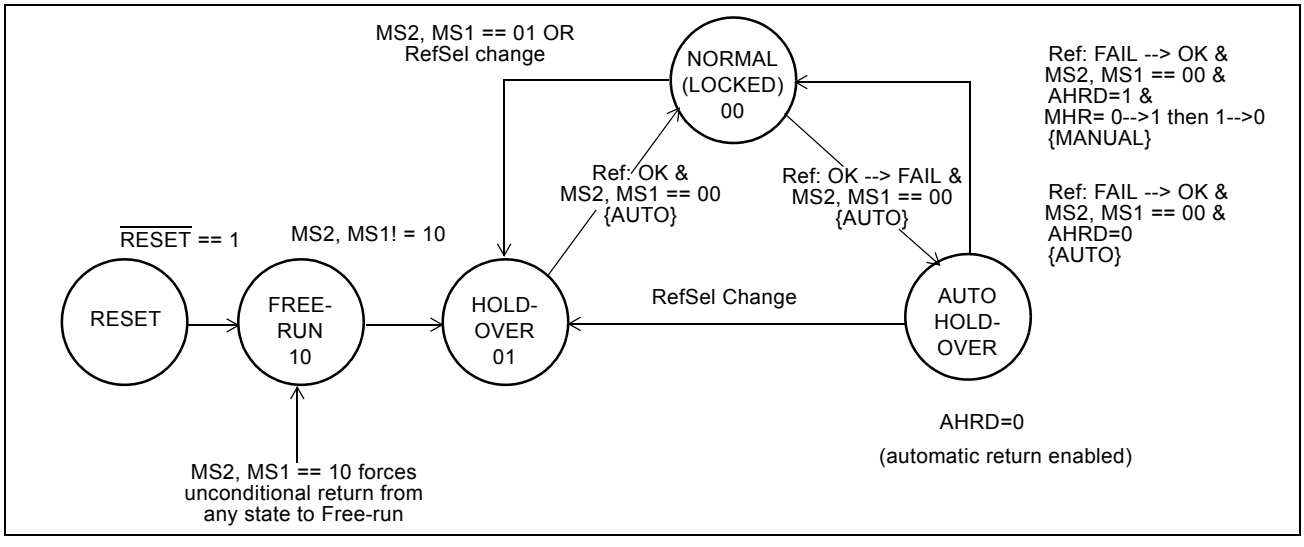


Figure 9 - Entry into Auto Holdover state and recovery into Normal mode by switching references

The new reference clock will most likely have a different phase but it may also have a different fractional frequency offset. In order to lock to a new reference with a different frequency, the Core PLL may be stepped gradually towards the new frequency. The frequency slope will be limited to less than 2.0 ppm/sec.

5.1.4 Reference Switching (RefSel): NORMAL --> HOLDOVER --> NORMAL

The NORMAL to HOLDOVER to NORMAL mode switching is usually performed when:

- A reference clock is available but its frequency drifts beyond some specified limit. In a Network Element with stratum 3 internal clocks, the reference failure is declared when its frequency drifts more than ±12 ppm beyond its nominal frequency.
- During routine maintenance of equipment when orderly switching of reference clocks is possible. This may happen when synchronization references must be rearranged or when a faulty line card must be replaced.

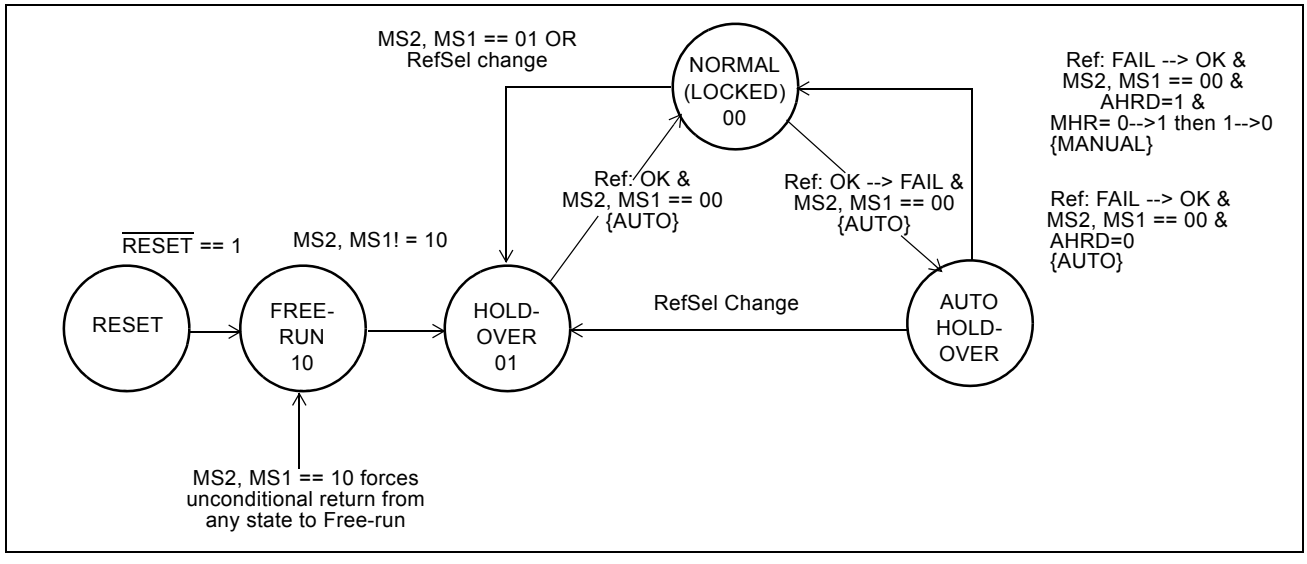


Figure 10 - Manual Reference Switching

Two types of transitions are possible:

- Semi-automatic transition, which involves changing RefSel input to select a secondary reference clock without changing the mode select inputs MS2, MS1 = 00 (Normal mode). This forces ZL30402 to momentarily transition through the Holdover state and automatically return to Normal mode after synchronizing to a secondary reference clock.
- Manual transition, which involves switching into Holdover mode (MS2, MS1 = 01), changing references with RefSel, and manual return to the Normal mode (MS2, MS1 = 00).

In both cases, the change of references provides “hitless” switching.

5.2 Programming Master Clock Oscillator Frequency Calibration Register

The Master Crystal Oscillator and its programmable Master Clock Frequency Calibration register (see Table 18, Table 19, Table 20, and Table 21) have been described in Section 3.0 "Master Clock Frequency Calibration Circuit", on page 16. Programming of this register should be done after system has been powered long enough for the Master Crystal Oscillator to reach a steady operating temperature. When the temperature stabilizes the crystal oscillator frequency should be measured with an accurate frequency meter. The frequency measurement should be substituted for the f_{offset} variable in the following equation.

$$MCFC = 45036 * (- f_{offset})$$

where f_{offset} is the crystal oscillator frequency offset from the nominal 20 000 000 Hz frequency expressed in Hz.

Example 1: Calculate the binary value that must be written to the MCFC register to correct a -1ppm offset of the Master Crystal Oscillator. The -1ppm offset for a 20 MHz frequency is equivalent to -20 Hz:

MCFC = 45036 * 20 = 900720 = 00 0D BE 70 H

Note: Correcting the -1ppm crystal offset requires +1ppm MCFC offset.

Example 2: Calculate the binary value that must be written to the MCFC register to correct a +2 ppm offset of the Master Crystal Oscillator. The +2 ppm offset for 20 MHz frequency is equivalent to 40 Hz:

MCFC = 45036 * (-40) = -1801440 = FF E4 83 20 H

6.0 Characteristics

6.1 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DDR}	-0.3	7.0	V
2	Voltage on any pin	V_{PIN}	-0.3	VDD+0.3	V
3	Current on any pin	I_{PIN}		30	mA
4	Storage temperature	T_{ST}	-55	125	°C
5	Package power dissipation (80 pin LQFP)	P_{PD}		1000	mW
6	ESD rating	V_{ESD}		1500	V

* Voltages are with respect to ground (GND) unless otherwise stated
* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions*

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD}	3.0	3.3	3.6	V
2	Operating temperature	T_A	-40	25	+85	°C

* Voltages are with respect to ground (GND) unless otherwise stated

DC Electrical Characteristics*

	Characteristics	Symbol	Min.	Max.	Units	Notes
1	Supply current with C20i = 20 MHz	I_{DD}		135	mA	Outputs unloaded
2	Supply current with C20i = 0V	I_{DDS}		2.2	mA	Outputs unloaded
3	CMOS high-level input voltage	V_{CIH}	$0.7V_{DD}$		V	
4	CMOS low-level input voltage	V_{CIL}		$0.3V_{DD}$	V	
5	Input leakage current	I_{IL}		15	µA	$V_I=V_{DD}$ or GND
6	High-level output voltage	V_{OH}	2.4		V	I_{OH}=10 mA
7	Low-level output voltage	V_{OL}		0.4	V	I_{OL}=10 mA
8	LVDS: Differential output voltage	V_{OD}	250	450	mV	Z_T=100 Ω
9	LVDS: Change in VOD between complementary output states	dV_{OD}		50	mV	Z_T=100 Ω
10	LVDS: Offset voltage	V_{OS}	1.125	1.375	V	Note 1
11	LVDS: Change in VOS between complementary output states	dV_{OS}		50	mV	
12	LVDS: Output short circuit current	I_{OS}		24	mA	Pin short to GND
13	LVDS: Output rise and fall times	T_{RF}	260	900	ps	Note 2

* Voltages are with respect to ground (GND) unless otherwise stated

Note 1: V_{OS} is defined as $(V_{OH} + V_{OL}) / 2$
Note 2: Rise and fall times are measured at 20% and 80% levels.

AC Electrical Characteristics - Timing Parameter Measurement - CMOS Voltage Levels*

	Characteristics	Symbol	Level	Units
1	Threshold voltage	V_T	$0.5V_{DD}$	V
2	Rise and fall threshold voltage High	V_{HM}	$0.7V_{DD}$	V
3	Rise and fall threshold voltage Low	V_{LM}	$0.3V_{DD}$	V

* Voltages are with respect to ground (GND) unless otherwise stated
* Supply voltage and operating temperature are as per Recommended Operating Conditions
* Timing for input and output signals is based on the worst case conditions (over T_A and V_{DD})

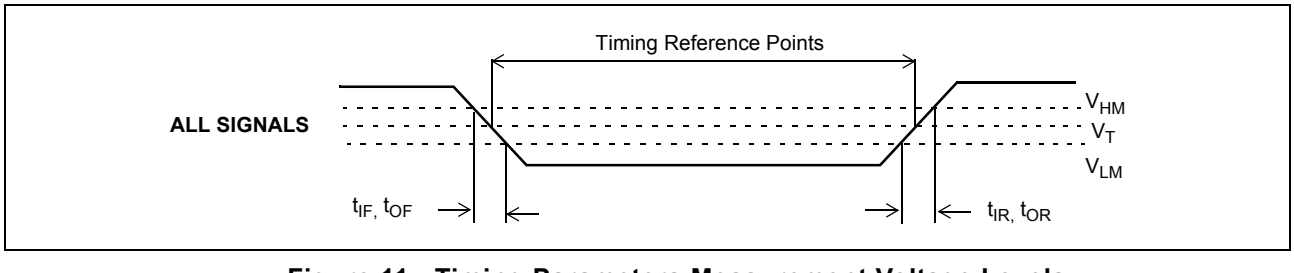


Figure 11 - Timing Parameters Measurement Voltage Levels

AC Electrical Characteristics - Microprocessor Timing*

	Characteristics	Symbol	Min.	Max.	Units	Notes
1	$\overline{DS}$ Low	t_{DSL}	65		ns	
2	$\overline{DS}$ High	t_{DSH}	100		ns	
3	$\overline{CS}$ Setup	t_{CSS}	0		ns	
4	$\overline{CS}$-Hold	t_{CSH}	0		ns	
5	R/$\overline{W}$ Setup	t_{RWS}	20		ns	
6	R/$\overline{W}$ Hold	t_{RWH}	5		ns	
7	Address Setup	t_{ADS}	10		ns	
8	Address Hold	t_{ADH}	10		ns	
9	Data Read Delay	t_{DRD}		60	ns	C_L=90 pF
10	Data Read Hold	t_{DRH}		10	ns	
11	Data Write Setup	t_{DWS}	10		ns	
12	Data Write Hold	t_{DWH}	5		ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions

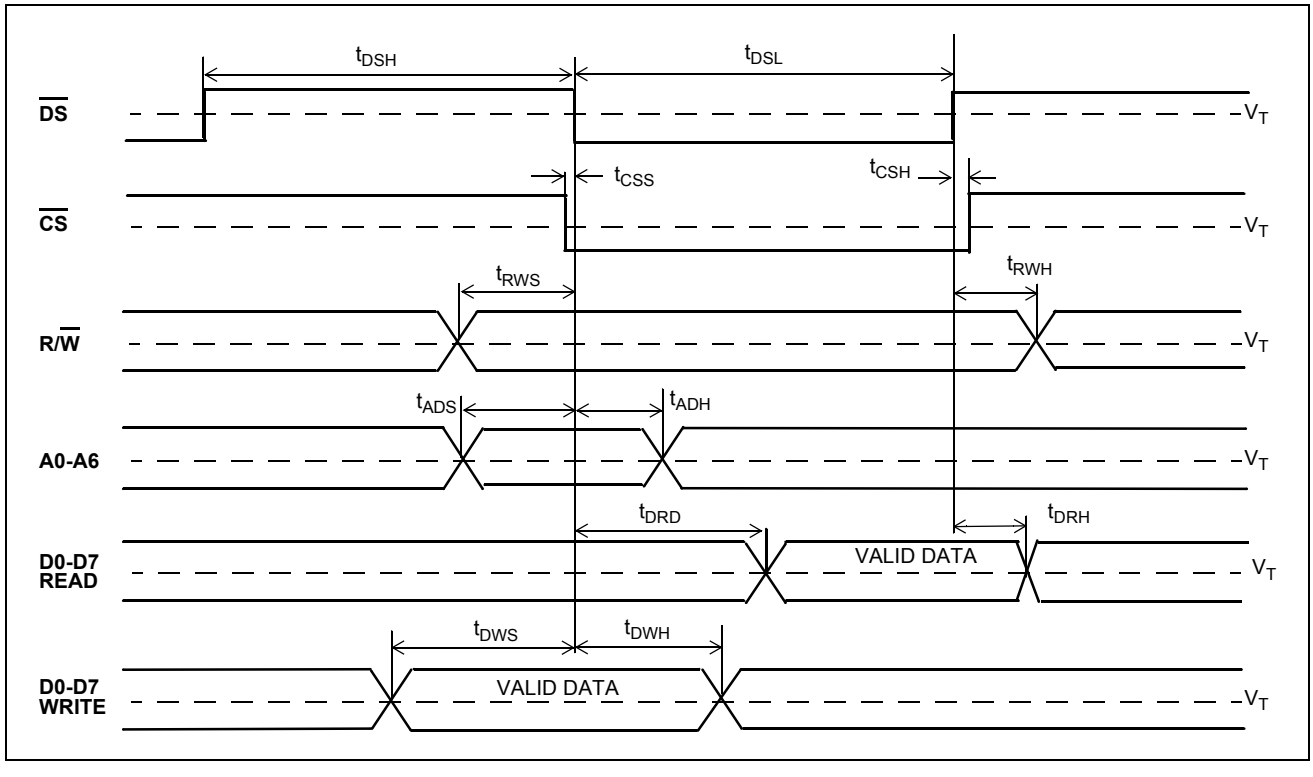


Figure 12 - Microport Timing

AC Electrical Characteristics - ST-BUS and GCI Output Timing*

	Characteristics	Symbol	Min.	Max.	Units	Notes
1	$\overline{F16o}$ pulse width low (nom 61ns)	t_{F16L}	52	61	ns	
2	F8o to $\overline{F16o}$ delay	t_{F16D}	19	27	ns	
3	$\overline{C16o}$ pulse width low	t_{C16L}	19	35	ns	
4	$\overline{C16o}$ to F8o delay	t_{C16D}	-2	6	ns	
5	F8o pulse width high (nom 122 ns)	t_{F8H}	118	128	ns	
6	C8o pulse width low	t_{C8L}	54	65	ns	
7	C8o to F8o delay	t_{C8D}	-2	6	ns	
8	$\overline{F0o}$ pulse width low (nom 244)	t_{F0L}	236	248	ns	
9	F8o to $\overline{F0o}$ delay	t_{F0D}	115	123	ns	
10	$\overline{C4o}$ pulse width low	t_{C4L}	114	126	ns	
11	$\overline{C4o}$ to F8o delay	t_{C4D}	2	8	ns	
12	C2o pulse width low	t_{C2L}	235	250	ns	
13	C2o to F8o delay	t_{C2D}	-2	6	ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions

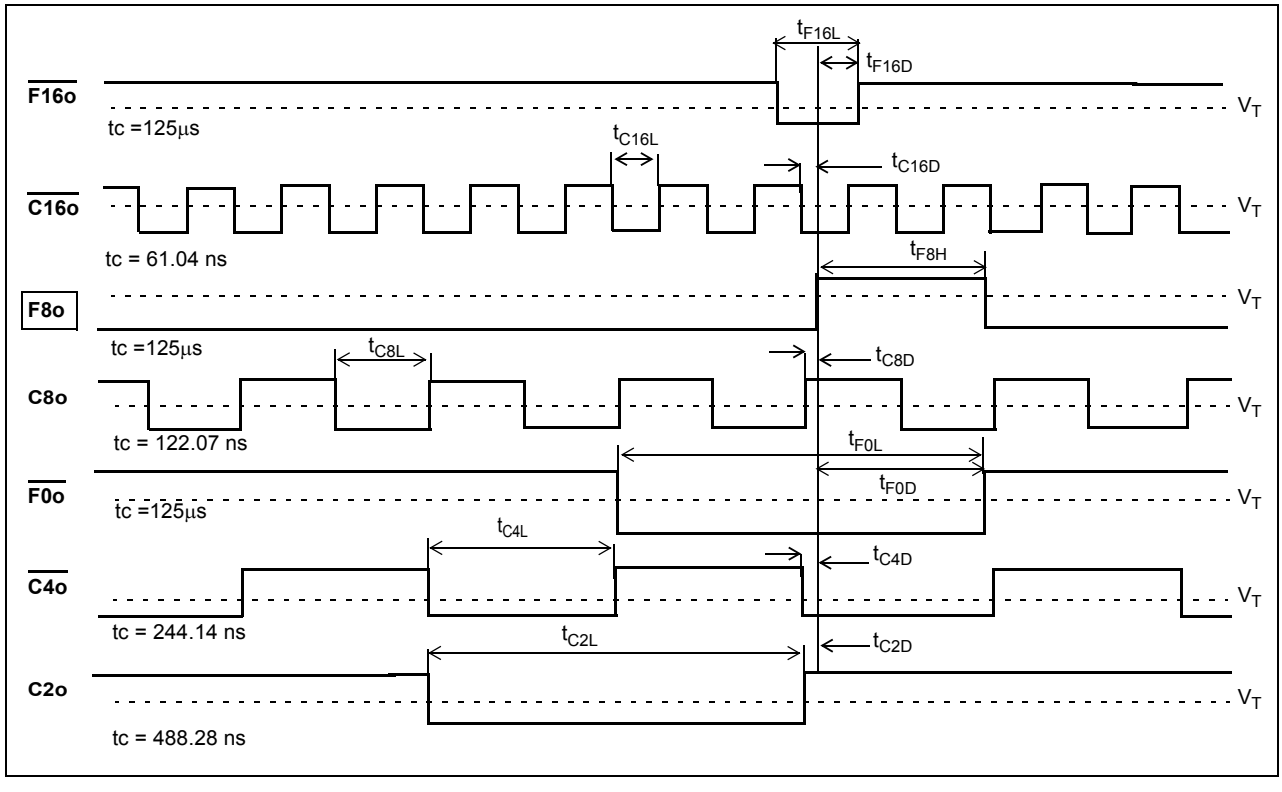


Figure 13 - ST-BUS and GCI Output Timing

AC Electrical Characteristics - DS1, DS2 and C19o Clock Timing*

	Characteristics	Symbol	Min.	Max.	Units	Notes
1	C6o pulse width low	t_{C6L}	70	83	ns	
2	F8o to C6o delay	t_{C6D}	80	95	ns	
3	C1.5o pulse width low	$t_{C1.5L}$	315	330	ns	
4	C1.5o to F8o delay	$t_{C1.5D}$	55	75	ns	
5	C19o pulse width high	t_{C19H}	19	35	ns	
6	C19o to F8o delay	t_{C19D}	8	14	ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions

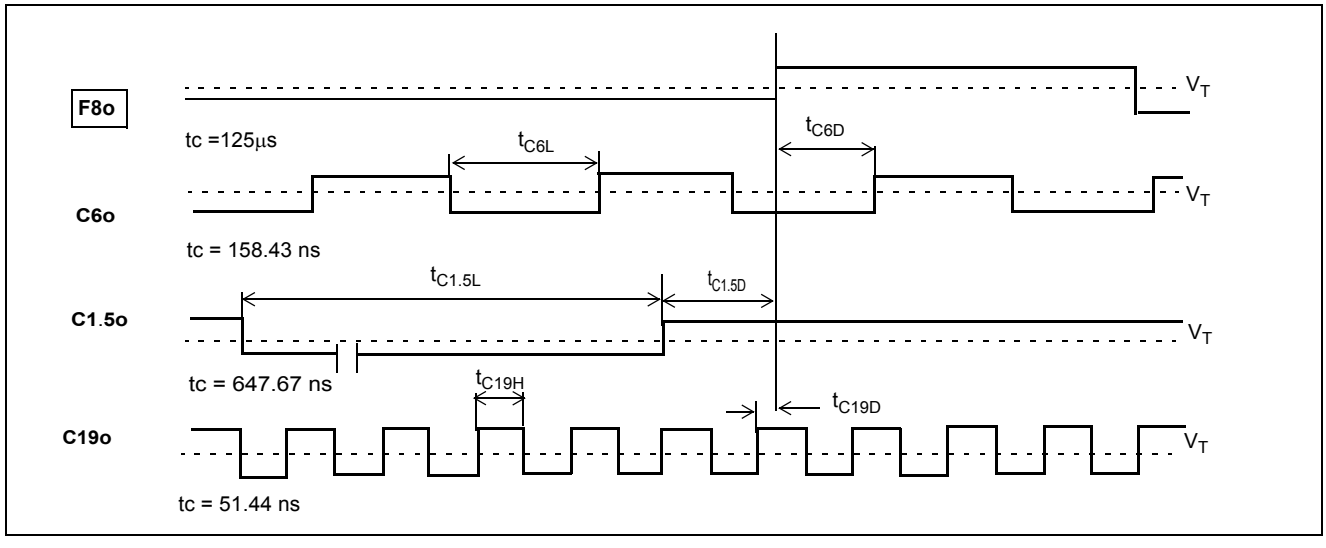


Figure 14 - DS1, DS2 and C19o Clock Timing

AC Electrical Characteristics - C155o and C19o Clock Timing

	Characteristics	Symbol	Min.	Max.	Units	Notes
1	C155o pulse width low	t_{C155L}	2.7	3.7	ns	
2	C155o to C19o rising edge delay	$t_{CF19DLH}$	-10	5	ns	
3	C155o to C19o falling edge delay	$t_{CF19DHL}$	-7	7	ns	
4	C19 pulse width high	t_{CF19H}	22	33		

* Supply voltage and operating temperature are as per Recommended Operating Conditions

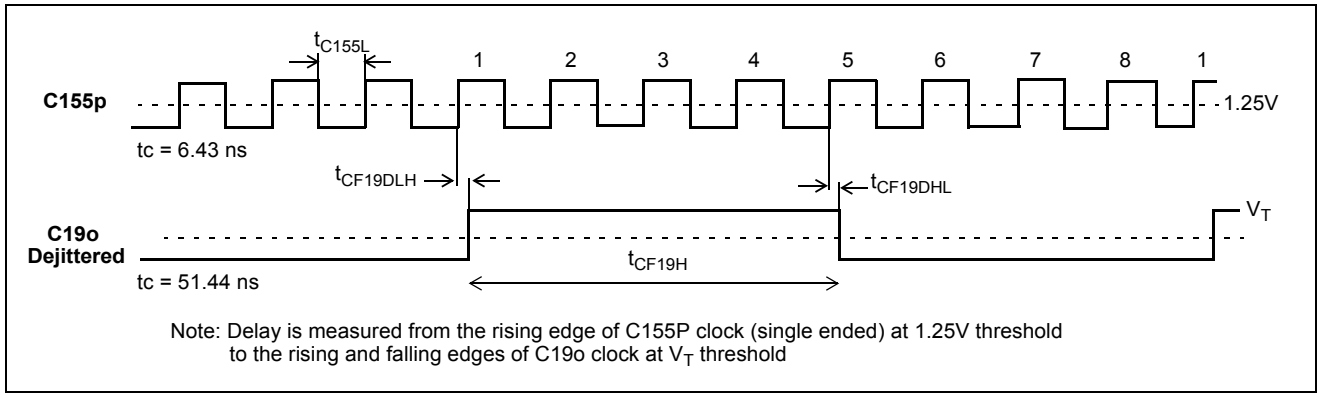


Figure 15 - C155o and C19o Timing

AC Electrical Characteristics - Input to Output Phase Alignment (after $\overline{\text{RefAlign}}$ change from 1 to 0)*

	Characteristics	Symbol	Min.	Max.	Units	Notes
1	8 kHz ref pulse width high	t_{R8H}	100		ns	
2	F8o to 8 kHz ref input delay	t_{R8D}	-15	115	ns	Note 1
3	1.544 MHz ref pulse width high	$t_{R1.5H}$	100		ns	
4	1.544 MHz ref input to F8o delay	$t_{R1.5D}$	210	220	ns	
5	2.048 MHz ref pulse width high	t_{R2H}	100		ns	
6	2.048 MHz ref input to F8o delay	t_{R2D}	192	202	ns	
7	19.44 MHz ref pulse width high	t_{R19H}	20		ns	
8	F8o to 19.44 MHz ref input delay	t_{R19D}	5	14	ns	
9	19.44 MHz ref input to C19o delay	$t_{R19C19D}$	-4	4	ns	
10	Reference input rise and fall time	t_{IR}, t_{IF}		10	ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions
Note 1: For 8 kHz reference alignment refer to Application Note ZL-27 "Phase Alignment between 8 kHz Output and 8 kHz Input Reference on ZL30402"

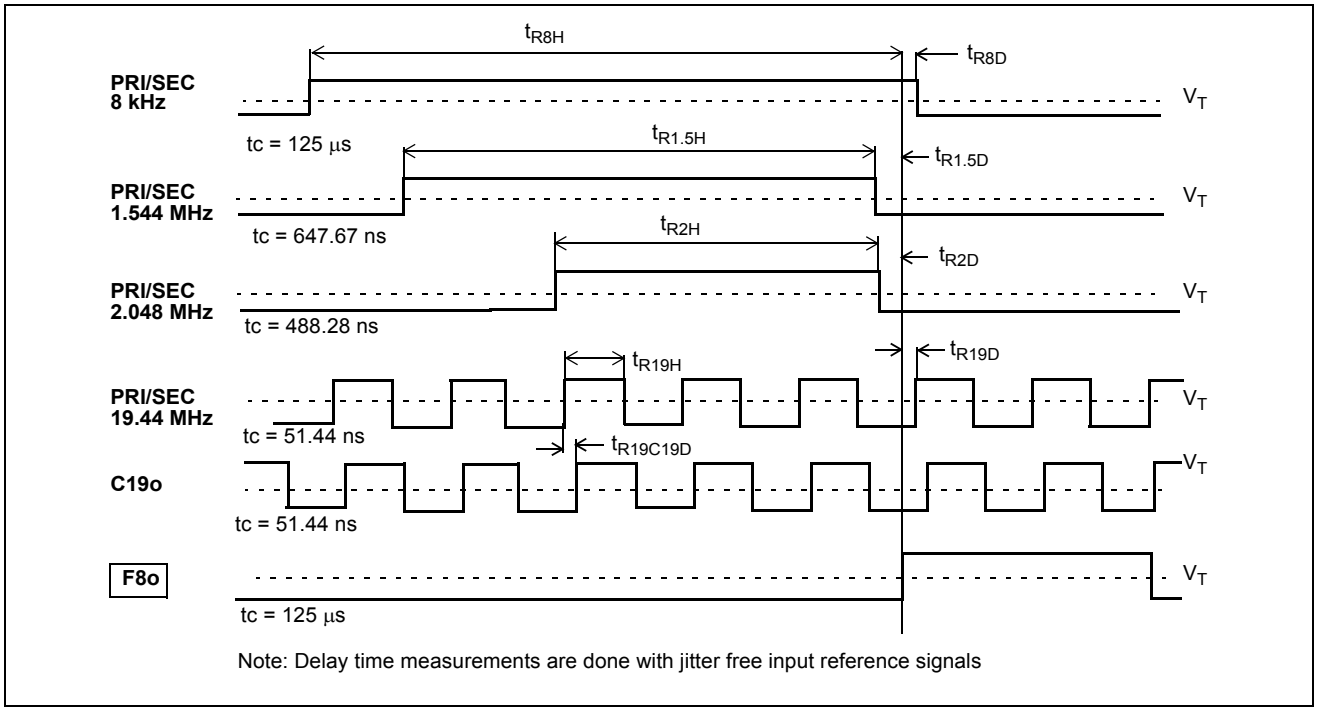


Figure 16 - Input Reference to Output Clock Phase Alignment

AC Electrical Characteristics - Input Control Signals*

	Characteristics	Symbol	Min.	Max.	Units	Notes
1	Input controls Setup time	t_S	100		ns	
2	Input controls Hold time	t_H	100		ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

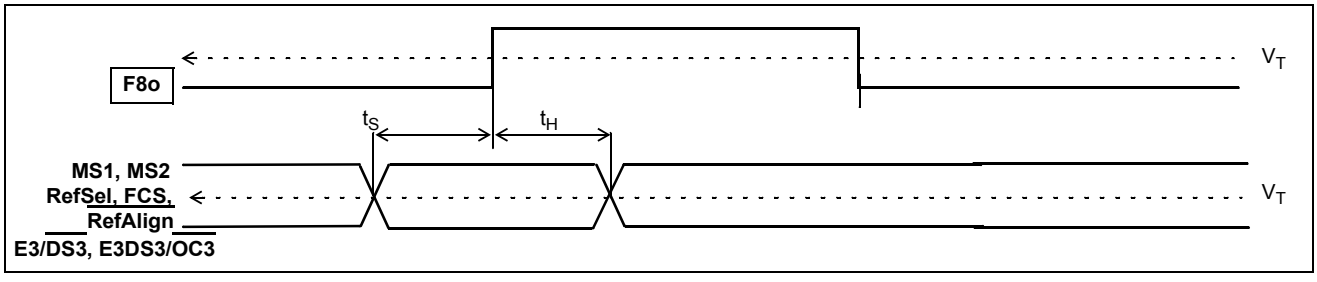


Figure 17 - Input Control Signal Setup and Hold Time

AC Electrical Characteristics - E3 and DS3 Output Timing*

	Characteristics	Symbol	Min.	Max.	Units	Notes
1	C44o clock pulse width high	t_{C44H}	8	12	ns	
2	C11o clock pulse width high	t_{C11H}	8	40	ns	
3	C34o clock pulse width high	t_{C34H}	12	15	ns	
4	C8.5o clock pulse width high	$t_{C8.5L}$	7	40	ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions

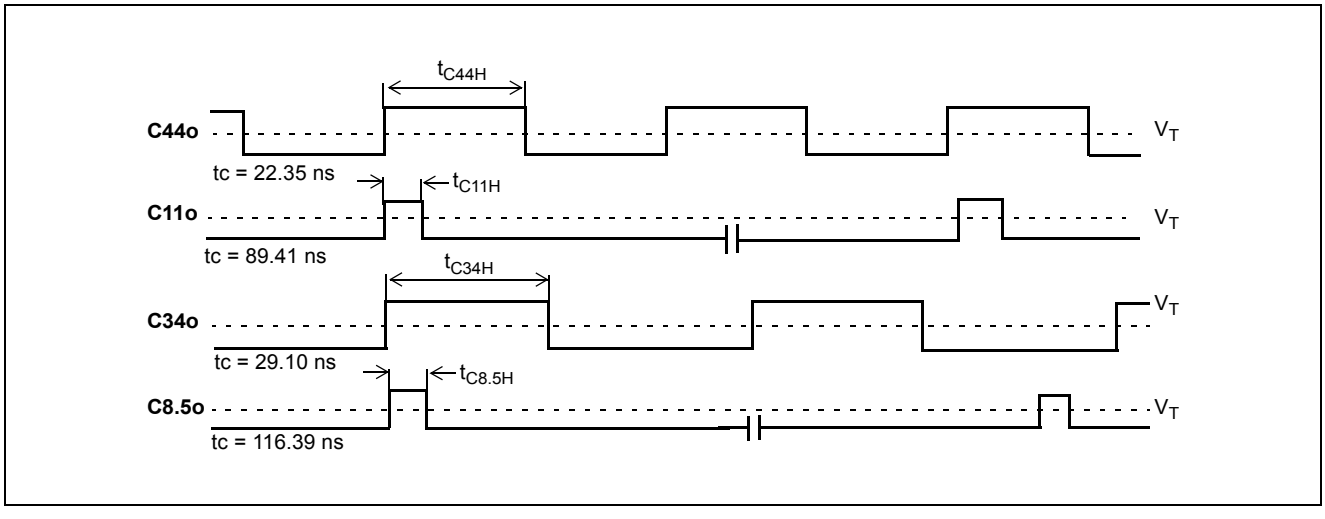


Figure 18 - E3 and DS3 Output Timing

6.2 Performance Characteristics

Performance Characteristics*

	Characteristics	Typical	Units	Notes
1	Holdover accuracy	0.000001	ppm	
2	Holdover stability	NA	ppm	Determined by stability of 20MHz frequency source
3	Capture range	±104	ppm	
	Lock time			
4	1.1Hz Filter	70	s	±4.6ppm frequency offset
5	0.1Hz Filter	70	s	±4.6ppm frequency offset
	Output Phase variation			
6	Reference switching: PRI ⇐ SEC, SEC ⇐ PRI	50	ns	
7	Switching from Normal mode to Holdover mode	0	ns	
8	Switching from Holdover mode to Normal mode	50	ns	
	Output Phase Slope			
9	G.813 Option 1, GR-1244 stratum 3	41	1.326ms	
10	G.813 Option 2 GR-253 SONET stratum 3 GR-253 SONET SMC	885	ns/s	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics - Jitter Generation (Intrinsic Jitter) - Filtered*

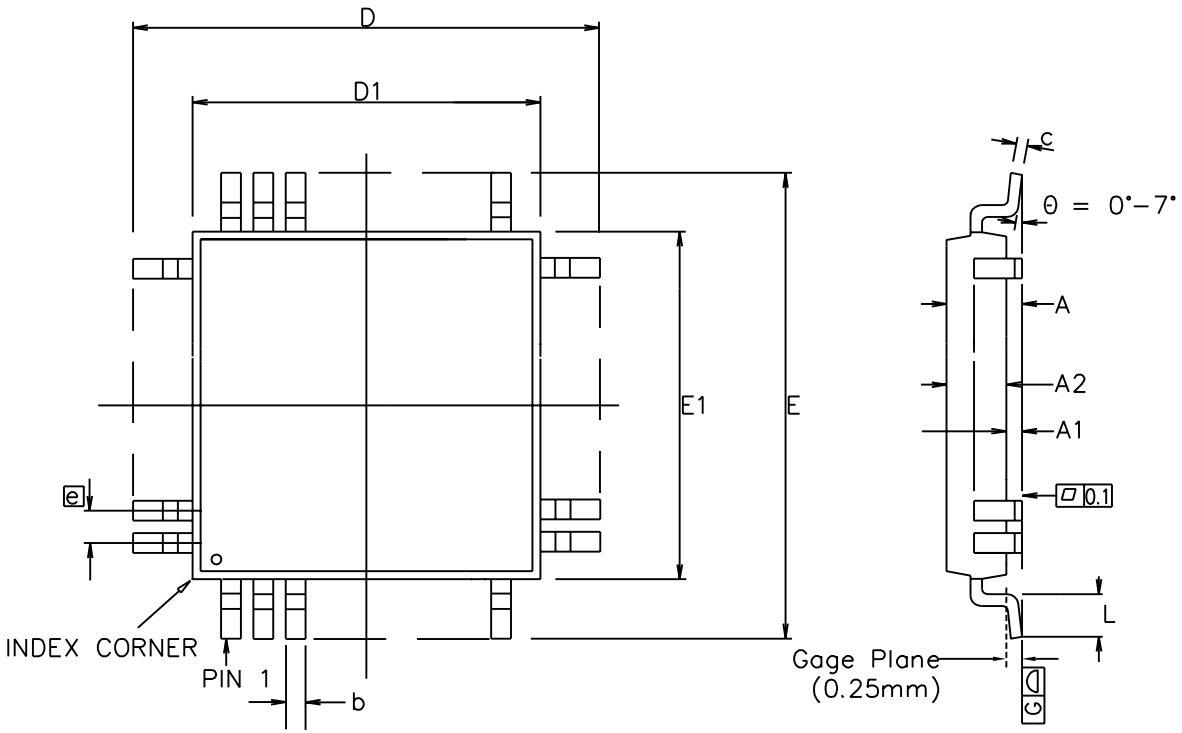
	Characteristics	Max UIpp	Max ns-pp	Notes
1	C1.5o (1.544 MHz)	0.004	2.75	Filter: 10 Hz - 40 kHz
2	C2o (2.048 MHz)	0.004	1.80	Filter: 20 Hz - 100 kHz
3	C19o (19.44 MHz) Dejittered	0.017	0.86	Filter: 100 Hz - 400 kHz OC-1
4	C19o (19.44 MHz) Dejittered	0.014	0.73	Filter: 20 kHz - 400 kHz OC-1
5	C19o (19.44 MHz) Dejittered	0.024	1.24	Filter: 500 Hz - 1.3 MHz OC-3
6	C19o (19.44 MHz) Dejittered	0.021	1.08	Filter: 65 kHz - 1.3 MHz OC-3
7	C19o (19.44 MHz)	0.026	1.34	Filter: 100 Hz - 400 kHz OC-1
8	C19o (19.44 MHz)	0.018	0.94	Filter: 20 kHz - 400 kHz OC-1
9	C19o (19.44 MHz)	0.035	1.78	Filter: 500 Hz - 1.3 MHz OC-3
10	C19o (19.44 MHz)	0.025	1.30	Filter: 65 kHz - 1.3 MHz OC-3
11	C34o (34.368 MHz)	0.038	1.11	Filter: 100 Hz - 800 kHz
12	C34o (34.368 MHz)	0.037	1.06	Filter: 10 kHz - 800 kHz
13	C44o (44.736 MHz)	0.032	0.72	Filter: 10 Hz - 400 kHz
14	C44o (44.736 MHz)	0.023	0.51	Filter: 30 kHz - 400 kHz
15	C155o (155.52 MHz)	0.106	0.68	Filter: 100 Hz - 400 kHz OC-1
16	C155o (155.52 MHz)	0.091	0.58	Filter: 20 kHz - 400 kHz OC-1
17	C155o (155.52 MHz)	0.145	0.93	Filter: 500 Hz - 1.3 MHz OC-3
18	C155o (155.52 MHz)	0.127	0.82	Filter: 65 kHz - 1.3 MHz OC-3

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics - Jitter Generation (Intrinsic Jitter) - Unfiltered*

	Characteristics	Max UIpp	Max ns-pp	Notes
1	C1.5o (1.544 MHz)	0.010	6.5	
2	C2o (2.048 MHz)	0.010	5.8	
3	C4o- (4.096 MHz)	0.020	4.8	
4	C6o (6.312 MHz)	0.033	5.2	
5	C8o (8.192 MHz)	0.042	5.2	
6	C8.5o (8.592 MHz)	0.028	3.3	
7	C11o (11.184 MHz)	0.031	2.8	
8	C16o- (16.384 MHz)	0.090	5.5	
9	C19o (19.44 MHz)	0.038	2.0	Dejittered with Analog PLL
10	C19o (19.44 MHz)	0.059	3.0	Analog PLL bypassed
11	C34o (34.368 MHz)	0.092	2.7	
12	C44o (44.736 MHz)	0.110	2.5	
13	C155o (155.52 MHz)	0.170	1.1	
14	F0o (8 kHz)	NA	4.7	
15	F8o (8 kHz)	NA	4.0	
16	F16o (8 kHz)	NA	3.1	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	– – –	1.60		0.002	0.063
A1	0.05	0.15		0.010	0.006
A2	1.35	1.45		0.053	0.057
D	16.00 BSC			0.630 BSC	
D1	14.00 BSC			0.551 BSC	
E	16.00 BSC			0.630 BSC	
E1	14.00 BSC			0.551 BSC	
L	0.45	0.75		0.018	0.030
e	0.65 BSC			0.026 BSC	
b	0.22	0.38		0.009	0.015
c	0.09	0.20		0.004	0.008
	Pin features				
N	80				
ND	20				
NE	20				
NOTE	SQUARE				

Conforms to JEDEC MS–026 BEC Iss. C

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould prorusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.10 mm max.

This drawing supersedes 418/ED/51210/024 (Swindon)

ISSUE	1	2	3	
ACN	201363	207143	212836	
DATE	28Oct96	14Jul99	21May02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
GP / B

Package Code QC

Package Outline for 80 lead LQFP (14 x 14 x 1.4mm) 2.0mm Footprint

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