FURUNO GNSS Receiver

Model GN-8720

Hardware Specifications

(Document No. SE16-410-005-02)

FURUNO ELECTRIC CO., LTD.

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- GLONASS (Russia)
- Galileo(Europe)
- QZSS(Japan)
- SBAS(USA: WAAS, Europe: EGNOS, Japan: MSAS)

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Revision History

Version	Changed contents	Date
0	Initial release	2016.07.08
1	Corrected the description order of GNSS reception capability in Table 2.1. Added Notes 5) in Chapter 2. Corrected PU/PD for TXD2 in Table 5.1. Added Notes for equivalent pull-up/pull-down resistor in Table 6.3. Added Section 6.3.2. Corrected the equivalent circuit for TXD2 in Table 8.1. Updated the reference document in Chapter 15.	2016.09.30
2	Updated Section 6.3.2.	2016.10.07

Table of Contents

1 Outline

GN-8720 is a stand-alone, complete GNSS receiver module. Main features are as follows:

- Supports GPS, GLONASS, SBAS, QZSS and Galileo
- Outputs a time pulse (1PPS) synchronized to UTC time
- Software upgrade capability by Flash ROM
- Active Anti-jamming capability to suppress effects of CW jammers
- Multi path mitigation effects
- Works in both Autonomous mode and Assisted mode
- GPS/GLONASS high indoor sensitivity
- Fast TTFF of typically <1 second when in hot and 30 seconds in warm and 33 seconds in cold start conditions
- Available of active and passive antenna
- Low profile, small SMT package reducing the mounting area and mounting cost

2 GNSS General Specifications

Table 2.1 General Specifications

Items	Description		Notes
△1 GNSS reception capability[1)2)]	GPS L1C/A	12	
	GLONASS L1OF[3)]	10	
	Galileo E1B/E1C[4)5)]	8	
	QZSS L1C/A	2	
	SBAS L1C/A	2	PRN number is 120 to 138 of WAAS, MSAS, EGNOS, GAGAN
GNSS concurrent reception[1)]	GPS, GLONASS, Galileo, QZSS, SBAS	32	
Environment robustness performance	Active Anti-jamming	8CW	
	Multipath Mitigation	●	
Extended Ephemeris	Self assisted for GPS	3 days	Flash ROM base
	Server based for GPS	7 days	
Data update rate	GNSS	Up to 10Hz	
Serial data format	NMEA[6)]	●	
	FURUNO Binary[6)]	●	
Antenna	Active antenna	●	
	Passive antenna	●	
Operational limits	Altitude	18,300m	Based on Wassenaar arrangement specification
	Velocity	515 m/s	

Notes:

1) Update rate is 1Hz.
2) Satellite systems are selectable from GPS, GLONASS, Galileo, SBAS and QZSS. GPS, GLONASS and/or Galileo are required for positioning.
3) When a leap second is inserted during GLONASS only positioning after COLD Start with GLONASS only, positioning may become impossible.
4) When a leap second is inserted during Galileo only positioning, the outputted UTC time is one second fast/behind.
△1 5) GN-8720 was developed based on the Galileo Open Service Signal-In-Space Interface Control Document Issue 1.1 (OS SIS ICD v1.1). Software updates may be required due to change contents of the Galileo OS SIS ICD v1.1.
OS SIS ICD, Issue 1.1, September 2010© European Union 2010
6) See the protocol specifications for details.

3 GNSS General Performance

Table 3.1 General Performance

T_A=25°C

Items	Description		Notes
TTFF	Hot Outdoor[1)]	<1 s	These are specified with the measurement platform shown in Figure 3.1. Simulator output level is set to -130 dBm.
	Warm Outdoor	30 s	
	Cold Outdoor	33 s	
	Hot Indoor	9 s	These are specified with the measurement platform shown in Figure 3.1. Simulator output level is set to -150 dBm.
GPS sensitivity[2)]	Tracking	-161 dBm	These are specified with the measurement platform shown in Figure 3.1.
	Hot Acquisition	-161 dBm	
	Cold Acquisition	-147 dBm	
	Reacquisition	-161 dBm	
GLONASS sensitivity[2)]	Tracking	-157 dBm	
	Hot Acquisition	-157 dBm	
	Cold Acquisition	-143 dBm	
	Reacquisition	-157 dBm	
Galileo sensitivity[2)]	Tracking	-145 dBm	
	Hot Acquisition	-135 dBm	
	Cold Acquisition	-135 dBm	
	Reacquisition	-135 dBm	
QZSS sensitivity[2)]	Tracking	-146 dBm	
SBAS sensitivity[2)]	Tracking	-138 dBm	
Position accuracy[2)]	Horizontal Outdoor	2.5m CEP	GPS only Open sky 24 hours with recommended antenna
		2.0m CEP	GPS, GLONASS and SBAS Open sky 24 hours with recommended antenna
	Horizontal Indoor	19m CEP	These are specified with the measurement platform shown in Figure 3.1. Simulator output level is set to -150 dBm.
PPS accuracy[2)]	1σ	10 µs	Open sky, static with recommended antenna

Notes:
1) Time to fix from the Hot start command input at fixsession off state when GPS is used in position fix.
2) Update rate is 1Hz.

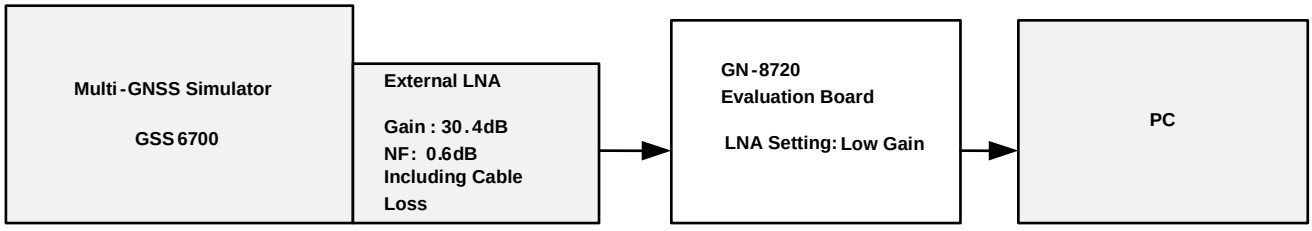


Figure 3.1 Measurement Platform

4 Functional Overview

GN-8720 is a stand-alone, complete GNSS receiver module that can provide accurate GNSS PVT (Position, Velocity & Time) information through serial communication channel. The key device inside is *eRide*OPUS 7, the latest monolithic GNSS receiver chip that contains ARM9™ processor for signal tracking and processing, high performance integrated LNA, PLL Synthesizer, Down-converter, ADC and DSP. GN-8720 also contains Flash ROM for firmware and data storage, TCXO for reference clock, 32 kHz crystal for RTC (Real time clock), L1 band SAW filter and power-on reset circuit. The block diagram is shown in Figure 4.1.

GN-8720 has power-on reset function inside. It detects VCC input voltage, and sets internal power-on reset signal (POR_N) to logic L when the voltage is lower than power-on reset threshold voltage shown in Table 6.4. GN-8720 also has external reset signal input, RST_N, which allows to force GN-8720 reset by external control. RST_N and POR_N are Wired-OR to create internal reset signal for initializing whole module.

FLNA pin has a special function to configure LNA gain. In case this pin is connected to VCC, internal LNA is set to low gain mode. And in case of no connection (open), high gain mode is selected. So for active antenna, this pin should be connected to VCC, and for passive antenna open.

ANT_DET0/ANT_DET1 pins are used to feed the status of active antenna connection to ARM™ subsystem from the antenna current detection circuit placed outside of GN-8720. These signals can show three (3) states of antenna connection; normal, open (low current) and short (high current). For details, please refer “FURUNO GPS/GNSS Receiver 86/87 series User's Design Guide (SE13-900-001)”.

Reserved pins have pull-up or pull-down resistors inside adequately, so please do not connect anything.

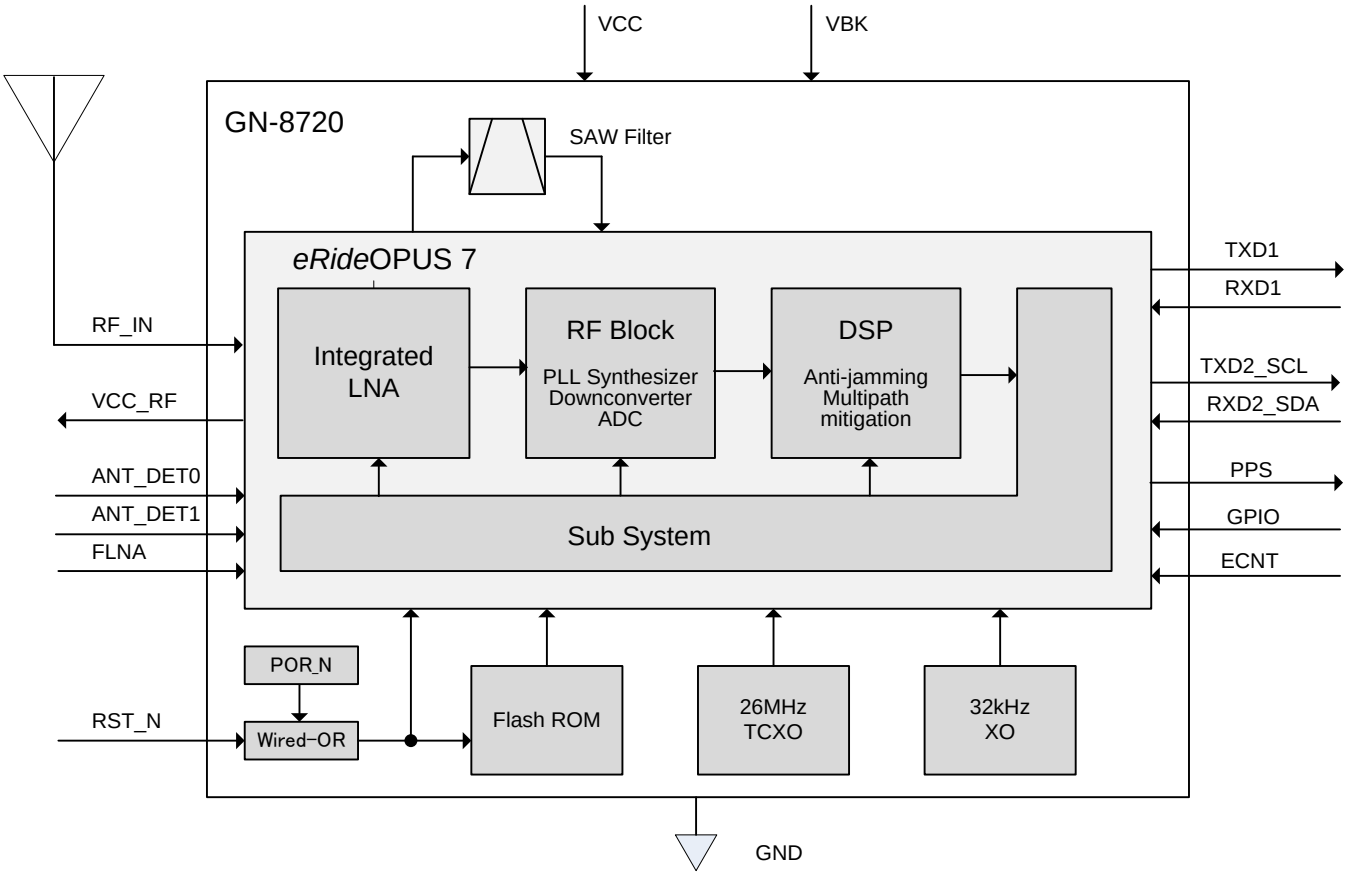


Figure 4.1 Block Diagram

5 I/O Signal Description

Table 5.1 I/O Signal Description

#	Pin Name	Type	PU/PD[1)]	Description
1	RESERVED	-	-	Do not connect anything
2	FLNA	Digital Input	Pull-down	LNA gain select pin Logic L (leave open) : High Gain Logic H (connect to VCC) : Low Gain
3	PPS	Digital Output	Pull-down	PPS output pin Do not pull-up externally[2)]
4	RESERVED	-	-	Do not connect anything
5	ANT_DET1	Digital Input	Pull-up	Antenna detection input pins[3)]
6	ANT_DET0	Digital Input	Pull-up	
7	RESERVED	-	-	Do not connect anything
8	RST_N	Digital Input/Output	Pull-up	External reset signal input pin Logic L : Reset Logic H (Open)[4)] : Normal operation
9	VCC_RF	Power Output	-	Power supply output pin for active antenna
10	GND	-	-	Ground
11	RF_IN	Analog Input	-	GNSS signal input pin
12	GND	-	-	Ground
13	GND	-	-	Ground
14	RESERVED	-	-	Do not connect anything
15	RESERVED	-	-	Do not connect anything Do not pull-up externally[2)]
16	RESERVED	-	-	Do not connect anything
17	RESERVED	-	-	Do not connect anything
18	RXD2	Digital Input	Pull-up	UART2 reception port
19	TXD2	Digital Output	Pull-up △1	UART2 transmission port
20	TXD1	Digital Output	-	UART1 transmission output pin
21	RXD1	Digital Input	Pull-up	UART1 reception input pin
22	VBK	Power Input	-	Backup power supply input pin Leave open if battery backup function is not used
23	VCC	Power Input	-	Main power supply input pin
24	GND	-	-	Ground

Notes:
1) Pull-up and pull-down resistor values are shown in Table 6.3.
2) These pins have pull-down resistors inside to ensure power-on configuration, so it is prohibited to connect any pull-up resistor at the outside of the module.
3) For details, see FURUNO GPS/GNSS Receiver 86/87 series User's Design Guide (SE13-900-001).
4) RST_N is Wired-OR with internal power-on reset (POR_N) signal, so please drive with open-drain or open-collector device.

6 Electrical Characteristics

6.1 Absolute Maximum Rating

The lists of absolute maximum ratings are specified over operating case temperature shown in Table 7.1. Stresses beyond those listed under those range may cause permanent damage to module.

Table 6.1 Absolute Maximum Rating

Items	Symbol	Min.	Max.	Unit	Notes
Supply voltage	V_{CC_ABS}	-0.3	4.0	V	
Backup supply voltage	V_{BK_ABS}	-0.3	4.0	V	
Digital input (DI) voltage	-	-0.3	4.0	V	
Digital output (DO) current	-	-	±7	mA	
VCC_RF output current	$I_{CC\_RF\_ABS}$		150	mA	
RF_IN input power (High Gain mode)	P_{RFINH_ABS}		-20	dBm	at 1575.42MHz & 1602MHz
			1	dBm	at 900MHz
			1	dBm	at 1800MHz
RF_IN input power (Low Gainmode)	P_{RFINL_ABS}		-5	dBm	at 1575.42MHz & 1602MHz
			0	dBm	at 900MHz
			-1	dBm	at 1800MHz

6.2 Power Supply

Table 6.2 Power Supply Characteristics

T_A=25°C, unless otherwise stated

Items	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply voltage to VCC	V_{CC}	3	3.3	3.6	V	
Backup supply to VBK	V_{BK}	1.4	-	3.6	V	
Rising slew rate of VCC	V_{CC_SR}	-	-	$3.6x10^4$ 1)	V/s	See Figure 6.1
Rising slew rate of VBK	V_{BK_SR}	3.6	-	$3.6x10^4$ 1)	V/s	See Figure 6.1
Output voltage from VCC_RF	V_{CC_RF}	V_{CC}-0.2	-	V_{CC}	V	$I_{CC\ RF}$=100mA
VCC current consumption Low Gain mode (FLNA: High)	I_{CCAL}	-	60	108	mA	Full search @T_A=85°C
	I_{CCTL}	-	54.5	-	mA	Tracking satellite outdoor @-130dBm signal level
VCC current consumption High Gain mode (FLNA: Open)	I_{CCAH}	-	67.5	115.5	mA	Full search @T_A=85°C
	I_{CCTH}	-	62	-	mA	Tracking satellite outdoor @-130dBm signal level
VBK current consumption at back up	I_{BKN}	-	9	20	µA	V_{CC}=0V
VBK current consumption at normal operation)	I_{BKB}	-	0.4	2	µA	V_{CC}=3.3V

Notes:

1) When the rising slew rate of VCC and VBK is more than $3.6x10^4$ V/s, the internal ESD protection circuit turns on during the voltage rising and the inrush current of the power supply may be increased. However, it does not cause damage to the module.

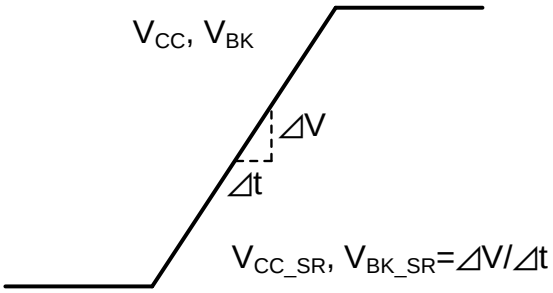


Figure 6.1 Rising Slew Rate

6.3 Interface

6.3.1 Interface Signal

Table 6.3 Interface Signal

Items	Symbol	Min.	Typ.	Max.	Unit	Notes
Logic L input voltage	V_{IL}	-	-	0.8	V	
Logic H input voltage	V_{IH}	2.0	-	-	V	
Hysteresis voltage	V_{hst}	0.31	-	-	V	
Logic L output voltage	V_{OL}	-	-	0.4	V	@$\|I_{OL}\|$ = 2mA
Logic H output voltage	V_{OH}	2.4	-	-	V	@$\|I_{OH}\|$ = 2mA
Equivalent pull-up resistor	R_{PU}	29	41	62	kΩ	@V_I = 3.3V △1
Equivalent pull-down resistor	R_{PD}	30	44	72	kΩ	@V_I = 0V △1

6.3.2 Precaution on Using the Input Pin with Pull-up Resistor △1

If the input pin with a pull-up resistor (5.ANT_DET1, 6.ANT_DET0, 8.RST_N, 18.RXD2, 21.RXD1) is connected to a signal source through an in-series resistor R_{in} (that includes the output impedance of the signal source), R_{in} must be less than or equal to 180Ω. △2

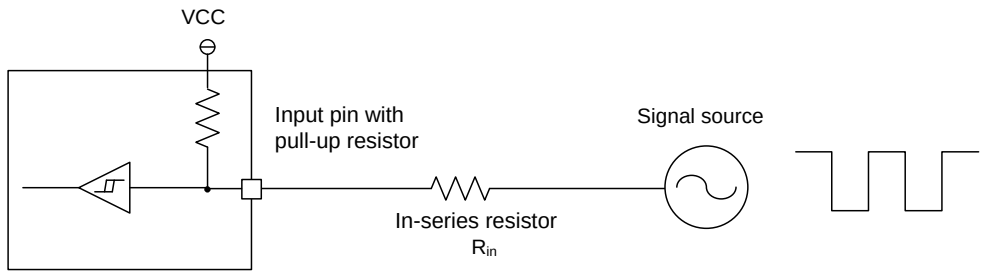


Figure 6.2 Precaution on Using the Input Pin with Pull-up Resistor

6.4 Reset

6.4.1 Internal Power-on Reset

GN-8720 contains internal power-on reset circuit which detects VCC voltage and creates POR_N (power-on reset) signal for initializing module. Table 6.4 shows the threshold voltages to detect and create POR_N signal.

Table 6.4 Power-on Reset Voltage

Items	Symbol	Min.	Typ.	Max.	Unit	Notes
Power On Reset threshold voltage (rising)	V_{RTH_POR}	-	-	3.0	V	
Power On Reset threshold voltage (falling)	V_{FTH_POR}	2.7	-	-	V	

6.4.2 External Reset

In most cases, it is not required to drive external reset input (RST_N) pin. However, if it is needed to force being in reset state externally for e.g. synchronizing reset state with application circuitry, RST_N can be used for this purpose. RST_N should be driven by open-drain or open-collector device for avoiding any collision with internal power-on reset driver.

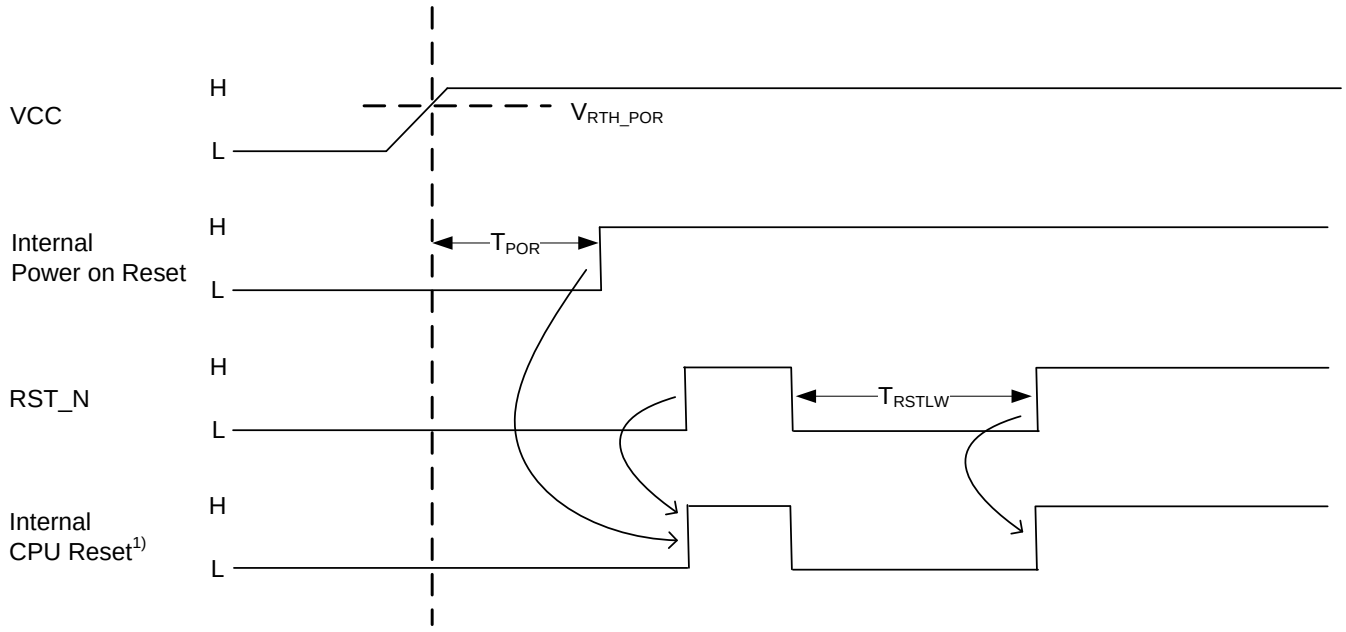


Figure 6.3 Reset Sequence

Table 6.5 Reset Sequence

Items	Symbol	Min.	Max.	Unit	Notes
Internal power on reset released time after VCC reaches V_{RTH_POR}	T_{POR}	150	250	ms	
Reset pulse width	T_{RSTLW}	300	-	ms	

Notes:
1) CPU reset is released when both the internal power on reset and the external reset (RST_N) are released.

6.5 UART Wake-up Timing after Reset

6.5.1 Without External Reset

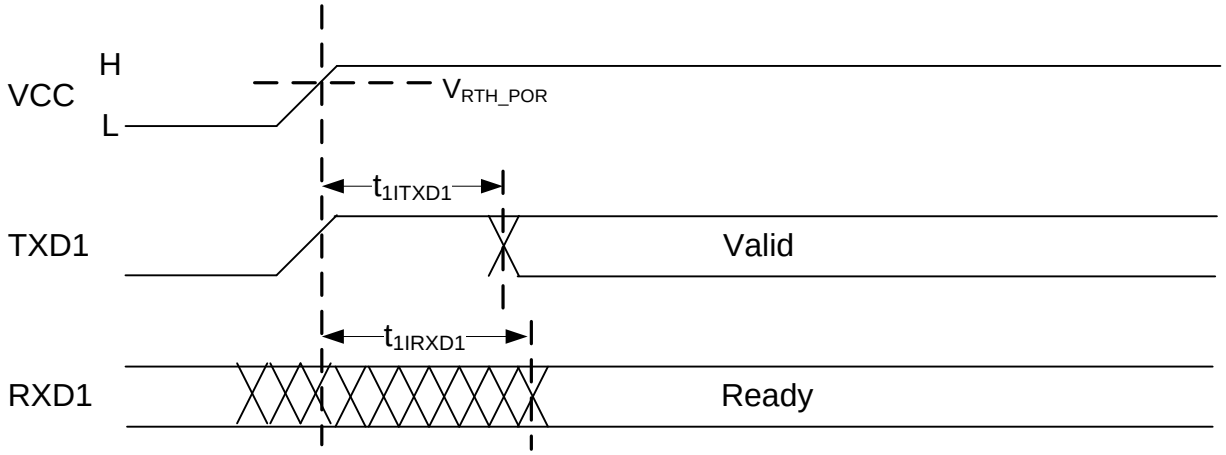


Figure 6.4 UART Wake-up Timing after V_{RTH_POR}

Table 6.6 UART Wake-up Timing after V_{RTH_POR}

Items	Symbol	Min.	Max.	Unit	Notes
Time delay from VCC reaches V_{RTH_POR} to TXD1 valid	t_{1ITXD1}	-	400	ms	
Time delay from VCC reaches V_{RTH_POR} to RXD1 ready	t_{1IRXD1}	-	600	ms	

6.5.2 With External Reset

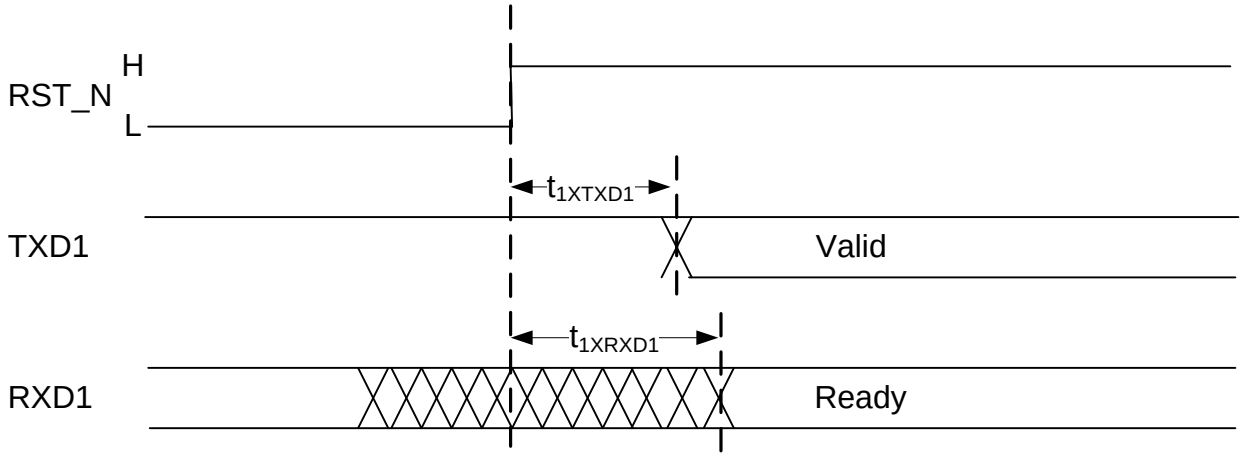


Figure 6.5 UART Wake-up Timing after RST_N

Table 6.7 UART Wake-up Timing after RST_N

Items	Symbol	Min.	Max.	Unit	Notes
Time delay from RST_N set to H to TXD1 valid	t_{1XTXD1}	-	200	ms	
Time delay from RST_N set to H to RXD1 ready	t_{1XRXD1}	-	400	ms	

6.5.3 Baud Rate Setting

The UART inside GN-8720 can handle various baud rate serial data shown in Table 6.8. The baud rate clock is created from 71.5 MHz system clock, hence it has some deviation errors against ideal baud rate clock as shown in Table 6.8.

Table 6.8 Baud Rate vs. Deviation Error

Baud rate [bps]	Deviation error [%]
4800	+0.00
9600	+0.11
19200	-0.11
38400	+0.32
57600	-0.54
115200	-0.54
230400	+2.08
460800	-3.02

6.6 Recommended GNSS Antenna

6.6.1 Active Antenna

Table 6.9 Recommended Active Antenna

Items	Min.	Typ.	Max.	Unit	Notes
GPS center frequency	-	1575.42	-	MHz	2.046 MHz bandwidth
GLONASS center frequency	-	1602	-	MHz	9 MHz bandwidth
Antenna element gain	0	-	-	dBi	
Amplifier gain1	10	-	35[1)]	dB	Including cable loss High Gain mode (FLNA: Open)
Amplifier gain2	15	-	50[1)]	dB	Including cable loss Low Gain mode (FLNA: High)
Amplifier NF	-	1.5	3	dB	Including cable loss
Impedance	-	50	-	Ω	
VSWR	-	-	2	-	

Notes:
1) For best jammer resistance (and lower power consumption) use 10 dB lower gain than the max gain.

6.6.2 Passive Antenna

Table 6.10 Recommended Passive Antenna

Items	Min.	Typ.	Max.	Unit	Notes
GPS center frequency	-	1575.42	-	MHz	2.046 MHz bandwidth
GLONASS center frequency	-	1602	-	MHz	9 MHz bandwidth
Antenna element gain	0	-	-	dBi	FLNA: Open
Impedance	-	50	-	Ω	
VSWR	-	-	2	-	

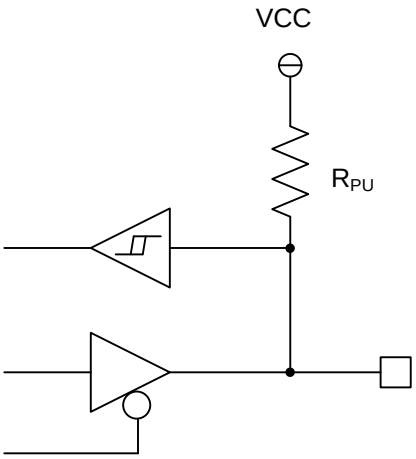
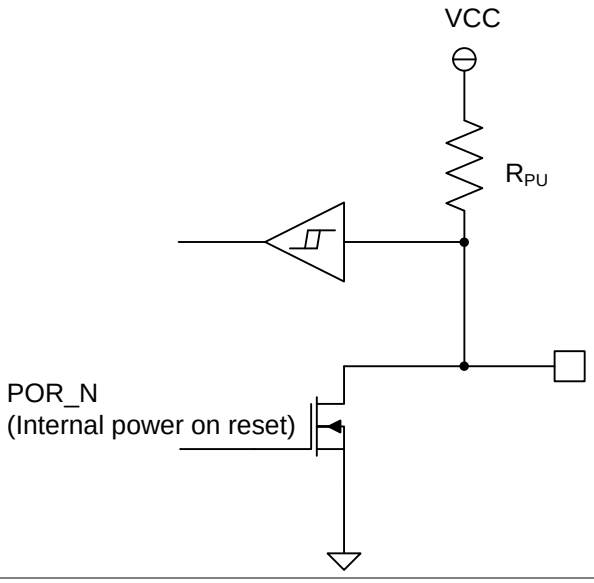
7 Environmental Specifications

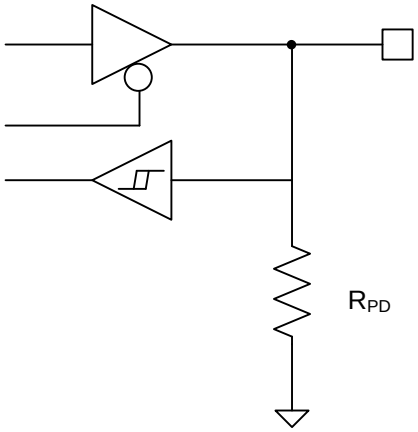
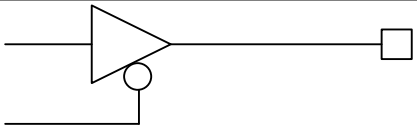
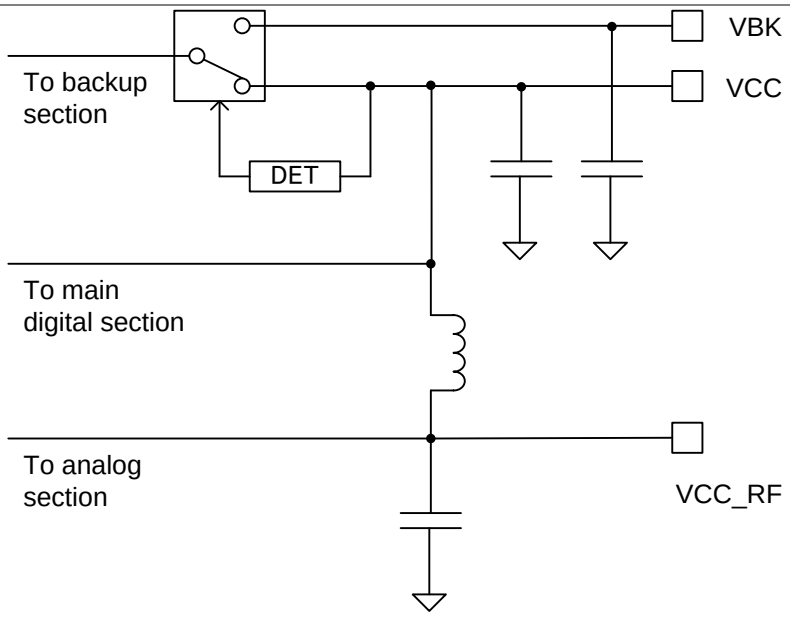
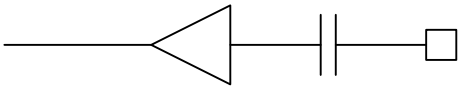
Table 7.1 Environmental Specifications

Items	Specification	Unit	Notes
Operating temperature	-40 to +85	°C	
Storage temperature	-40 to +85	°C	
Operation humidity	85（MAX）	%R.H	T_A= 60°C, No condensation

8 Equivalent Circuit

Table 8.1 Equivalent Circuit

Pin Name	Equivalent Circuit
1. RESERVED, 5.ANT_DET1, 6.ANT_DET0, 17. RESERVED, 18. RXD2, 19. TXD2, △1 21.RXD1	
8.RST_N	

Pin Name	Equivalent Circuit
2.FLNA, 3.PPS, 4. RESERVED, 7. RESERVED, 14. RESERVED, 15. RESERVED, 16. RESERVED	
20.TXD1	
9.VCC_RF, 22.VBK, 23.VCC	 AC coupling capacitor Rated voltage: 50V
11.RF_IN	 Integrated LNA

9 Mechanical Specifications

9.1 Package Dimension

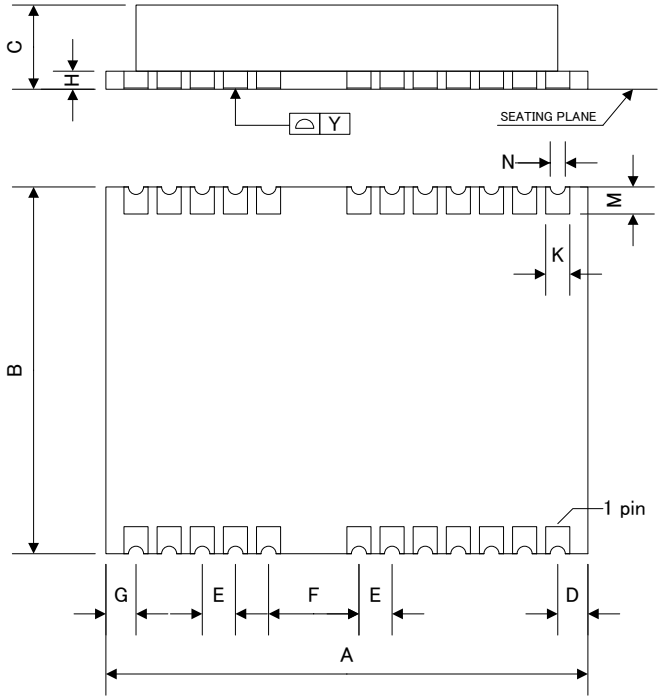


Figure 9.1 Package Dimension

Table 9.1 Package Dimension

	Min. [mm]	Typ. [mm]	Max. [mm]
A	15.8	16.0	16.2
B	12.0	12.2	12.4
C	2.6	2.8	3.0
D	0.9	1.0	1.1
E	1.0	1.1	1.2
F	2.9	3.0	3.1
G	0.9	1.0	1.1
H	-	0.6	-
K	0.7	0.8	0.9
M	0.8	0.9	1.0
N	0.4	0.5	0.6
Y[1)]	-	-	0.1

Notes:
1) The height of the terminals to the mounting surface

9.2 Electrode

Electrode Material: Cu
Metallic Finishing: Electroless gold flashing (Au: 0.03 μ and over Ni: 3 μ and over)

9.3 Weight

1.01g (TYP)

9.4 Pin Position List

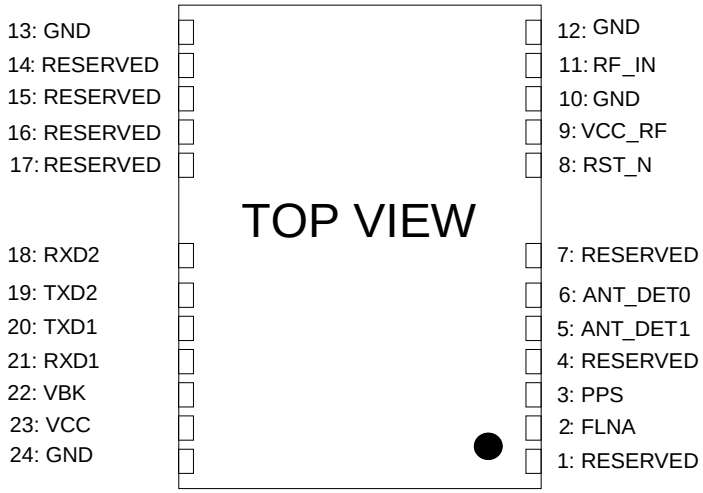
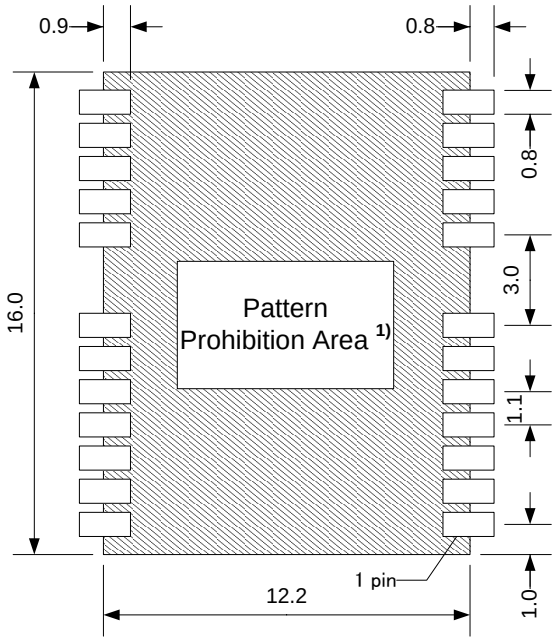


Figure 9.2 Pin Position List

10 Reference Design

10.1 Recommended Land Pattern



Unit: [mm]

Figure 10.1 Recommended Land Pattern

Notes:
1) At the bottom of the module, there are some signal lines and via holes. For avoiding any signal shortage, please do not put any signal line nor via hole at the part of the user's board where is facing to the bottom of the module.

10.2 Example of Connection

10.2.1 With Active Antenna

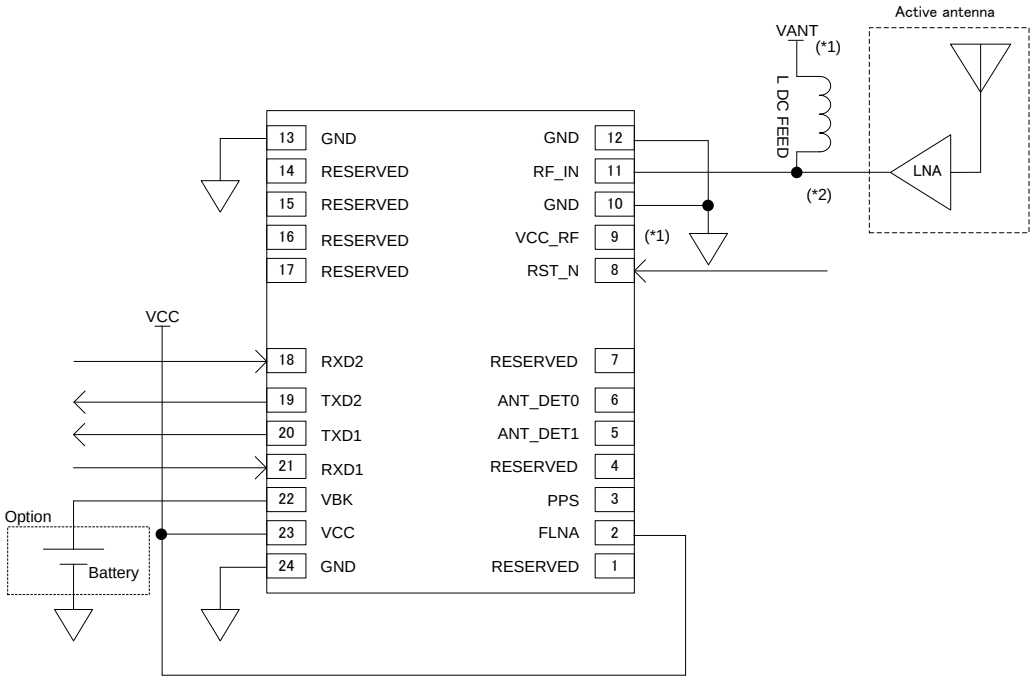


Figure 10.2 Example of Connection (with Active Antenna)

Notes:

1) VCC_RF, power supply output pin, can be used for VANT. However, when the signal line which the VANT voltage is superposed is short-circuited, the VCC_RF output current may exceed the absolute maximum rating $I_{CC\_RF\_ABS}$. Therefore, it is recommended to implement an over current protection circuit for preventing an over current.
2) In case of using an external antenna, it is recommended to implement the ESD protection with an ESD protection diode or a λ/4 short stub for preventing excessive stress to the RF_IN pin. Please refer “FURUNO GPS/GNSS Receiver 86/87 series User's Design Guide (SE13-900-001)” about the λ/4 short stub.

10.2.2 With Passive Antenna

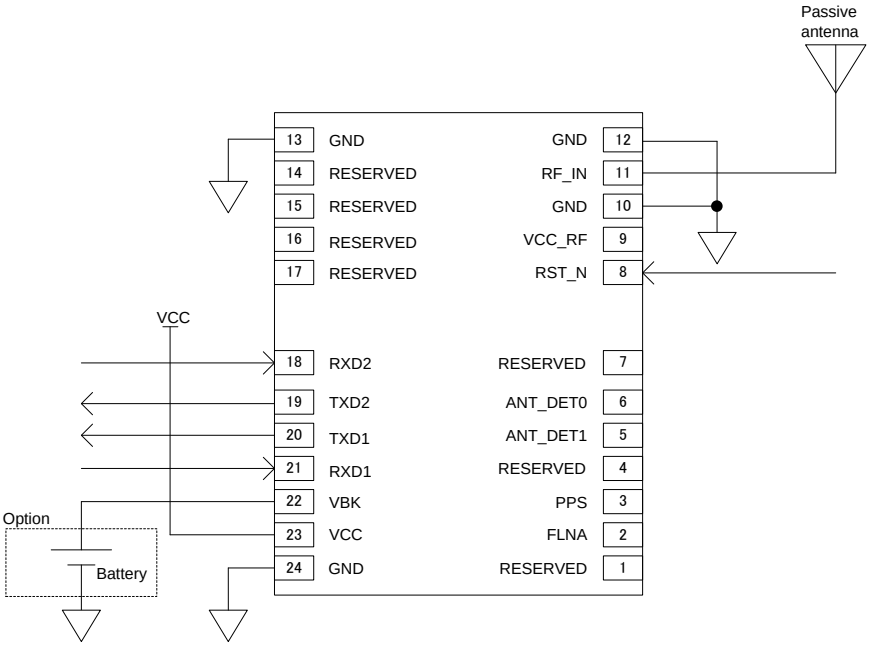
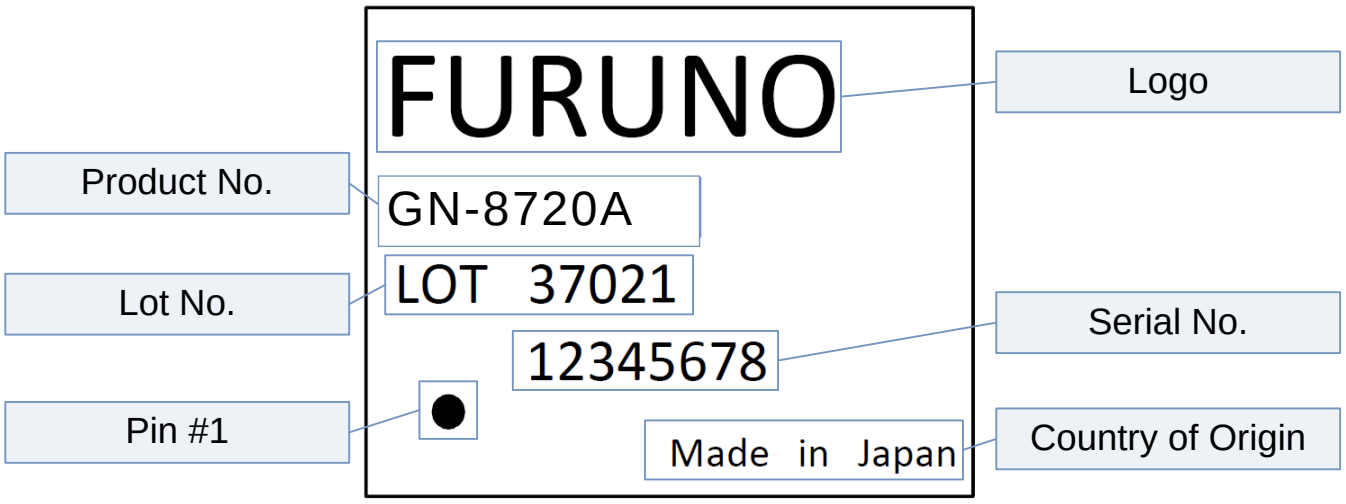
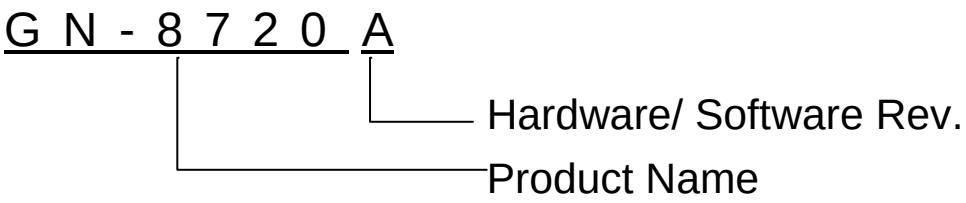


Figure 10.3 Example of Connection (with Passive Antenna)

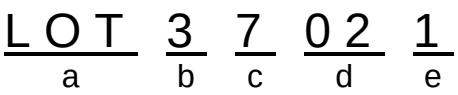
11 Marking



(1) Logo FURUNO
(2) Product No. GN-8720A



(3) Lot No. LOT 37021



#	Code	Description
a	LOT	"LOT"
b	3	Year (last digit of the year number: 2015=5)
c	7	Month (1 to 9, X, Y, Z)
d	02	Date (01 to 31)
e	1	Internal control number

(4) Serial No. 12345678
Individual unique number
(5) Country of origin Japan
(6) Pin 1 symbol

12 Handling Precaution

The section especially describes the conditions and the requests when mounting the product.

Surface mount products like this may have a crack when thermal stress is applied during surface mount assembly after they absorb atmospheric moisture. Therefore, please observe the following precautions:

(1) This product contains semi-conductor inside. While handling this, be careful about the static electrical charge. To avoid it, use conductive mat, ground wristband, anti-static shoes, ionizer, etc. as may be necessary.
(2) Try to avoid mechanical shock and vibration. Try not to drop this product.
(3) When mounting this product, be aware of the location of the electrode.
(4) This product should not be washed.
(5) The reflow conditions are as shown in chapter 14. The reflow can be done twice at most.
(6) Surface mount products like this may have a crack when thermal stress is applied during surface mount assembly after they absorb atmospheric moisture. Therefore, please observe the following precautions:
    ① This moisture barrier bag may be stored unopened 12 months at or below 30°C/90%RH.
    ② After opening the moisture bag, the packages should be assembled within 1 week in the environment less than 30°C/60%RH.
    ③ If, upon opening, the moisture indicator card in the bag shows humidity above 30% or the expiration date has passed, they may still be used with the addition of a bake of 24 hours at 125°C.
    Caution: If the packing material is likely to melt at 125°C, heat-proof tray or aluminum magazine etc. must be used for high temperature.
    ④ Expiration date: 12 months from the sealing date.
(7) This module includes a crystal oscillator. It may not be able to maintain the characteristic under the vibrating condition, windy and cold conditions and noisy conditions. Please evaluate the module on ahead, if it may be used under these conditions.

13 Solder Profile

13.1 Reflow Profile

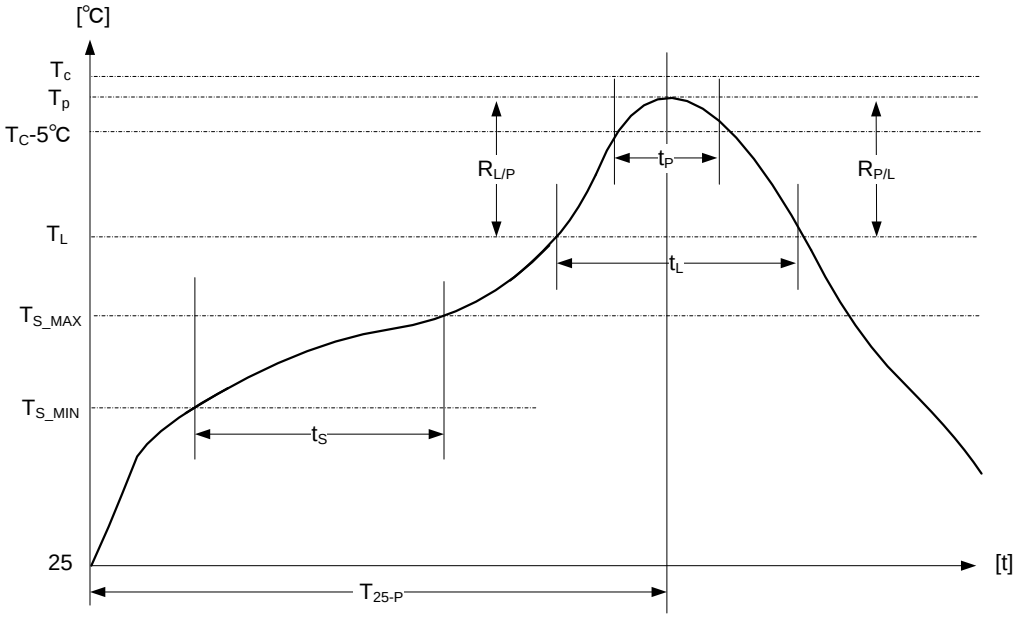


Figure 13.1 Condition of Reflow (Based on IPC/JEDEC J-SED-020D)

Table 13.1 Condition of Reflow (Pb-free)

Item	Symbol	Condition	Notes
Preheat/Soak Minimum Temperature	$T_{S\text{-}MIN}$	150°C	
Preheat/Soak Maximum Temperature	$T_{S\text{-}MAX}$	200°C	
Preheat/Soak Time from $T_{S\text{-}MIN}$ to $T_{S\text{-}MAX}$	t_S	60 to 120 s	
Ramp-up rate T_L to T_P	$R_{L/P}$	3°C/s (Max)	
Liquidus Temperature	T_L	217 to 220°C	
Time maintained above T_L	t_L	60 to150 s	
Specified classification temperature	T_C	260°C	
Time within 5°C of T_C	t_P	30 s	Tolerance for t_p is defined as a user maximum
Ramp-down rate T_L to T_P	$R_{P/L}$	6°C/s (Max)	
Time from 25°C to peak temperature	$T_{25\text{-}P}$	8 min. (Max)	

Notes:
- Please reflow according to Figure 13.1 and Table 13.1.
- Recommended temperature reflow profile pattern is lead free.
- Recommended atmosphere in chamber is Nitrogen.
- Oxygen density level is less than 1500 ppm.
- Profile temperature should be measured on top of the shielding case.
- Package condition except IPC/JEDEC J-STD-020D needs pre-baking.
- If customer should change to reflow profile from what we recommend due to temperature condition inside of reflow chamber. Please inquire us for impact on the following items.
  - Soldering of module pad on customer's board and our module
  - Solder re-melting of components mounted on our module

Table 13.2 shows the moisture sensitivity level and number of reflow for assembly at user side.

Table 13.2 Moisture Sensitivity Level, Number of Reflow for Assembly at User Side

Item	Condition
Moisture Sensitivity Level	3
Number of reflow for assembly at user side	2

13.2 Precaution about Partial Heating with the Way except Reflow

If the internal temperature when the product is heated partially with, for example, like a soldering iron, hot air and light beam welder exceeds 215 degree, the internal wiring may be disconnected by thermal stress.

14 Special Instruction

14.1 Electronic Component

Components in GN-8720 module such as chip resistors, capacitors, memories and TCXO are planned to be purchased from multiple manufacturers/vendors according to FURUNO's procurement policy. So it is possible that multiple components from multiple manufacturers/vendors could be used even in the same production lot.

14.2 RoHS

GN-8720 complies with RoHS directives.

15 Reference Documents

- FURUNO 86&87Module Package Specifications (SE13-600-024)
- FURUNO 86/87 Module Reliability Test (SE16-600-012) △1
- FURUNO GPS/GNSS Receiver 86/87 series User's Design Guide. (Document No. SE13-900-001)