Features

- **Vcc = 5V ± 5%**
- **Military Temperature Range**
- **Fully Compatible with the TS68040**
- **Five Low Skew Outputs**
  - **Five Outputs (Q0-Q4) with Output-to-Output Skew < 500 ps Each Being Phase End Frequency Locked to the SYNC Input**
- **Three Additional Outputs are Available:**
  - **The 2X_Q Output Runs Twice the System "Q" Frequency**
  - **The Q/2 Output Runs At 1/2 the System "Q" Frequency**
  - **The $\overline{Q5}$ Output is Inverted (180° Phase Shift)**
- **Two Selectable Clock Inputs**
  - **Two Selectable CLOCK Inputs are Available for Test or Redundancy Purposes**
  - **Test Mode Pin (PLL_EN) Provided for Low Frequency Testing**
  - **All Outputs Can Go Into High Impedance (3-state) for Board Test Purposes**
- **Input Frequency Range From 5 MHz to 2X_Q FMAX**
- **Three Input/Output Ratios**
  - **Input/Output Phase-locked Frequency Ratios of 1:2, 1:1 and 2:1 are Available**
- **Low Part-to-part Skew**
  - **The Phase Variation from Part-to-part Between the SYNC and FEEDBACK Inputs is Less than 550 ps (Derived From the tPD Specification, which Defines the Part-to-part Skew)**
- **CMOS and TTL Compatible**
  - **All Outputs Can Drive Either CMOS or TTL Inputs**
  - **All Inputs are TTL-level Compatible**
- **LOCK Indicator (LOCK) Indicates a Phase-locked State**

Low Skew CMOS PLL Clock Driver Tri-State 70 and 100 MHz Versions

TS88915T

Description

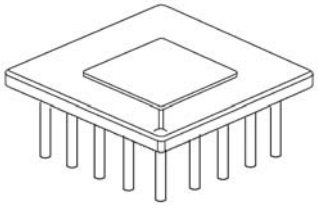
The TS88915T Clock Driver utilizes a phazed-locked loop (PLL) technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for high performance microprocessors such as TS68040, TSPC603E,TSPC603P,TSPC603R, PCI bridge, RAM's, MMU's.

Screening/Quality

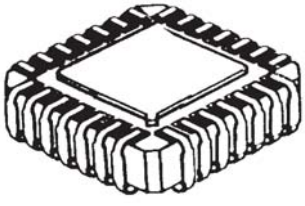
This Product is Manufactured:

- Based Upon the Generic Flow of MIL-STD-883
- or According to Atmel-Grenoble Standard

R suffix
PGA 29
Ceramic Pin Grid Array



W suffix
LDCC 28
Leaded Ceramic Chip Carrier

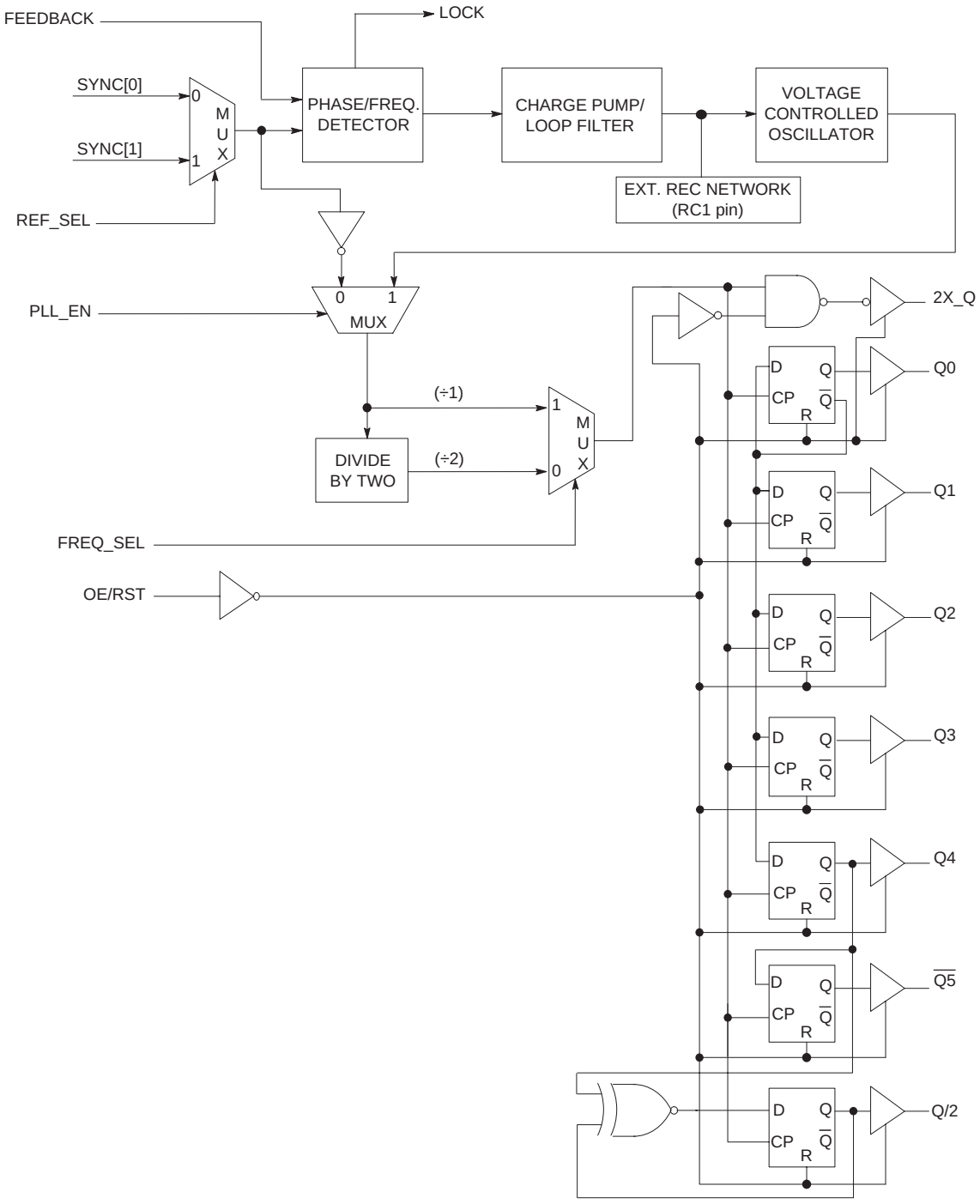


Rev. 2122A–HIREL–06/02

Introduction

The TS88915T is a CMOS PLL Clock Driver using phase-locked loop (PLL) technology. The PLL allows the high current and low skew outputs to lock onto a single input and distribute it with essentially zero delay to multiple components on a board. The PLL also allows the TS88915T to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency. Multiple 88915's can lock onto a single reference clock, which is ideal for applications when a central system clock must be distributed synchronously to multiple boards (see Figure 12).

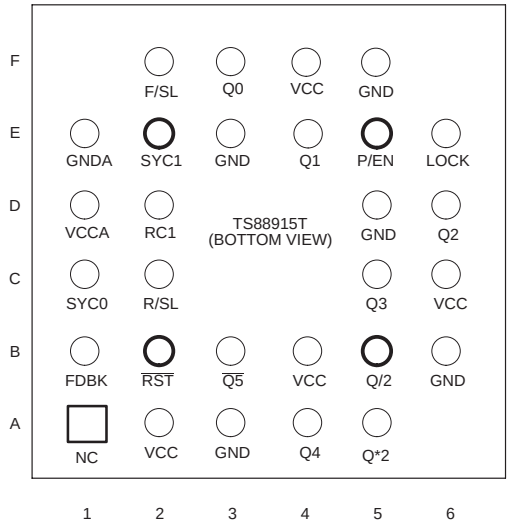
Figure 1. TS88915T Block Diagram (All Versions)



Pin Assignments

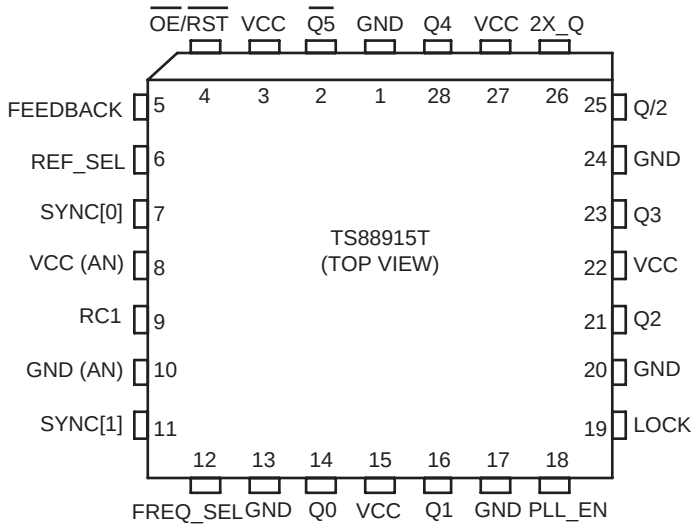
29-lead Pin Grid Array (PGA)

Figure 2. 29-lead PGA (Bottom View)



28-lead Ceramic Leaded Chip Carrier (LDCC)

Figure 3. 28-lead LDCC (Top View)



Signal Description

Table 1. Signal Index

Pin Name	Num	I/O	Signal Function
SYNC[0]	1	Input	Reference Clock Input
SYNC[1]	1	Input	Reference Clock Input
REF_SEL	1	Input	Chooses Reference Between SYNC[0] and SYNC[1]
FREQ_SEL	1	Input	Doubles VCO Internal Frequency
FEEDBACK	1	Input	Feedback Input to Phase Detector
RC1	1	Input	Input for External RC Network
Q(0-4)	5	Output	Clock Output (Locked to SYNC)
$\overline{Q5}$	1	Output	Inverse of Clock Output
2x_Q	1	Output	2 x Clock Output (Q) Frequency (Synchronous)
Q/2	1	Output	Clock Output (Q) Frequency ÷ 2 (Synchronous)
LOCK	1	Output	Indicates Phase Lock has been Achieved (High when Locked)
$\overline{OE}/\overline{RST}$	1	Input	Output Enable/Asynchronous Reset (Active Low)
PLL_EN	1	Input	Disables Phase-lock for Low Frequency Testing
VCC, GND	11	Power	Power and Ground pins Pins 8 and 10 are “analog” supply pins for internal PLL only

Scope

This drawing describes the specific requirements for the clock driver TS88915T, in compliance with MIL-STD-883 class B or Atmel standard screening.

Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics.
2. MIL-PRF-38535 appendix A: General specifications for microcircuits.

Requirements

General

The microcircuits are in accordance with the applicable documents and as specified herein.

Design and Construction

Terminal Connections

Depending on the package, the terminal connections shall be as shown in Figure 2 and Figure 3.

Lead Material and Finish

Lead material and finish shall be as specified in MIL-STD-1835 (see “Package Mechanical Data” on page 17).

Package

The macrocircuits are packaged in hermetically sealed ceramic packages, which conform to case outlines of MIL-STD-1835, but “Package Mechanical Data” on page 17.

The precise case outlines are described at the end of the specification (see “Package Mechanical Data” on page 178) and into MIL-STD-1835.

Absolute Maximum Ratings

Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

Table 2. Absolute Maximum Rating for the TS88915T

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	-0.5	6.0	V
Input Voltage	V_{in}	-0.5	V_{CC} + 0.5	V
Storage Temperature Range	T_{stg}	-65	+150	°C
Power Dissipation PGA Package LDCC Package	P_D		500	mW
Thermal Resistance Junction-Case PGA29 LDCC28	Θ_{JC}	 - -	 7 7	°C/W

Note: Functional operating conditions are given in AC and DC electrical specifications. Stresses beyond the absolute maximums listed may affect device reliability or cause permanent damage to the device.
Caution: Input voltage must not be greater than the supply voltage by more than 2.5V at all times including during power-on reset.

Mechanical and Environment

The microcircuits shall meet all environmental requirements of either MIL-STD-883 for class B devices or for Atmel standard screening.

Marking

The document that defines the markings is identified in the related reference documents. Each microcircuit is legible and permanently marked with the following information as minimum:

- Atmel Logo
- Manufacturer's Part Number
- Class B Identification
- Date-code of Inspection Lot
- ESD Identifier If Available
- Country of Manufacturing

Electrical Characteristics

General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below:

- Table Static Electrical Characteristics for the Electrical Variants
- Table Dynamic Electrical Characteristics for TS88915T (70 MHz and 100 MHz Versions)

Static Characteristics

DC Electrical Characteristics

(Voltages Referenced to GND) T_c = -55°C to +125°C for 70 MHz and 100 MHz version; VCC = 5.0V ± 5%

Symbol	Parameter	Test Conditions		Limits	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1V or V_{CC} - 0.1V		2.0	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1V or V_{CC} - 0.1V		0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL}, I_{OH} = -36 mA(1)	V_{CCmin} V_{CCmax}	4.01 4.51	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL}, I_{OL} = 36 mA(1) V_{in} = V_{IH} or V_{IL}, I_{OL} = 15 mA(6)		0.44(4) 0.50(5) 0.20	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND, V_{CCmax}		±1.0	µA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} - 2.1V, V_{CCmax}		2.0(2)	mA
I_{CC}	Maximum Quiescent Supply Current (per package)	V_I = V_{CC} or GND, V_{CCmax}		1.0	mA
I_{OZ}	Maximum Tri-State Leakage Current	V_I = V_{IH} or V_{IL},V_O = V_{CC} or GND, V_{CCmax}		$50	µA

Notes: 1. I_{OL} and I_{OH} are 12 mA and -12 mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0 ms, one output loaded at a time.
4. Specification value for static tests at 25°C and at minimum rated operating temperature.
5. Specification value for static tests at maximum rated operating temperature.
6. Specifications values which can be used for compability with the Power PC.

Capacitance and Power Specifications

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	10	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0V
PD_1	Power Dissipation at 50 MHz with 50Ω Thevenin Termination	23 mW/Output 184 mW/Device	mW	V_{CC} = 5.0V T = 25°C
PD_2	Power Dissipation at 50 MHz with 50Ω Parallel Termination to GND	57 mW/Output 456 mW/Device	mW	V_{CC} = 5.0V T = 25°C

Note: 1. PD_1 and PD_2 mW/Output are for a 'Q' output.

Dynamic Characteristics (Tc = -55°C to +125°C, VCC = 5.0V ± 5%)

Frequency Specifications

Symbol	Parameter	Guaranteed Minimum		Unit
		88915T-70	88915T-100	
f_{max}(1)	Maximum Operating Frequency (2X_Q Output)	70	100	MHz
	Maximum Operating Frequency (Q0-Q4, $\overline{Q5}$ Outputs)	35	50	MHz

Note: 1. Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50Ω terminated to V_{CC}/2.

SYNC Input Timing Requirements

Symbol	Parameter	Minimum		Maximum	Unit
		88915T-70	88915T-100		
$t_{RISE/FALL}$, SYNC Inputs	Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V	–	–	3.0	ns
t_{CYCLE}, SYNC Inputs	Input Clock Period, SYNC Inputs	28.5(1)	20.0(1)	200(2)	ns
Duty Cycle SYNC Inputs	Input Duty Cycle, SYNC Inputs	50% ± 25%			

Notes: 1. These t_{CYCLE} minimum values are valid when 'Q' output is feed back and connected to the FEEDBACK pin.
2. Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is feed back, and if FREQ_SEL is high or low.

AC Characteristics (T_c = -55°C to +125°C, V_{CC} = 5.0V ± 5%, Load = 50Ω terminated to V_{CC}/2)

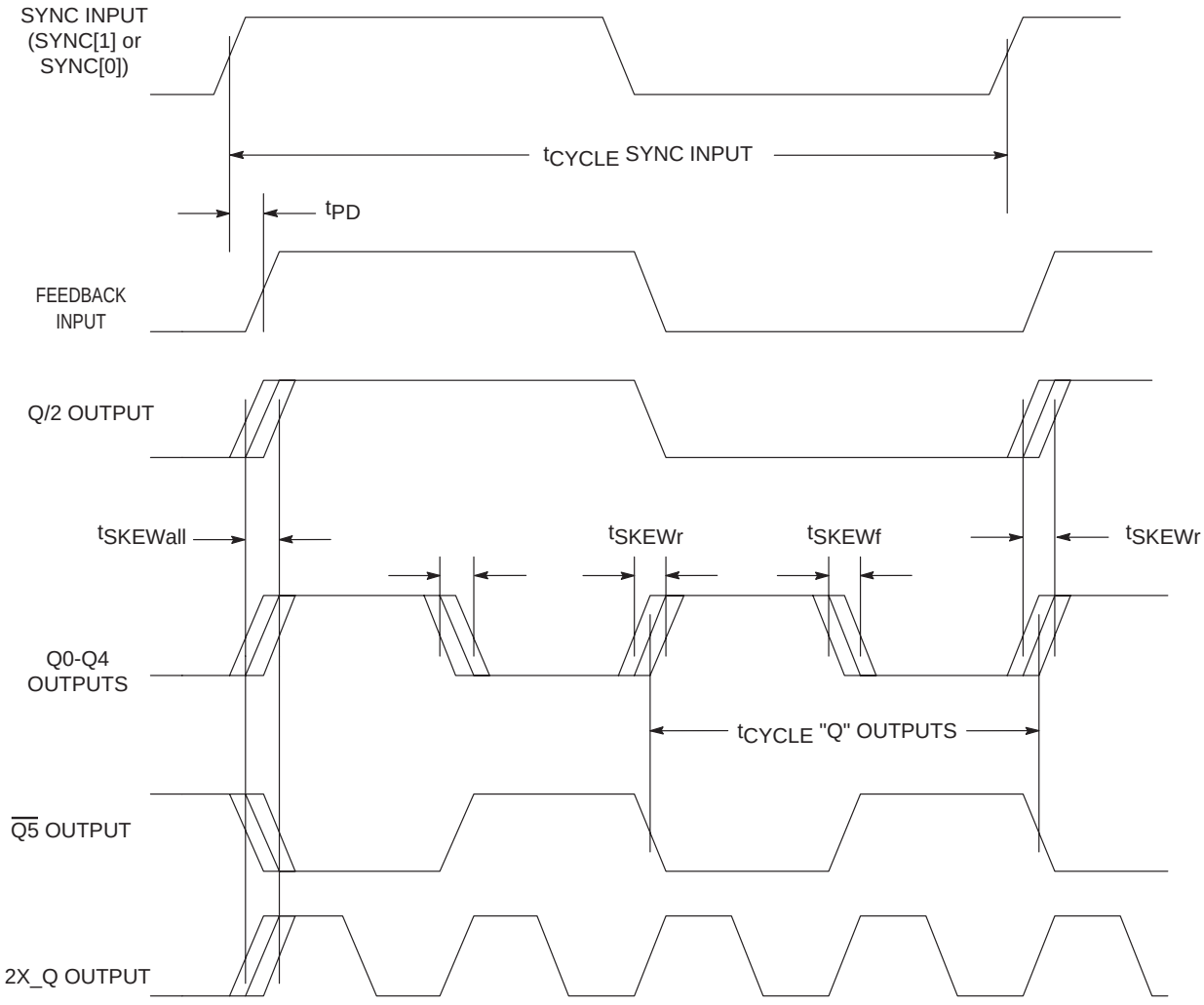
Symbol	Parameter		Min	Max	Unit	Conditions
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.2 V_{CC} and 0.8 V_{CC})		1.0	2.5	ns	Into a 50Ω Load Terminated to V_{CC}/2
$t_{RISE/FALL}$(1) 2X_Q Output	Rise/Fall Time into a 20 pF Load, with Termination(2)		0.5	1.6	ns	t_{RISE}: 0.8V - 2.0V t_{FALL}: 2.0V - 0.8V
$t_{PULSE\ WIDTH}$(1) (Q0-Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, Q5, Q/2 at V_{CC}/2		$0.5t_{CYCLE}$ - 0.5(2)	$0.5t_{CYCLE}$ + 0.5(2)	ns	Into a 50Ω Load Terminated to V_{CC}/2
$t_{PULSE\ WIDTH}$(1) (2X_Q Output)	Output Pulse Width: 2X_Q at 1.5V	40 MHz 50 MHz 66 MHz 100 MHz	$0.5t_{CYCLE}$ - 1.5(2) $0.5t_{CYCLE}$ - 1.0 $0.5t_{CYCLE}$ - 0.5 $0.5t_{CYCLE}$ - 0.5	$0.5t_{CYCLE}$ + 1.5(2) $0.5t_{CYCLE}$ + 1.0 $0.5t_{CYCLE}$ + 0.5 $0.5t_{CYCLE}$ + 0.5	ns	Must use termination(2)
$t_{PULSE\ WIDTH}$(1) (2X_Q Output)	Output Pulse Width: 2X_Q at V_{CC}/2	40-49 MHz 50-65 MHz 66-100 MHz	$0.5t_{CYCLE}$ - 1.5(2) $0.5t_{CYCLE}$ - 1.0 $0.5t_{CYCLE}$ - 0.5	$0.5t_{CYCLE}$ + 1.5(2) $0.5t_{CYCLE}$ + 1.0 $0.5t_{CYCLE}$ + 0.5	ns	Into a 50Ω Load Terminated to V_{CC}/2
t_{PD}(1)(3) SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK input pins)	70 MHz 100 MHz	(With 1 MΩ from RC1 to An V_{CC})		ns	See Note 4 and Figure 6 for detailed explanation
			-1.05	-0.40		
			-1.05	-0.30		
			(With 1 MΩ from RC1 to An GND)			
			+1.25	+3.25		
t_{SKEWr}(1)(4) (Rising)(5)	Output-to-Output Skew between Outputs Q0-Q4, Q/2 (Rising edges only)		–	500	ps	All Outputs into a matched 50Ω load Terminated to V_{CC}/2
t_{SKEWf}(1)(4) (Falling)	Output-to-Output Skew between Outputs Q0-Q4 (Falling edges only)		–	750	ps	All Outputs into a matched 50Ω load Terminated to V_{CC}/2
$t_{SKEWall}$(1)(4) (Falling)	Output-to-Output Skew 2X_Q, Q/2, Q0-Q4 Rising, $\overline{Q5}$ Falling		–	750	ps	All Outputs into a matched 50Ω load Terminated to V_{CC}/2

AC Characteristics (T_c = -55°C to +125°C, V_{CC} = 5.0V ± 5%, Load = 50Ω terminated to V_{CC}/2) **(Continued)**

Symbol	Parameter	Min	Max	Unit	Conditions
t_{LOCK} (5)	Time required to acquire Phase-Lock from time SYNC inputs signal is received	1.0	10	ms	Also time to lock indicator High
t_{PZL}	Output Enable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0-Q4, $\overline{Q5}$ and Q/2	3.0	14	ns	Measured with the PLL_EN pin Low
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0-Q4, $\overline{Q5}$ and Q/2	3.0	14	ns	Measured with the PLL_EN pin Low

Notes:
1. These specifications are not tested, they are guaranteed by statistical characterization. See General AC specification Note 1.
2. t_{CYCLE} in this specification is 1/Frequency at which the particular output is running.
3. The T_{PD} specification's min/max values may shift closer to zero of a larger pull up resistor is used.
4. Under equally loaded conditions and at a fixed temperature and voltage.
5. With V_{CC} fully powered-on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1 µF, t_{LOCK} minimum is with C1 = 0.01 µF.

Figure 4. Output/Input Switching Waveforms and Timing Diagrams
(These waveforms represent the hook-up configuration of Figure 8)

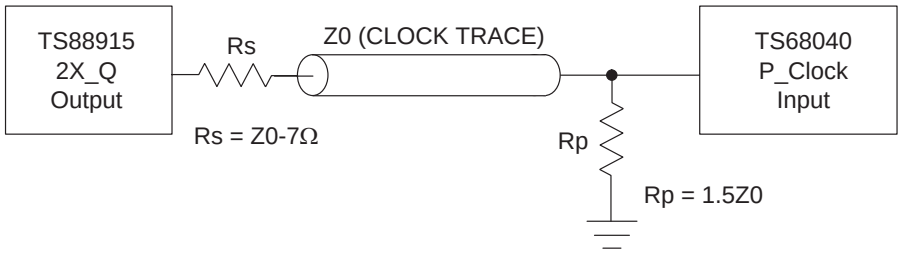


Application Information

General AC Specification Notes

1. Several specifications can only be measured when the TS88915T is in phase-locked operation. TS88915T units are fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix.
2. These two specs ($t_{RISE/FALL}$ and $t_{PULSE\ WIDTH}$ 2X_Q output) guarantee that the TS88915T meets the 33 MHz TS68040 P-Clock input specification (at 66 MHz). For these two specs to be guaranteed by Atmel, the termination scheme shown below in Figure 5 must be used.

Figure 5. TS68040 P-Clock Input Termination Scheme



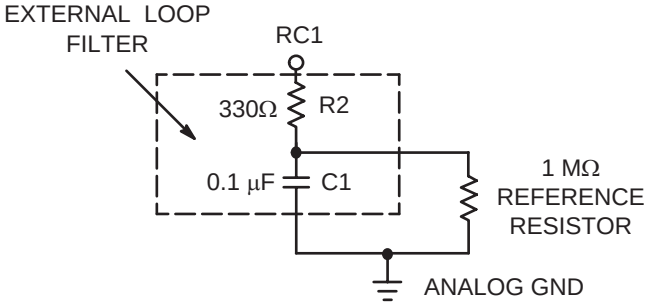
3. To meet the 25 MHz TS68040 P-clock input specification (2 x Q tpulse width at 50 MHz) FREQ-SEL must be low. This configuration improve the accuracy of the 88915T duty cycle.
4. The wiring diagrams and explanations in Figure 8, Figure 9 and Figure 10 demonstrate the input and output frequency relationships for three possible feedback configurations. The allowable SYNC input range for each case is also indicated. There are two allowable SYNC frequency ranges, depending whether FREQ_SEL is high or low. Although not shown, it is possible to feed back the $\overline{Q5}$ output, thus creating a 180° phase shift between the SYNC input and the "Q" outputs. Table 3 below summarizes the allowable SYNC frequency range for each possible configuration.

Table 3. Allowable SYNC Input Frequency Range for Different Feedback Configurations

FREQ_SEL Level	FEEDBACK Output	Allowable SYNC Input Frequency Range (MHz)	Corresponding VCO Frequency Range	Phase Relationships of the "Q" Outputs to Rising SYNC Edge
HIGH	Q/2	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	0°
HIGH	any "Q" (Q0-Q4)	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	0°
HIGH	Q5	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	180°
HIGH	2X_Q	20 to (2X_Q FMAX Spec)	20 to (2X_Q FMAX Spec)	0°
LOW	Q/2	2.5 to (2X_Q FMAX Spec)/8	20 to (2X_Q FMAX Spec)	0°
LOW	any "Q" (Q0-Q4)	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	0°
LOW	Q5	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	180°
LOW	2X_Q	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	0°

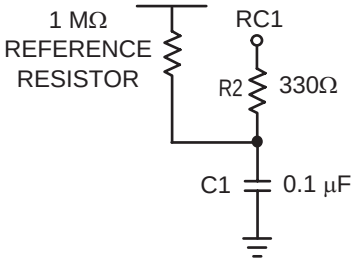
5. A 1 MΩ resistor tied to either Analog V_{CC} or Analog GND as shown in Figure 5 is required to ensure no jitter is present on the TS88915T outputs. This technique causes a phase offset between the SYNC input and the output connected to the FEEDBACK input, measured at the input pins. The T_{PD} spec describes how this offset varies with process, temperature and voltage. The specs are arrived at by measuring the phase relationship for the 14 lots described in Note 1 while the part was in phase-locked operation. The actual measurements are made with 10 MHz SYNC input (1.0 ns edge rate from 0.8V - 2.0V) with the Q/2 output feed back. The phase measurements are made at 1.5V. The Q/2 output is terminated at the FEEDBACK input with 100Ω to V_{CC} and 100Ω to GND.

Figure 6. Depiction of the Fixed SYNC to Feedback Offset (t_{PD}) Which is Present When a 1 MΩ Resistor is Tied to V_{CC} or GND



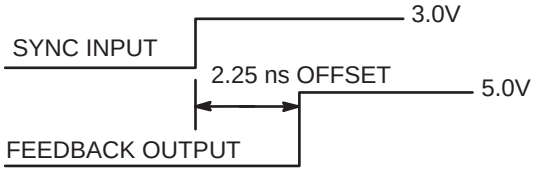
With the 1 MΩ resistor tied in this fashion, the t_{PD} specification measured at the input pins is:

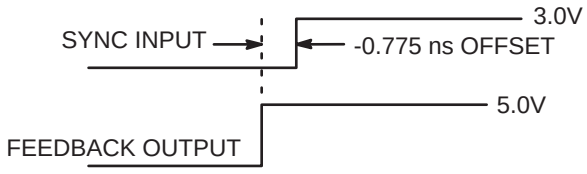
t_{PD} = 2.25 ns ± 1.0 ns



With the 1 MΩ resistor tied in this fashion, the t_{PD} specification measured at the input pins is:

t_{PD} = -0.775 ns ± 0.275 ns





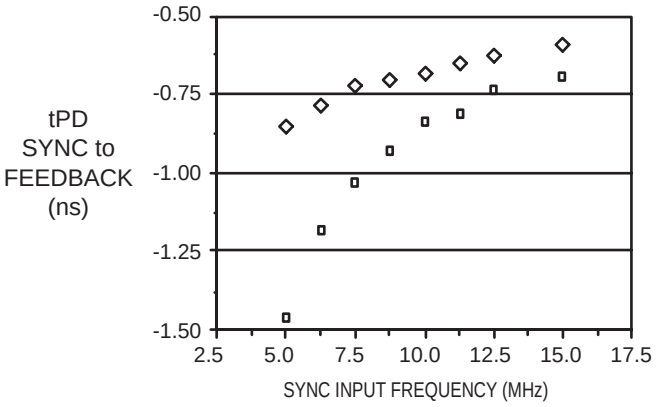
6. The t_{SKEWr} specification guarantees that the rising edges of outputs Q/2, Q0, Q1, Q2, Q3 and Q4 will always fall within a 500 ps window within one part. However, if the relative position of each output within this window is not specified, the 500 ps window must be added to each side of the t_{PD} specification limits to calculate the total part-to-part skew. For this reason the absolute distribution of these outputs is provided in Table 4. When taking the skew data, Q0 was used as a reference, so all measurements are relative to this output. The information in Table 4 is derived from measurements taken from the 14 process lots described in Note 1, over the temperature and voltage range.

Table 4. Relative Position of Outputs Q/2, Q0-Q4, 2X_Q,Within the 500 ps t_{SKEWr} Spec Window

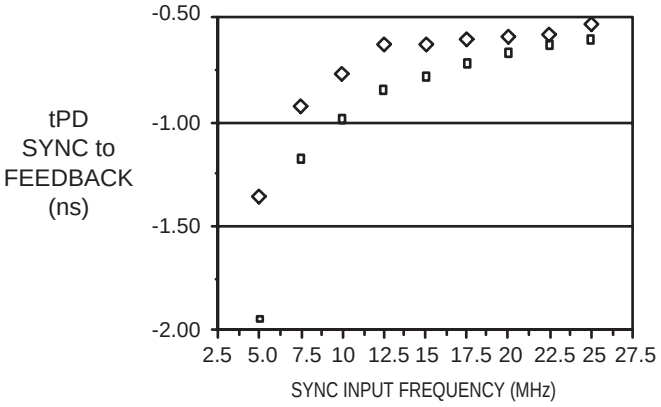
Output	- (ps)	+ (ps)
Q0	0	0
Q1	-72	40
Q2	-44	275
Q3	-40	255
Q4	-274	-34
Q/2	-16	250
2X_Q	-633	-35

7. Calculation of Total Output-to-Output skew Between Multiple Parts (Part-to-Part Skew)
   By combining the t_{PD} specification and the information in Note 5, the worst case Output-to-Output skew between multiple TS88915's connected in parallel can be calculated. This calculation assumes that all parts have a common SYNC input clock with equal delay that input signal to each part. This skew value is valid at the TS88915 output pins only (equally loaded), it does not include PCB trace delays due to varying loads.With a 1 MΩ resistor tied to analog VCC as shown in Note 4, the t_{PD} spec. limits between SYNC and the Q/2 output (connected to the FEEDBACK pin) are -1.05 ns and -0.5 ns. To calculate the skew of any given output between two or more parts, the absolute value of the distribution of that output given in Table 4 must be subtracted and added to the lower and upper t_{PD} spec limits respectively. For output Q2, [276-(-44)] = 320 ps is the absolute value of the distribution. Therefore [-1.05 - 0.32] = -1.37 ns is the lower t_{PD} limit, and [-0.5 + 0.32] = -0.18 ns is the upper limit. Therefore the worst case skew of output Q2 between any number of part is [(-1.37)-(-0.18)] = 1.19 ns. Q2 has the worst case skew distribution of any output, so 1.2 ns is the absolute worst case Output-to-Output skew between multiple parts.
8. Note 4 explains that the t_{PD} specification was measured and is guaranteed for the configuration of the Q/2 output connected to the FEEDBACK pin and the SYNC input running at 10 MHz. The fixed offset (t_{PD}) as described above has some dependence on the input frequency and what frequency the VCO is running. The graphs of Figure 6 demonstrate this dependence. The data presented in Figure 6 is from devices representing process extremes, and the measurements were also taken at the voltage extremes (V_{CC} = 5.25V and 4.75V). Therefore the data in Figure 6 is a realistic representation of the variation of t_{PD}.

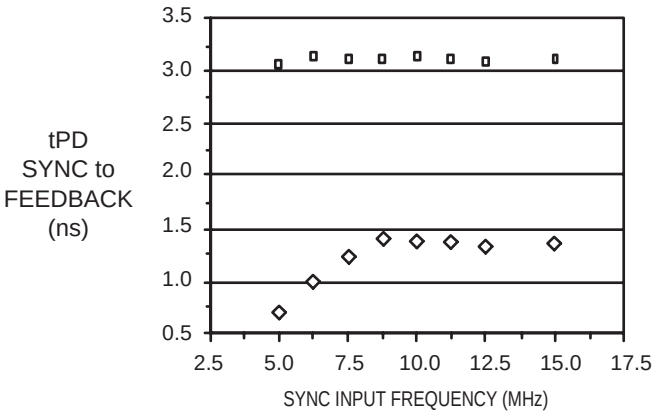
Figure 7.



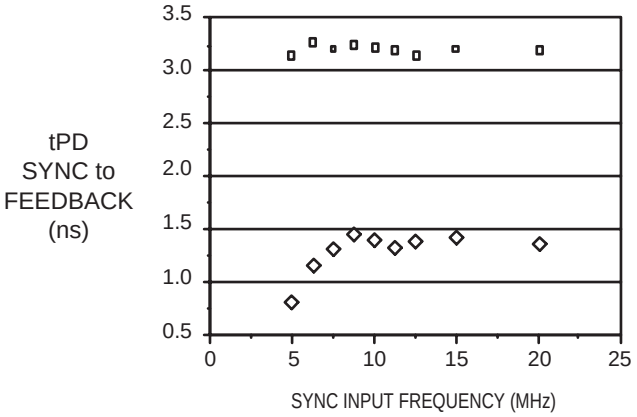
tPD versus Frequency for Q/2 output feed back, including process and voltage variation at 25°C (with 1 MΩ resistor tied to analog VCC)



tPD versus Frequency for Q4 output feed back, including process and voltage variation at 25°C (with 1 MΩ resistor tied to analog VCC)



tPD versus Frequency for Q/2 output feed back, including process and voltage variation at 25°C (with 1 MΩ resistor tied to analog GND)



tPD versus Frequency for Q4 output feed back, including process and voltage variation at 25°C (with 1 MΩ resistor tied to analog GND)

9. The Lock indicator pin (LOCK) will reliably indicate a phase-locked condition at SYNC input frequencies down to 10 MHz. At frequencies below 10 MHz, the frequency of correction pulses going into the phase detector from the SYNC and FEEDBACK pins may not be sufficient to allow the lock indicator circuitry to accurately predict a phase-locked condition. The TS88915T is guaranteed to provide stable phase-locked operation down to the appropriate minimum input frequency given in Table 3, even though the LOCK pin may be low at frequencies below 10 MHz.

Timing Notes

1. The TS88915T aligns rising edges of the FEEDBACK input and the SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between $V_{CC}/2$ crossing point of the appropriate output edges. All skews are specified as ‘windows’, not as a “deviation around a center point”.
3. If a “Q” output is connected to the FEEDBACK input (this situation is not shown), the “Q” output frequency would match the SYNC input frequency, the 2X_Q out-

put would run twice the SYNC frequency, and the Q/2 output would run at half the SYNC frequency. See Figure 7, Figure 8 and Figure 9 below.

Figure 8. Wiring Diagram and Frequency Relationship with Q/2 Output Feed Back

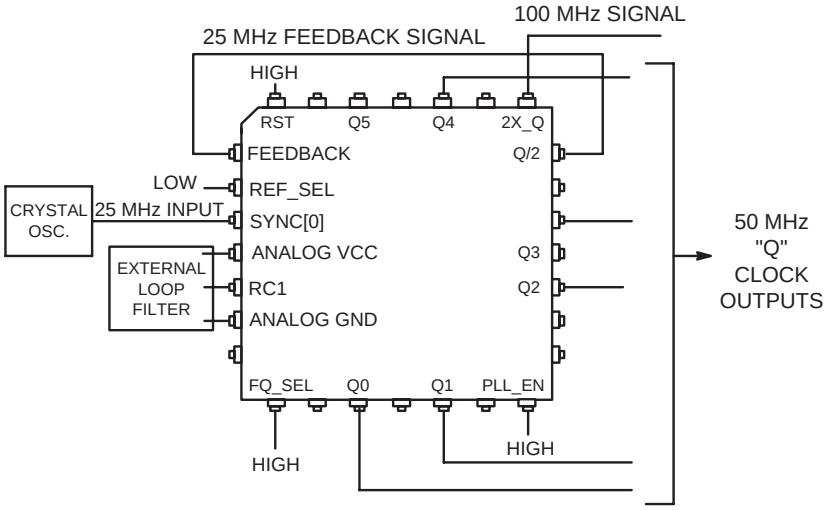


Figure 9. Wiring Diagram and Frequency Relationship with Q4 Output Feed Back

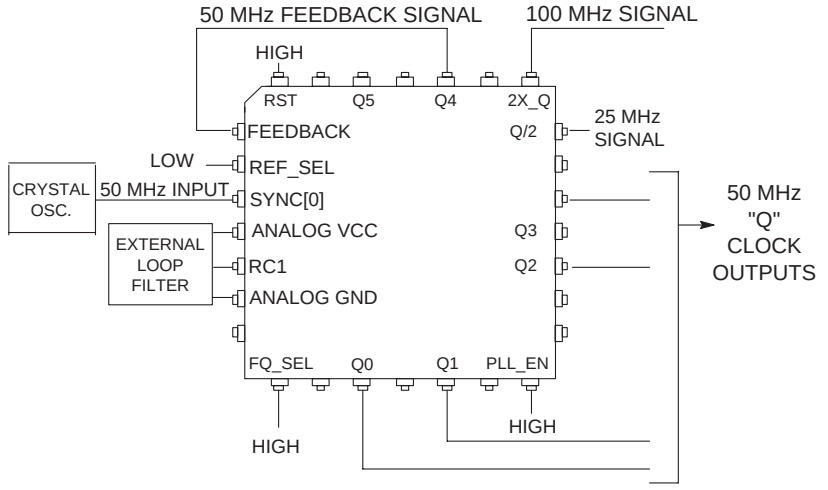
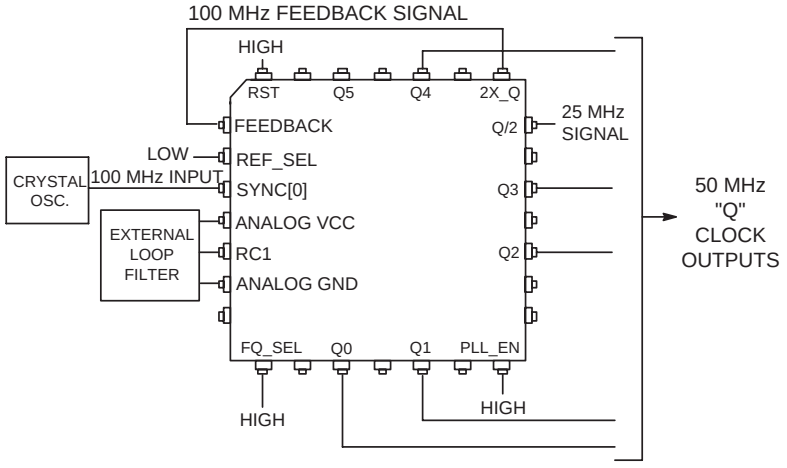


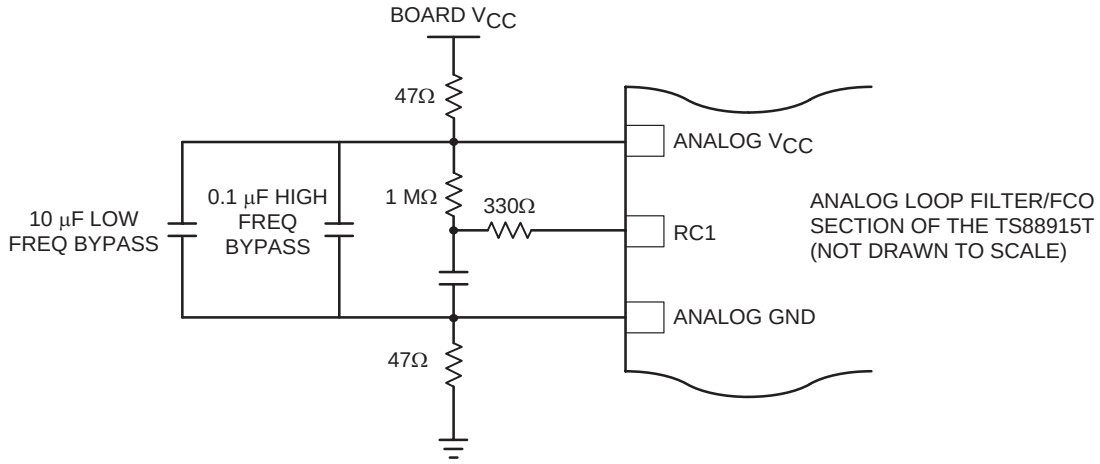
Figure 10. Wiring Diagram and Frequency Relationship with 2X_Q Output Feed Back



Notes Concerning Loop Filter and Board Layout Issues

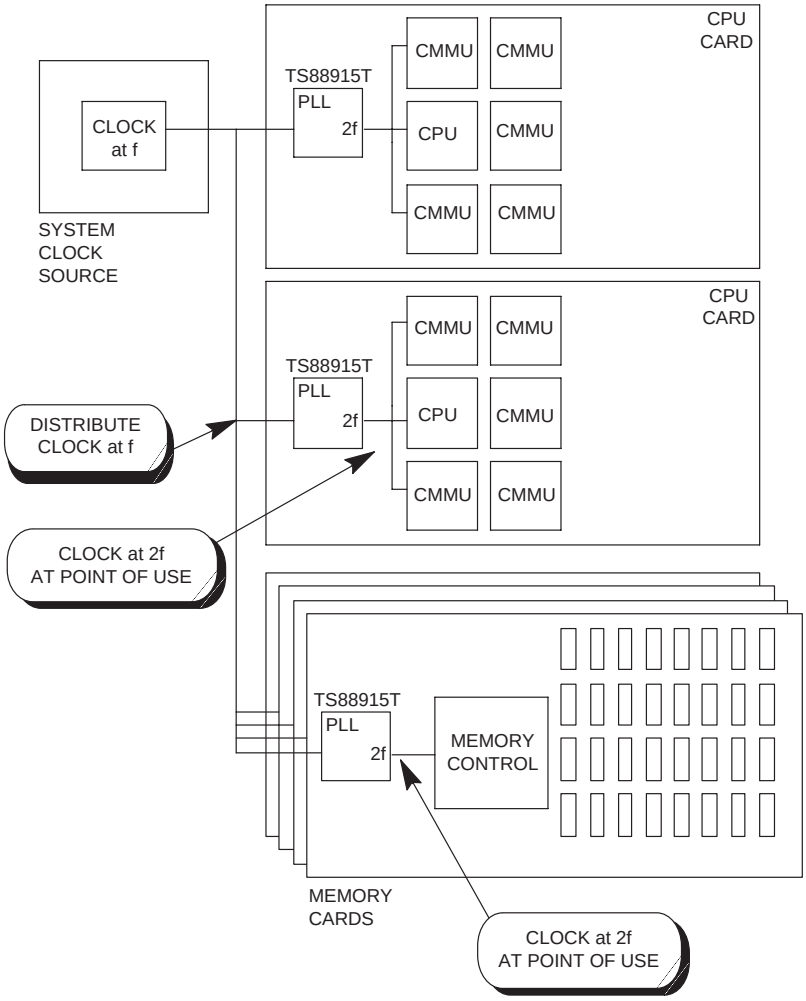
1. Figure 10 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter-free operation:
2. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.
3. The 47Ω resistors, the 10 µF low frequency bypass capacitor, and the 0.1 µF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 88915T's sensitivity to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100 mV step deviation on the digital V_{CC} supply will cause no more than 100 ps phase deviation on the 88915T outputs. A 250 mV step deviation on V_{CC} using the recommended filter values should cause no more than a 250 ps phase deviation; if a 25 µF bypass capacitor is used (instead of 1 µF) a 250 mV V_{CC} step should cause no more than a 100 ps phase deviation. If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88915T's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 10 is to give the 88915T additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.
4. There are no special requirements set forth for the loop filter resistors (1 MΩ and 330Ω). The loop filter capacitor (0.1 µF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.
5. The 1 MΩ reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead-band. If the VCO (2X_Q output) is running above 40 MHz, the 1 MΩ resistor provides the correct amount of current injection into the charge pump (2-3 µA). For the 70 and 100 MHz versions, if the VCO is running below 40 MHz, a 1.5 MΩ resistor should be used (instead of 1 MΩ).
6. In addition to the bypass capacitors used in the analog filter of Figure 10, there should be a 0.1 µF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88915T outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the package as possible.

Figure 11. Recommended Loop Filter and Analog Isolation Scheme for the TS88915T



Note: A separate analog power supply is not necessary and should not be used. Following these prescribed guidelines is all that is necessary to use the TS88915T in a normal digital environment.

Figure 12. Representation of a Potential Multi-Processing Application Utilizing the TS88915T for Frequency Multiplication and Low Board-to-board Skew



TS88915T System Level Testing Functionality

Tri-State functionality has been added to the TS88915T to ease system board testing. Bringing the $\overline{OE}/\overline{RST}$ pin low will put all outputs (except for LOCK) into a high impedance state. As long as the PLL_EN pin is low, the Q0-Q4, Q5 and Q/2 outputs will remain in the low state after the $\overline{OE}/\overline{RST}$ until a falling SYNC edge is seen. The 2X_Q output will be the inverse of the SYNC signal in this mode. If the tri-state functionality will be used, a pull-up or a pull-down resistor must be tied to the FEEDBACK input pin to prevent it from floating when the feedback output goes into high impedance.

With the PLL_EN pin low the selected SYNC signal is gated directly into the signal clock distribution network, bypassing and disabling the VCO. In this mode the outputs are directly driven by the SYNC input (per the block diagram). This mode can also be used for low frequency board testing.

Note: If the outputs are put into 3-state during normal PLL operation, the loop will be broken and phase-lock will be lost. It will take a maximum of 10 ms (t_{LOCK} spec) to regain phase-lock after the $\overline{OE}/\overline{RST}$ pin goes back high.

Preparation For Delivery

Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535.

Certificate of Compliance

Atmel offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

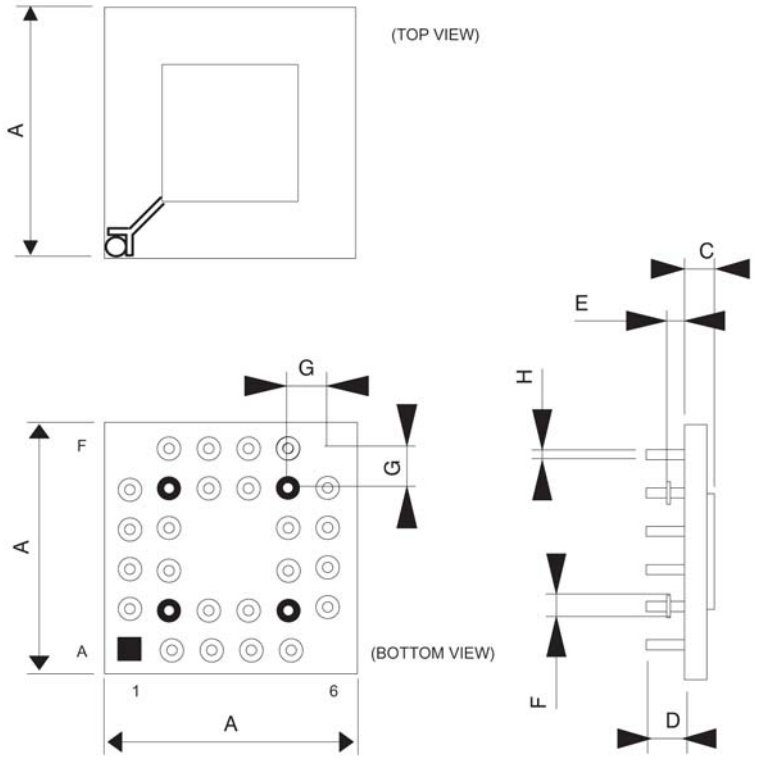
Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

- Devices Should Be Handled On Benches With Conductive And Grounded Surfaces
- Ground Test Equipment, Tools And Operator
- Do Not Handle Devices By The Leads.
- Store Devices In Conductive Foam Or Carriers.
- Avoid Use Of Plastic, Rubber, Or Silk In Mos Areas.
- Maintain Relative Humidity Above 50 Percent If Practical.

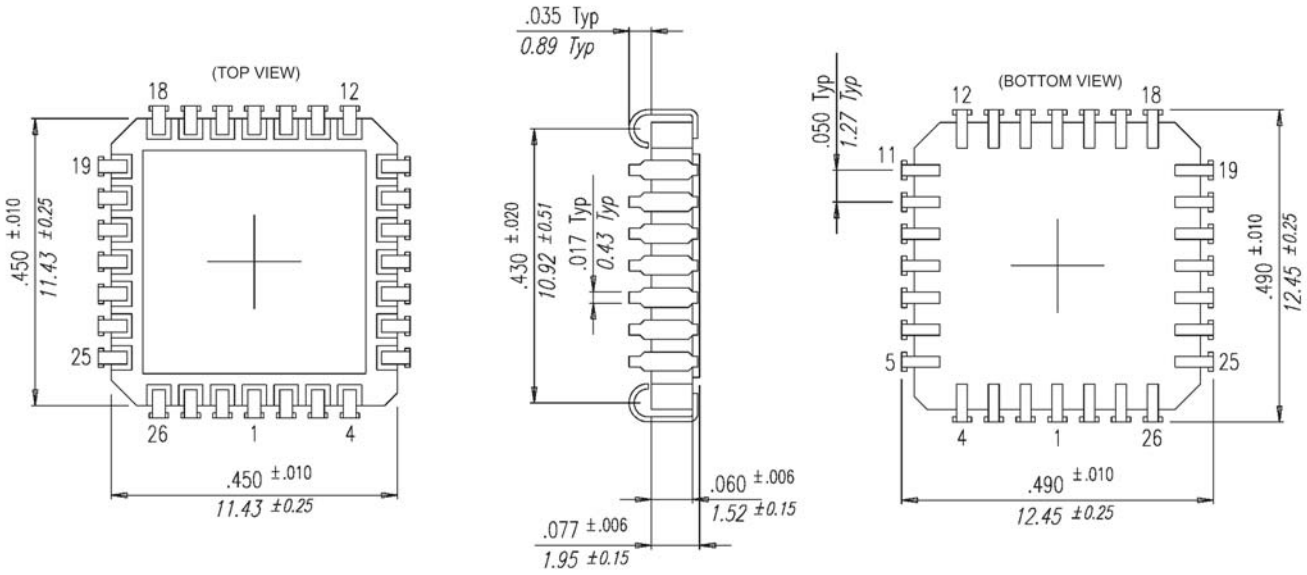
Package Mechanical Data

29-pin PGA



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.594	0.606	15.087	15.392
C	-	0.107	-	2.72
D	0.17	0.19	4.32	4.83
E	0.045	0.055	1.143	1.397
F	0.045	0.055	1.143	1.397
G	0.100 BSC		2.54 BSC	
H	0.017	0.019	0.43	0.48

28-pin LDCC



Note: This package is pin compatible with PLCC

Ordering Information

TS88915T M R B / T 70

Device Type

Temperature range : Tc
M : -55, +125°C
V : -40, +85°C

Package :
R: PGA
W: LDCC

Screening level :
__ : Standard
B/T: according to MIL-STD-883
D/T: Burn-in

Maximum Output Frequency :
70: 70 MHz
100: 100 MHz

Note: For availability of the different versions, contact your Atmel sales office.

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