CY14NVSRAMKIT-001

nvSRAM Development Kit User Guide

Doc. # 002-03522 Rev. *A

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Contents

Safety Information

Regulatory Compliance

The CY14NVSRAMKIT-001 nvSRAM Development Kit is intended for use as a memory development platform for hardware or software in a laboratory environment. The board is an open-system design, which does not include a shielded enclosure. Therefore, the board may cause interference with other electrical or electronic devices in close proximity.

Attaching additional wiring to this product or modifying the product operation from the factory default may affect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

The CY14NVSRAMKIT-001, as shipped from the factory, has been verified to meet with the requirements of CE as a Class A product.

The CY14NVSRAMKIT-001 contains ESD-sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused CY14NVSRAMKIT-001 boards in the protective shipping package.

End-of-Life/Product Recycling

The end-of-life cycle for this kit is five years from the date of manufacture mentioned on the back of the box. Contact your nearest recycler to discard the kit.

General Safety Instructions

ESD Protection

ESD can damage boards and associated components. Cypress recommends that the user perform procedures only at an ESD workstation. If an ESD workstation is not available, use appropriate ESD protection by wearing an antistatic wrist strap attached to the chassis ground (any unpainted metal surface) on the board when handling parts.

Handling Supercapacitors

The CY14NVSRAMKIT-001 board uses a 0.1 Farad supercapacitor for RTC backup. It is advisable not to touch the capacitor positive pin (anode) with a bare hand or a conducting material to avoid electrical shock.

Handling Boards

CY14NVSRAMKIT-001 boards are sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static-free surface. Use a conductive foam pad if available. Do not slide board over any surface.

1. Introduction

Thank you for your interest in the CY14NVSRAMKIT-001 nvSRAM Development Kit (DVK). The kit (shield) is designed as an easy-to-use and inexpensive development kit, showcasing the features of Cypress high-speed, parallel access (asynchronous interface), nonvolatile SRAM (nvSRAM). This kit works in conjunction with the SK-FM4-U120-9B560 FM4 MCU Evaluation Board, a starter kit for ARM® Cortex®-M4-based devices. You will need both kits to demonstrate the operation described in this guide. This board features a 16-Mbit parallel nvSRAM with real time clock (RTC) and associated circuits, super capacitor for RTC backup in the absence of the VCC supply, FM4 mounting headers, and test pins. This kit supports 3.3-V power supply.

Cypress nvSRAM is built on 130-nm technology and combines a silicon-oxide-nitride-oxide-silicon (SONOS) nonvolatile data storage cell with a high-performance SRAM cell. The parallel nvSRAMs provide the fastest nonvolatile writes at bus speed. They do not have any write delays and data is instantly nonvolatile. Because of fast write speeds, parallel nvSRAMs need to be active for short periods, yielding low energy consumption. Endurance is unlimited for writing into SRAM. The SRAM data is automatically saved to nonvolatile memory upon power down.

1.1 Kit Contents

The CY14NVSRAMKIT-001 DVK includes the following contents, as shown in Figure 1-1:

- CY14NVSRAMKIT-001 DVK board
- Quick Start Guide

Figure 1-1. Kit Contents

Visit www.cypress.com/CY14NVSRAMKIT-001 for more information. Inspect the contents of the kit; if you find any part missing, contact your nearest Cypress sales office for help.

1.2 Getting Started

This guide helps you to get acquainted with the CY14NVSRAMKIT-001 DVK. The Kit Installation chapter on page 10 describes the installation of the kit software. The Kit Overview chapter on page 14 explains the features of the kit. The Kit Operation chapter on page 20 explains how to program and run the kit. The Kit Software chapter on page 32 explains the GUI. The Kit Example Firmware chapter on page 41 explains the nvSRAM access APIs and pseudo codes. The Appendix on page 49 provides the kit block diagram, schematics, pin assignment, and the bill of materials (BOM).

1.3 Additional Learning Resources

Visit www.cypress.com/go/nvsram for additional learning resources in the form of datasheets and application notes.

Information on the companion FM4 MCU Evaluation Board resources is available at:
FM4-U120-9B560 FM4 MCU Evaluation Board

1.4 Technical Support

For assistance, visit Cypress Support or contact customer support at +1 (800) 541-4736 Ext. 2 (in the USA) or +1 (408) 943-2600 Ext. 2 (International).

1.5 Documentation Conventions

Table 1-1. Document Conventions for Guides

Convention	Usage
`Courier New`	Displays file locations, user entered text, and source code: `C:\ ...cd\icc\`
Italics	Displays file names and reference documentation.
[**Bracketed, Bold**]	Displays keyboard commands in procedures: [**Enter**] or [**Ctrl**] [**C**]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: 2 + 2 = 4
Text in gray boxes	Describes cautions or unique functionality of the product.

1.6 Acronyms and Definitions

Terms	Description
API	application programming interface
BOM	bill of materials
DAP	debug and programming
DNI	do not install
DVK	development kit
EBI	external bus interface
FBGA	fine-pitch ball grid array
MCU	microcontroller unit
nvSRAM	nonvolatile static random access memory
QSG	quick start guide
RTC	real time clock
TSOP	thin small outline package
UG	user guide

2. Kit Installation

This section describes the installation and uninstallation of the FM4 MCU Evaluation Board software, driver, and the CY14NVSRAMKIT-001 DVK contents.

2.1 Install SK-FM4-U120-9B560 Kit Software and Driver

The CY14NVSRAMKIT-001 DVK works with the FM4-U120-9B560 FM4 MCU Evaluation Board. Therefore, all software and drivers for that evaluation board need to be installed to work with the CY14NVSRAMKIT-001 DVK. Follow these steps to install the FM4-related software and drivers.

1. Download the “Complete Driver, Documentation, Software and Tools package” from the Documentation table on the FM4-U120-9B560 FM4 MCU Evaluation Board web page.

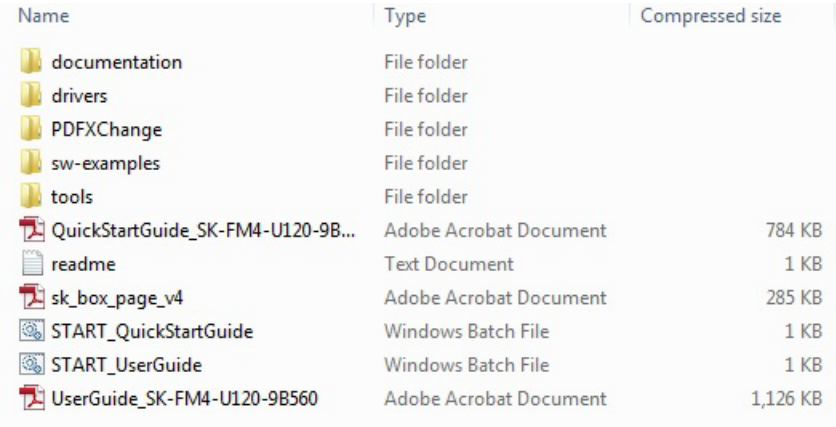
   Click Driver, Documentation, Software and Tool package to download the zip file.

   Table 2-1. FM4 MCU Documentation

User Guide	UserGuide_FM4-U120-9B560.pdf
Quick Start Guide	QuickStartGuide_FM4-U120-9B560.pdf
Schematics	FM4-U120-9B560-1v3_schematic.pdf
Complete Driver, Documentation, Software & Tools package	FM4-U120-9B560_CDv13.zip

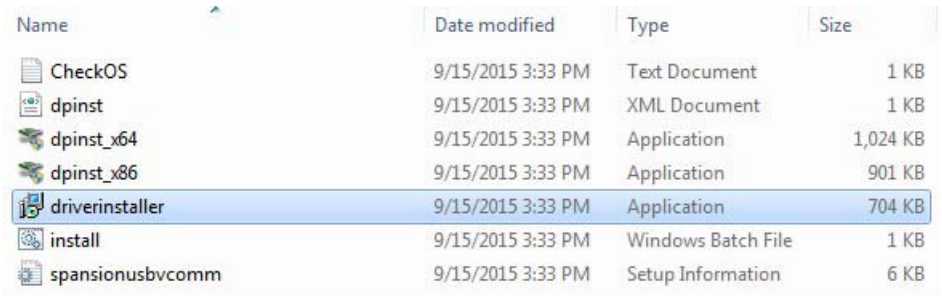
2. Save the downloaded file and extract the folders and files to a local folder. Figure 2-1 shows the contents of FM4-U120-9B560_CDv13.zip. You can download the latest version of the SK-FM4-U120-9B560 kit driver, documentation, software, and tool at the FM4 MCU Evaluation Board webpage.

   Figure 2-1. FM4-U120-9B560_CDv13.zip File Contents



3. To install the driver for the Debug and Programming (DAP) port (CN3) of the FM4-U120-9B560 FM4 MCU Evaluation Board, open **\drivers\cmsis-dap** and click **driverinstaller**.

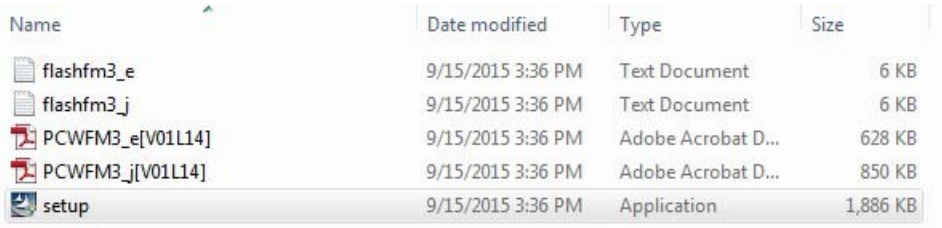
   Figure 2-2. Install CMSIS-DAP Driver



   When the Windows security dialog pops up, click **Install this driver software anyway** to continue the driver installation.

4. To install the Flash MCU Programmer required to program the FM4 MCU Evaluation Board with the nvSRAM firmware (*.srec* file), open **\tools\PCWFM** and click **setup**.

   Figure 2-3. Install Flash MCU Programmer



The default installation location is as follows:

Windows 7 (64-bit): `C:\Program Files (x86)\Spansion\FLASH MCU Programmer\FM3`

Windows 7 (32-bit): `C:\Program Files\Spansion\FLASH MCU Programmer\FM3`

2.2 Uninstall SK-FM4-U120-9B560 Kit Software and Driver

To uninstall the software, go to **Start** > **Control Panel** > **Programs and Features**; select the appropriate software package and click **Uninstall**.

2.3 Install CY14NVSRAMKIT-001 DVK Contents

Follow these steps to install the CY14NVSRAMKIT-001 DVK contents.

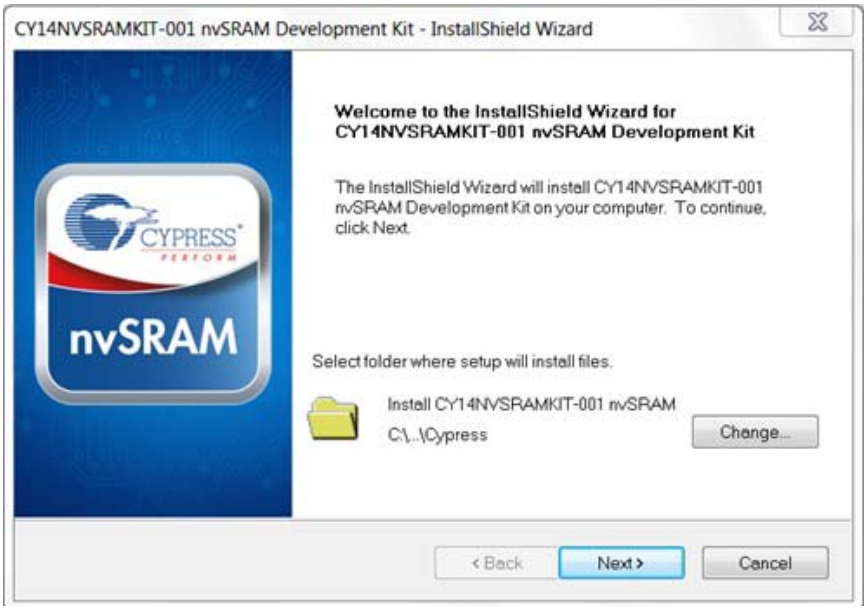
1. Download the kit software from www.cypress.com/CY14NVSRAMKIT-001 (see Figure 2-4).

   Figure 2-4. nvSRAM DVK Software

   The CY14NVSRAMKIT-001 Kit Setup executable file installs the kit contents, which include kit software, firmware, hardware files, and user documents.

2. The kit startup screen appears as shown in Figure 2-5.

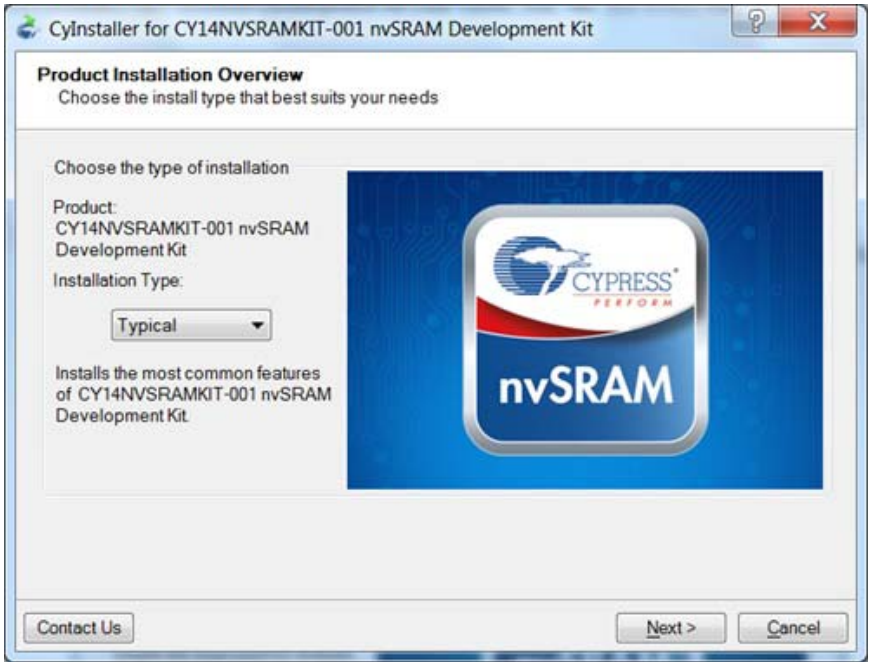
Figure 2-5. Kit Installer Startup Screen



Select the folder in which you want to install the CY14NVSRAMKIT-001 kit-related files or keep the default (recommended). Choose the directory and click **Next**.

3. Select the **Typical** installation type in the Product Installation Overview window, as shown in Figure 2-6. Click **Next**.

Figure 2-6. Product Installation Overview Window



When the installation begins, a list of packages appears on the installation page. A green check mark appears next to each package after successful installation.

4. If this is the first Cypress product that you have installed, enter your contact information or select **Continue without Contact Information**. Click **Finish** to complete the kit installation.

When the installation is complete, the kit contents and software are available as follows:
`<Install_Directory>\CY14NVSRAMKIT-001 nvSRAM Development Kit\1.0`
`<Install_Directory>\nvSRAM Kit Software\1.0`

The default locations are as follows:

Kit:

Windows 7 (64-bit): `C:\Program Files (x86)\Cypress\CY14NVSRAMKIT-001 nvSRAM Development Kit\1.0`

Windows 7 (32-bit): `C:\Program Files\Cypress\CY14NVSRAMKIT-001 nvSRAM Development Kit\1.0`

Software:

Windows 7 (64-bit): `C:\Program Files (x86)\Cypress\nvSRAM Kit Software\1.0`
Windows 7 (32-bit): `C:\Program Files\Cypress\ nvSRAM Kit Software\1.0`

Note: For Windows 7/8/8.1 users, the installed files and the folder are read-only. To modify these files or folders, copy them to another location on your system, change the folder property to disable the Read-only attribute, and modify the folder.

After the installation is complete, the following are installed on your computer:

- Kit documents
  - Quick Start Guide
  - Kit Guide
  - Release Notes
- Firmware
  - Kit firmware project
- Software
  - nvSRAM kit software
- Hardware
  - Schematic
  - Layout
  - Gerber
  - PCB assembly drawing
  - Bill of Materials (BOM)

2.4 Uninstall CY14NVSRAMKIT-001 DVK Contents

The software can be uninstalled using one of the following methods:

- Go to **Start** > **Control Panel** > **Programs and Features**; select the appropriate software package and click **Uninstall**.
- Go to **Start** > **All Programs** > **Cypress** > **Cypress Update Manager** > **Cypress Update Manager**.
  - Select the **CY14NVSRAMKIT-001 Kit Rev **** row and click **Uninstall**.
  - Select the **nvSRAM Kit Rev **** row and click **Uninstall**.

  Note: This method will uninstall only the kit software and not all the other software that may have been installed along with the kit software.

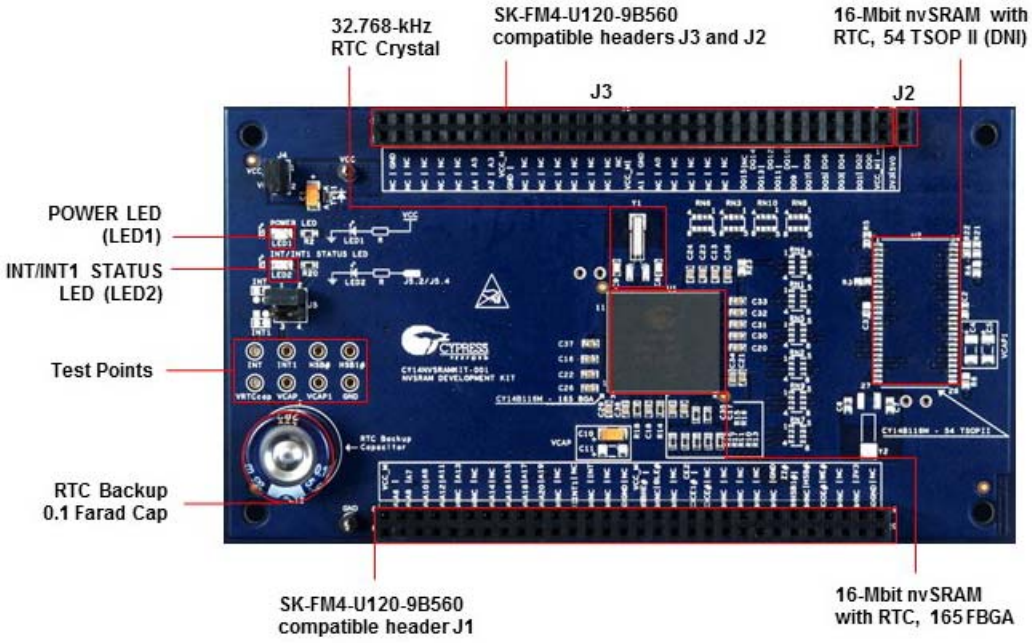
3. Kit Overview

3.1 CY14NVSRAMKIT-001 Kit Overview

The CY14NVSRAMKIT-001 DVK can be used to understand the features of parallel nvSRAMs (asynchronous interface). The DVK is an add-on board, which contains a 16-Mbit, x16, 3.3 V, parallel nvSRAM with RTC. It provides two 30x2 headers (J1 and J3) compatible with an SK-FM4-U120-9B560 FM4 MCU Evaluation Board. An additional two-pin header 2x1 (J2) is available next to J3 to be used as a guide for mounting the board in the correct orientation. The kit operates using a 3.3-V power supply from the baseboard. The CY14NVSRAMKIT-001 nvSRAM DVK consists of the following blocks as shown in Figure 3-1.

- 16-Mbit (1Mx16), parallel nvSRAM with RTC
- SK-FM4-U120-9B560 compatible headers
- 3.3-V VCC power supply
- POWER LED (LED1)
- INT/INT1 STATUS LED (LED2)
- Test points for HSB (HSB# and HSB1#) and RTC (INT and INT1)
- Do Not Install (DNI) footprint for the nvSRAM with RTC in 54 TSOP II
- 0.1 Farad super capacitor, which provides RTC backup for more than two days

Figure 3-1. CY14NVSRAMKIT-001 DVK Board Markup



3.2 Kit Introduction and Configuration Guide

The following sections describe various aspects of the kit hardware and the kit setup.

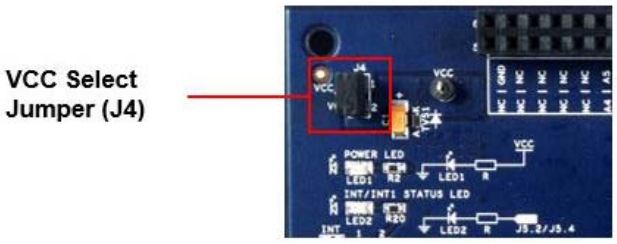
3.2.1 Power Supply Jumper

The CY14NVSRAMKIT-001 DVK hardware operates at 3.3 V, selected through header J4, as shown in Figure 3-2. The factory default jumper setting is 3.3 V (short pins 1 and 2 of J4).

CAUTION

- Do not power the CY14NVSRAMKIT-001 board through an external power source. The board is designed to be powered by the FM4 MCU base board.
- The CY14NVSRAMKIT-001 operates from 2.7 V to 3.6 V. Exceeding the maximum voltage limit (3.6 V) can damage the board.

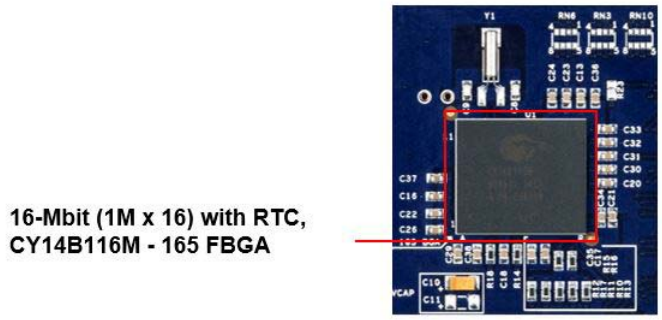
Figure 3-2. VCC Select Jumper



3.2.2 Parallel nvSRAM Device

Figure 3-3 shows the 16-Mbit, 1Mx16, 3.3 V, parallel nvSRAM with RTC part in the 165 FBGA package option.

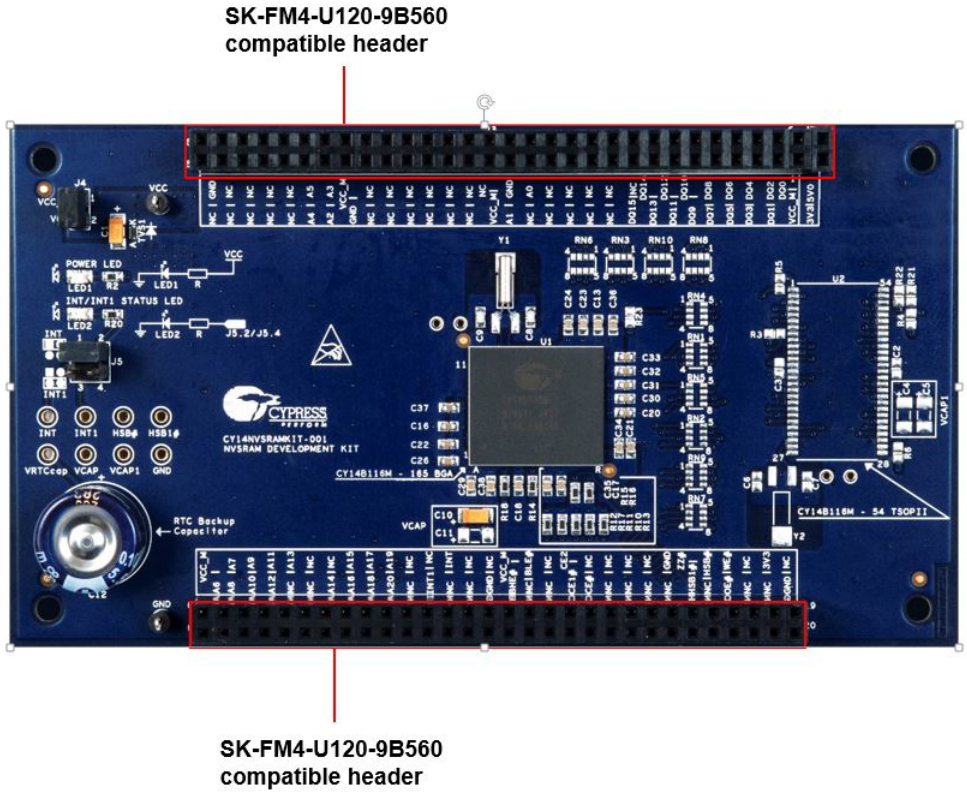
Figure 3-3. Cypress Parallel nvSRAM Device on the Board



3.2.3 Headers to FM4 MCU Evaluation Board (SK-FM4-U120-9B560)

Figure 3-4 shows the headers to the SK-FM4-U120-9B560 board – J1, J2, and J3. You can plug the DVK board onto the FM4 MCU Evaluation Board through these connectors. For the schematic, refer to the Appendix on page 49.

Figure 3-4. Headers to FM4 MCU Evaluation Board (SK-FM4-U120-9B560)



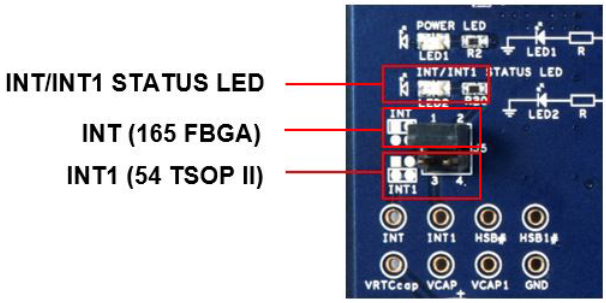
3.2.4 Interrupt (INT and INT1) Pins

The DVK board provides the nvSRAM RTC interrupt output via INT and INT1 pins for the 165 FBGA and 54-TSOP II packages respectively; see Figure 3-5. Loading a jumper to short pin 1 and 2 of the J5 connects the 165 FBGA nvSRAM interrupt output to the INT/INT1 STATUS LED. Similarly, loading a jumper to short pin 3 and 4 of the J5 connects the 54 TSOP II nvSRAM interrupt output to the INT/INT1 STATUS LED. The default loading for jumper J5 shorts pin 1 and 2 position.

The INT1 pin functionality is not available on the kit because the 54 TSOP II package is not populated by default.

CAUTION: When the 54 TSOP II nvSRAM is populated (by the user), it is recommended to connect only one jumper either on pin 1 and pin 2 or on pin 3 and pin 4 of J5 to monitor the interrupt outputs. Connecting two jumpers to enable the interrupt of both devices on the INT/INT1 STATUS LED can cause output contention when the output driver of either nvSRAM is configured as active HIGH (push or pull) output.

Figure 3-5. Interrupt Pins



3.2.5 Test Points

The DVK board provides INT, INT1, HSB#, HSB1#, VRTCcap, VCAP, VCAP1, VCC, and GND test points as shown in Figure 3-6. These test points are not loaded by default.

Figure 3-6. Test Points

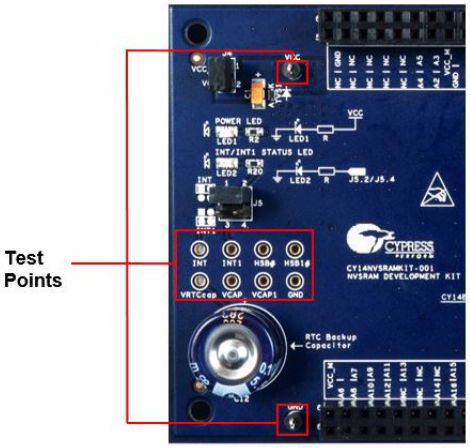


Table 3-1. Test Points

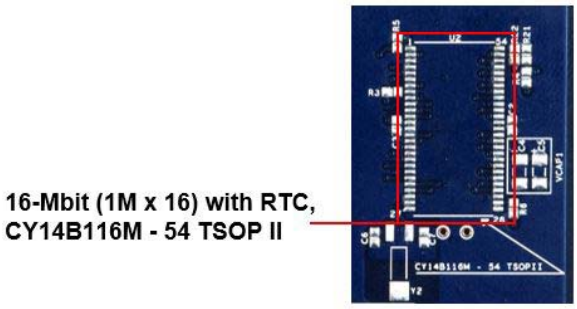
Test Points	Description
VCC	Test point for the kit board VCC
INT	Test point for the 165 FBGA nvSRAM interrupt output pin (INT)
INT1	Test point for the 54 TSOP II nvSRAM interrupt output pin (INT)
HSB#	Test point for the 165 FBGA nvSRAM HSB# pin
HSB1#	Test point for the 54 TSOP II nvSRAM HSB# pin
VRTCcap	Test point for the RTC backup capacitor
VCAP	Test point for the 165 FBGA nvSRAM VCAP pin
VCAP1	Test point for the 54 TSOP II nvSRAM VCAP pin
GND	Test point for the kit board ground

CAUTION: The VCC test point is only for probing and measurement purposes. Do not power the kit using this test point to avoid any damage to the board.

3.2.6 54 TSOP II - Not Populated by Default

The DVK board provides a footprint option for the 16-Mbit nvSRAM in the 54 TSOP II package. You can mount a 16-Mbit (1M x 16), 3.3 V, parallel nvSRAM device to evaluate the 54 TSOP II package in addition to the default 165 FBGA option on the DVK board. An independent chip select control is provided for the 54 TSOP II package, which enable access to the second device on the board with an appropriate firmware modification.

Figure 3-7. 54 TSOP II - Not Populated by Default

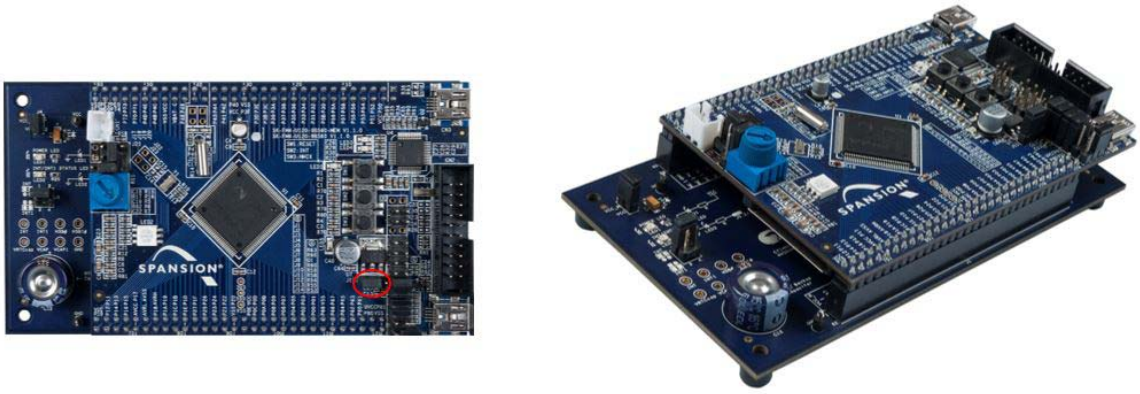


3.3 nvSRAM and MCU Kit Connection

The FM4 MCU Evaluation Board is plugged onto the CY14NVSRAMKIT-001 through three connectors: J1, J2, and J3, as shown in Figure 3-8.

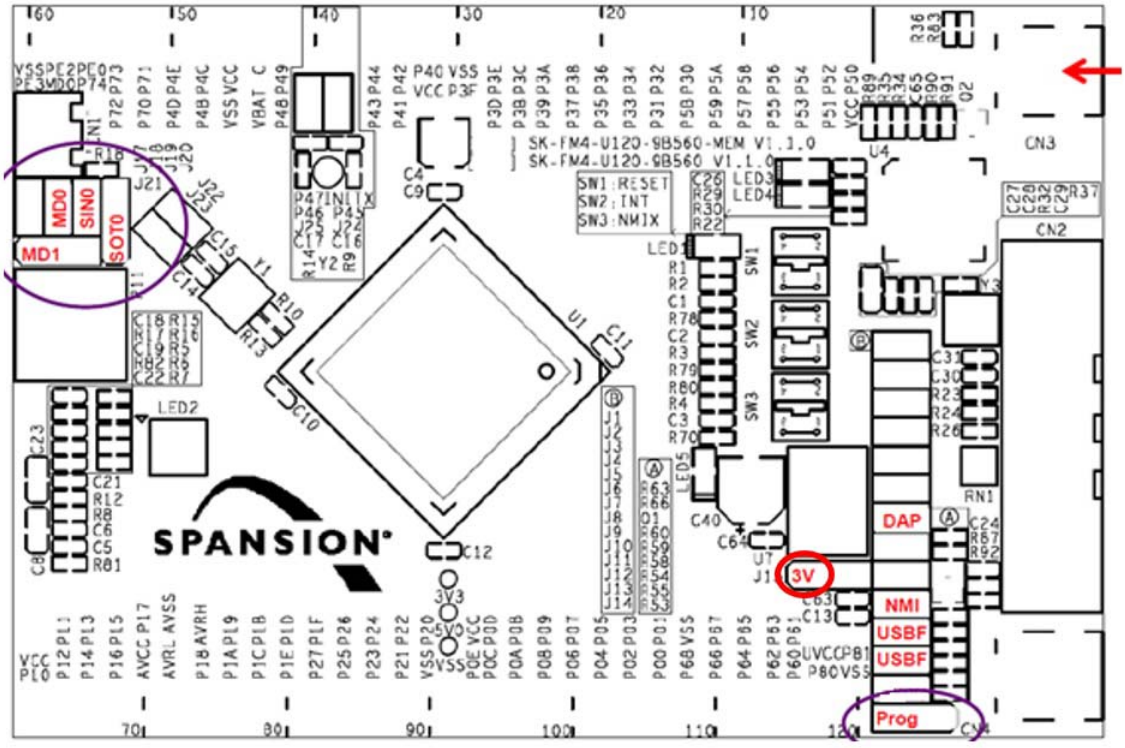
CAUTION: Change the voltage setting jumper J15 on the FM4 MCU Evaluation Board to the **3V** position as indicated in Figure 3-8 and Figure 3-9 before powering the board.

Figure 3-8. FM4 MCU Evaluation Board Mounted on CY14NVSRAMKIT-001



CAUTION: The FM4 MCU Evaluation Board is plugged onto the CY14NVSRAMKIT-001 DVK through its compatible headers J1, J2, and J3. Because J1 and J3 are high pin-count connectors on the FM4 MCU Evaluation Board, removing the FM4 MCU Evaluation Board can be difficult and may lead to bending its J1 and J3 connector pins. Therefore, take care when removing the FM4 MCU Evaluation Board from the setup. Sliding the FM4 MCU Evaluation Board out of headers slowly and evenly will reduce the risk of bending connector pins.

Figure 3-9. 3.3-V Setting on FM4 MCU Evaluation Board



4. Kit Operation

This section describes the setup to program and run the FM4 MCU Evaluation Board to execute the nvSRAM access on the CY14NVSRAMKIT-001 DVK.

4.1 Program the FM4 MCU Evaluation Board

The FM4 MCU is a 32-bit ARM Cortex-M4 microcontroller device. A firmware code is required to configure the MCU as the nvSRAM host controller to access the nvSRAM device on the CY14NVSRAMKIT-001 DVK. The firmware example code provided with the DVK collateral supports different nvSRAM functionalities such as write/read memory access, RTC register access, hardware store, software store, and sleep mode by toggling the dedicated sleep (ZZ#) pin on the nvSRAM.

The FM4 MCU board requires the following setup for firmware programming; see Figure 4-1:

1. Set the Prog jumper to the Programming Mode.
2. Retain USBF, USBF, and NMI jumper settings.
3. Set the 3V jumper position for 3.3 V operation.
4. Set the DAP jumper.
5. Set SOT0, SIN0, MD0, and MD1 jumpers.
6. All other jumpers, not marked, should remain unconnected.
7. Connect the MCU board to a PC via the CN3 port for programming.

   Refer to A.6.4 Jumper Setting Table - FM4 MCU Evaluation Board Programming Mode on page 63 for more details.

Figure 4-1. FM4 MCU Evaluation Board Jumper Setting in Programming Mode

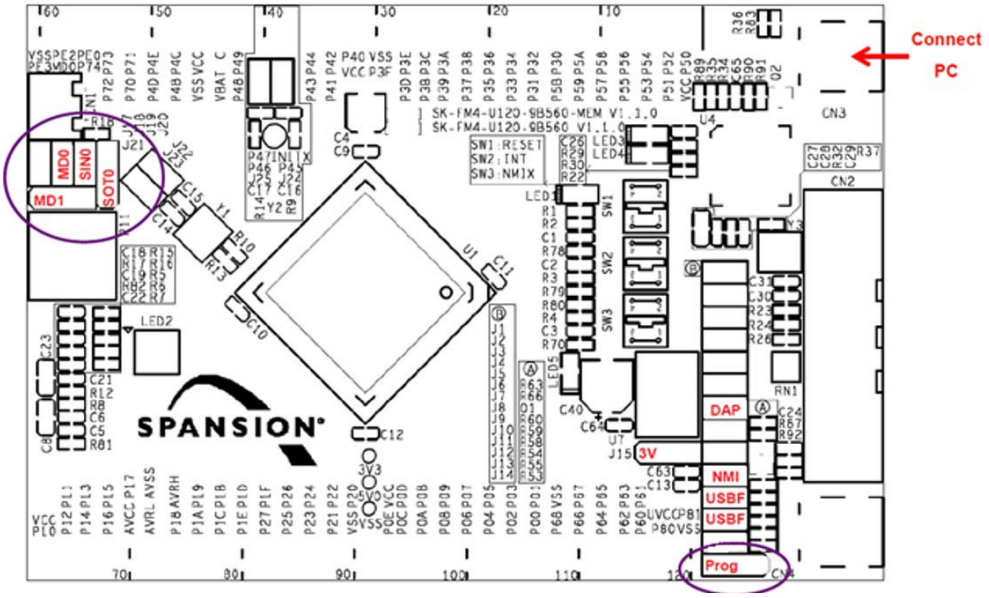
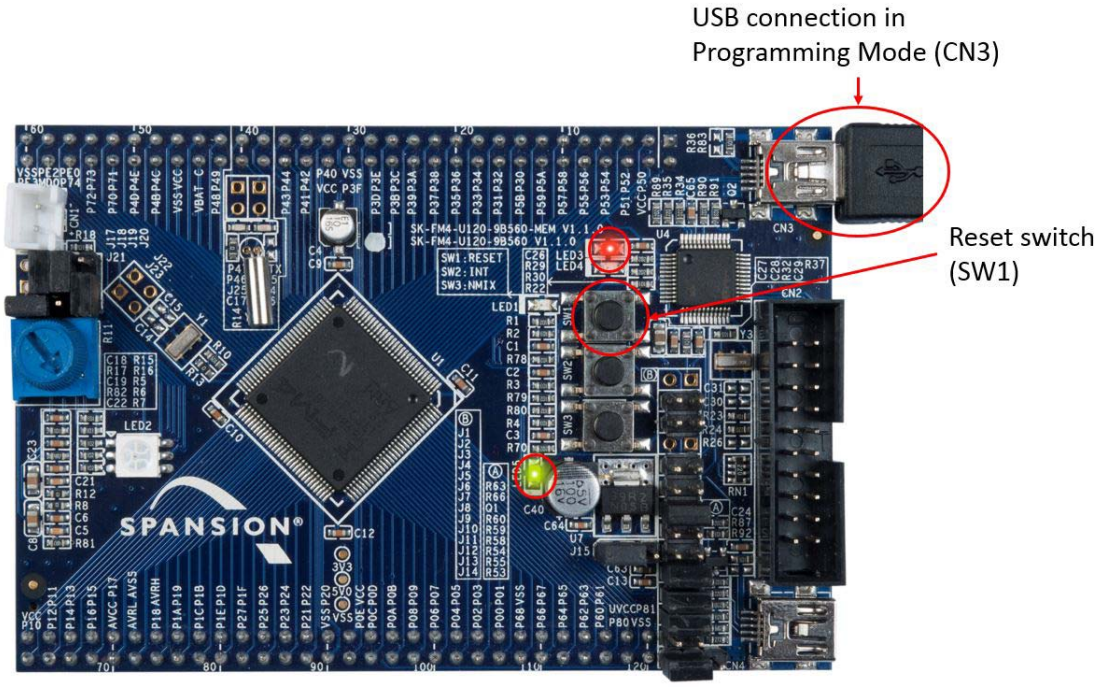


Figure 4-2. FM4 MCU Evaluation Board Setup in Programming Mode



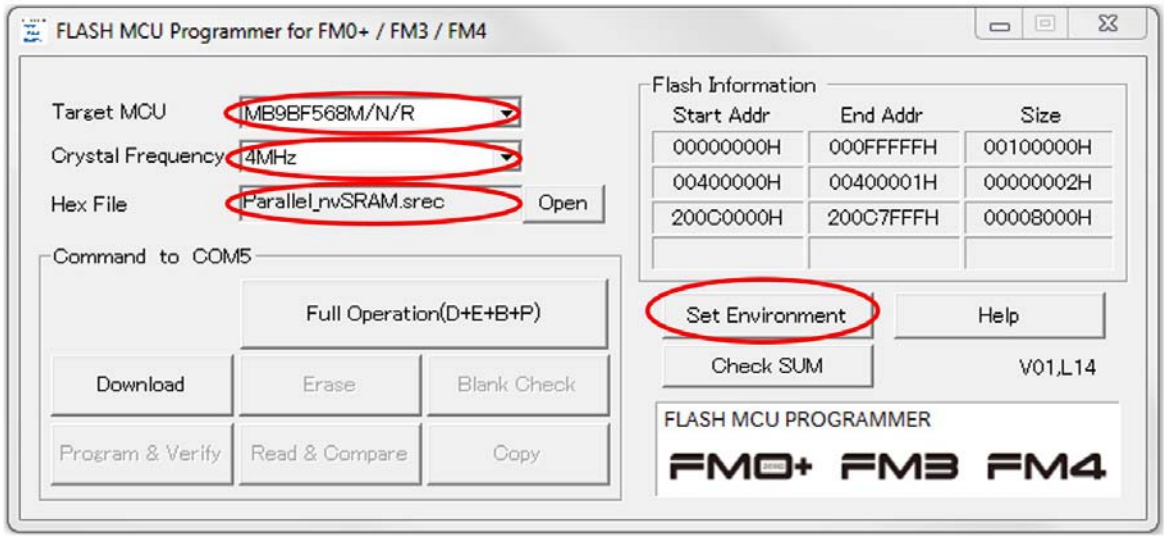
Note: LED5 (Green) indicates the board is powered from the USB port via the CN3 connector. LED3 (Red) indicates the board is powered in the Programming (and Debugging) mode. CY14NVSRAMKIT-001 connection to the FM4 MCU Evaluation Board is not necessary during programming.

8. Run the Flash MCU Programmer: **Start** > **All Programs** > **FLASH MCU Programmer** > **FM3**. Alternatively, you can execute "flash.exe" at the following locations:

   Windows 7 (64-bit): `C:\Program Files (x86)\Spansion\FLASH MCU Programmer\FM3`

   Windows 7 (32-bit): `C:\Program Files\Spansion\FLASH MCU Programmer\FM3`

Figure 4-3. Flash MCU Programmer



a. Select Target MCU: **MB9BF568M/N/R**

b. Select Crystal Frequency: **4MHz**

c. Select Hex File: `<Install_Directory>\CY14NVSRAMKIT-001 nvSRAM Development Kit\1.0\Firmware\Binary\Parallel_nvSRAM.srec`

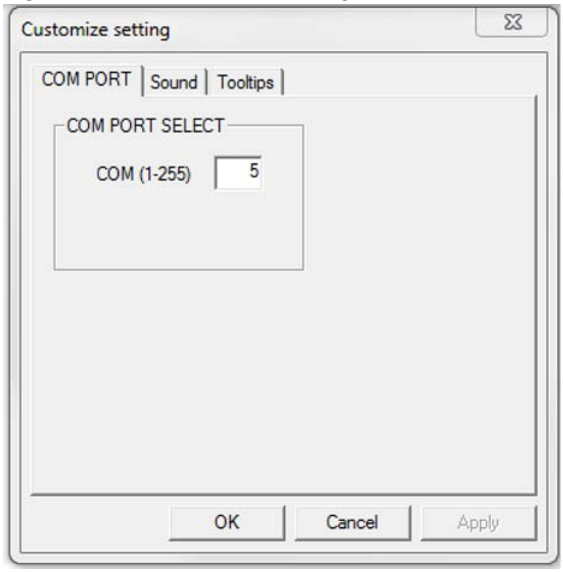
The default binary file location is as follows:

Windows 7 (64-bit): `C:\Program Files (x86)\Cypress\CY14NVSRAMKIT-001 nvSRAM Development Kit\1.0\Firmware\Binary\`

Windows 7 (32-bit): `C:\Program Files\Cypress\CY14NVSRAMKIT-001 nvSRAM Development Kit\1.0\Firmware\Binary\`

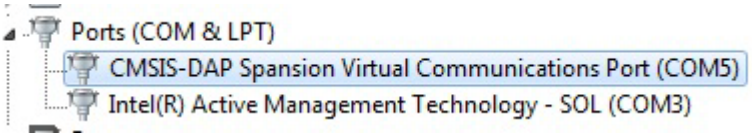
d. Select the Virtual COM-port by clicking the **Set Environment** button as shown in Figure 4-3. This will open a new 'Customize setting' window.

Figure 4-4. COM Port Setting



To identify the COM port for the Flash MCU Programmer: **Start** > **All Programs** > **Computer.** Right-click and select **Properties** > **Device Manager** > **Ports (COM & LPT)** and identify the **CMSIS-DAP Spansion Virtual Communications Port (COMx)**. For example, Figure 4-5 shows it is assigned to communication port 5 (COM5). Enter this value in COM to set the COM port.

Figure 4-5. Port Selection

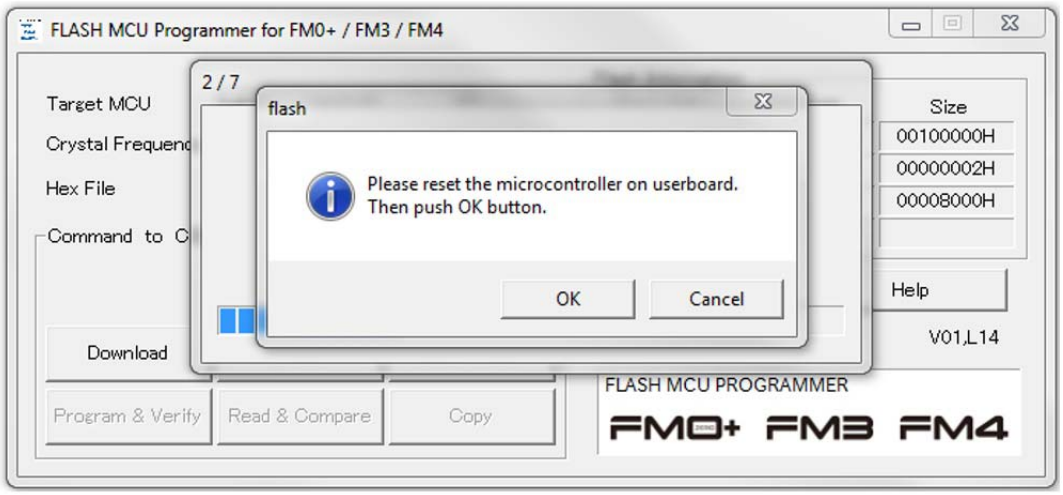


If the CMSIS-DAP Spansion Virtual Communications Port does not appear under **Ports (COM & LPT)**, then the driver is not installed. Refer to 2.1 Install SK-FM4-U120-9B560 Kit Software and Driver on page 10 to install the Debug and Programming (DAP) port (CN3) driver.

9. Click the **Full Operation** button to program the device.

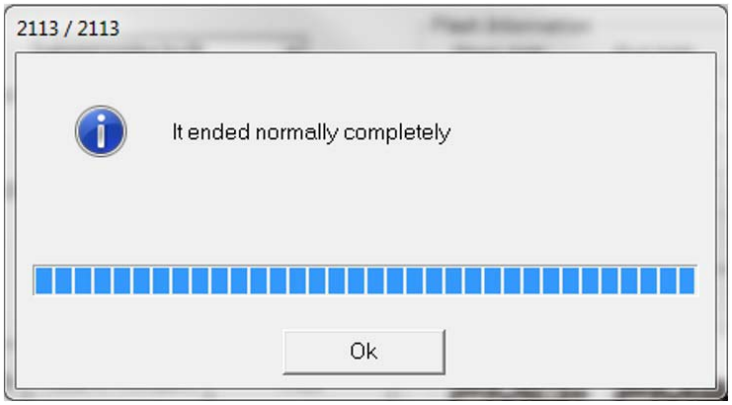
When the operation starts, a window pops up with the message shown in Figure 4-6.

Figure 4-6. Wait for Reset (SW1) Button Press to Continue Programming



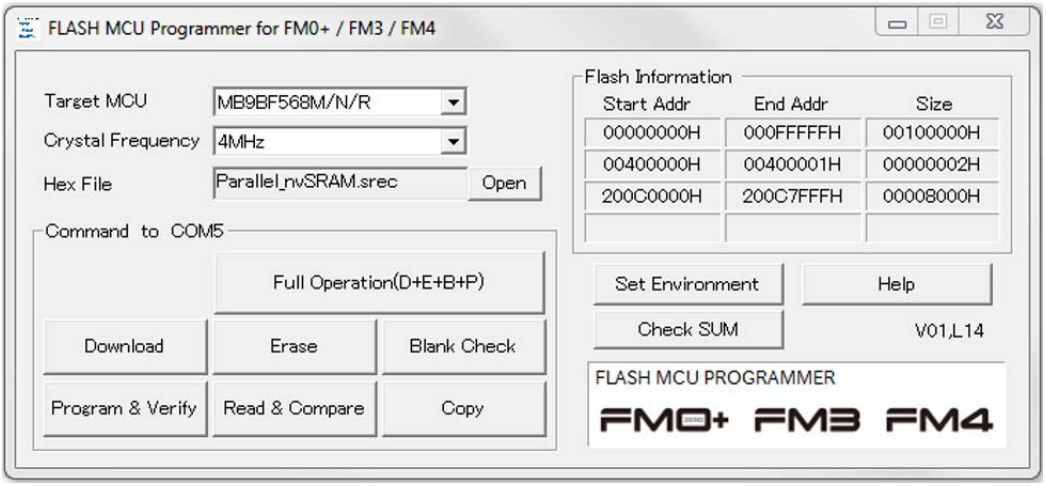
10. Press switch SW1 as shown in Figure 4-2 to reset the controller, then press **OK** (LED3 will blink). The programming cycle will complete and the message shown in Figure 4-7 is displayed. Press **OK**.

Figure 4-7. End of MCU Flash Programming



11. After the programming is complete, the other buttons, which were grayed out initially, are enabled. However, these operations are not required to use the nvSRAM DVK.

Figure 4-8. Flash MCU Programmer Enables Buttons after Programming



4.2 Run the FM4 MCU Evaluation Board

After the FM4 MCU is successfully programmed, it must be configured in the Run mode to execute user commands. The nvSRAM kit software program, discussed in the Kit Software chapter on page 32, sends the user commands to the MCU via the CN4 USB interface. The FM4 MCU firmware decodes the user commands and executes operation on the nvSRAM. The FM4 MCU Evaluation Board requires the following setup to run the programmed firmware as shown in Figure 4-9:

1. Set the Run jumper position to configure in the Run Mode.
2. Retain USBF, USBF, and NMI jumper setting.
3. Retain the 3V jumper position as is for 3.3 V operation.
4. Set the USB jumper.
5. Set the SOT0, SIN0, and LED jumpers.
6. All other jumpers, not marked, should remain unconnected in the DVK Run mode.
7. Connect the MCU board to a PC via the CN4 port.

   Refer to A.6.5 Jumper Setting Table - FM4 MCU Evaluation Board Run Mode on page 64 for more details.

Figure 4-9. FM4 MCU Evaluation Board Jumper Setting in Run Mode

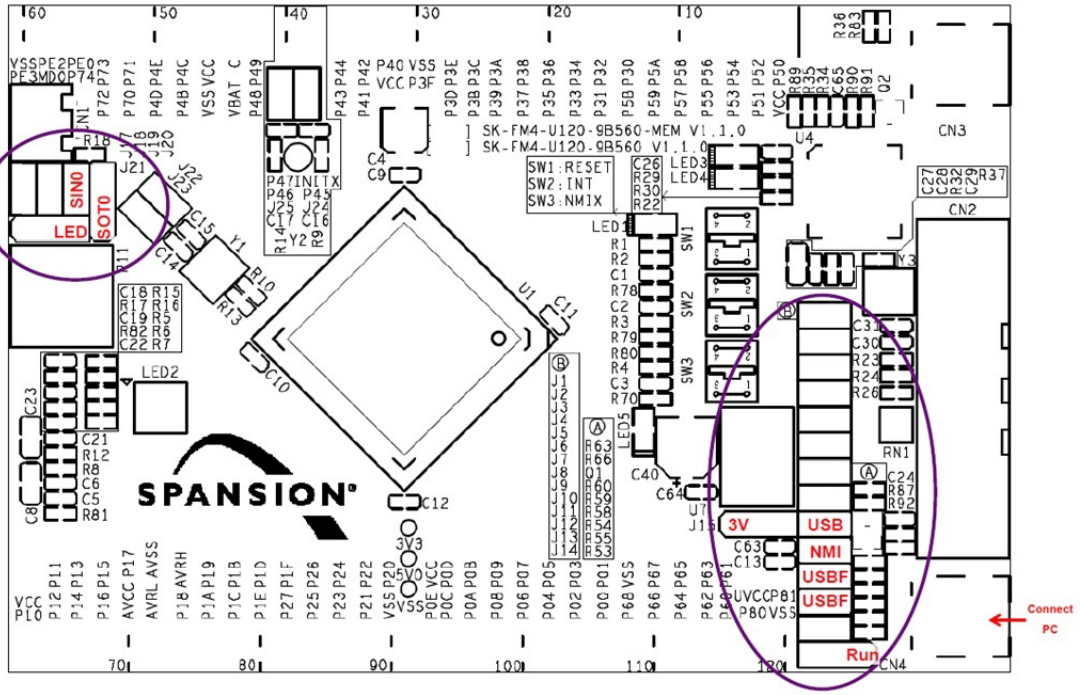
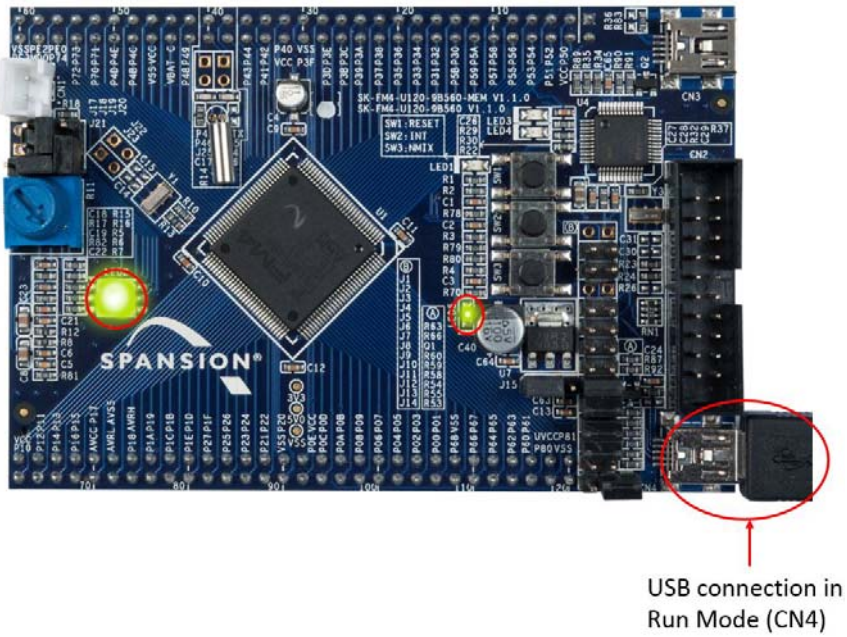


Figure 4-10. FM4 MCU Evaluation Board Setup in Run Mode

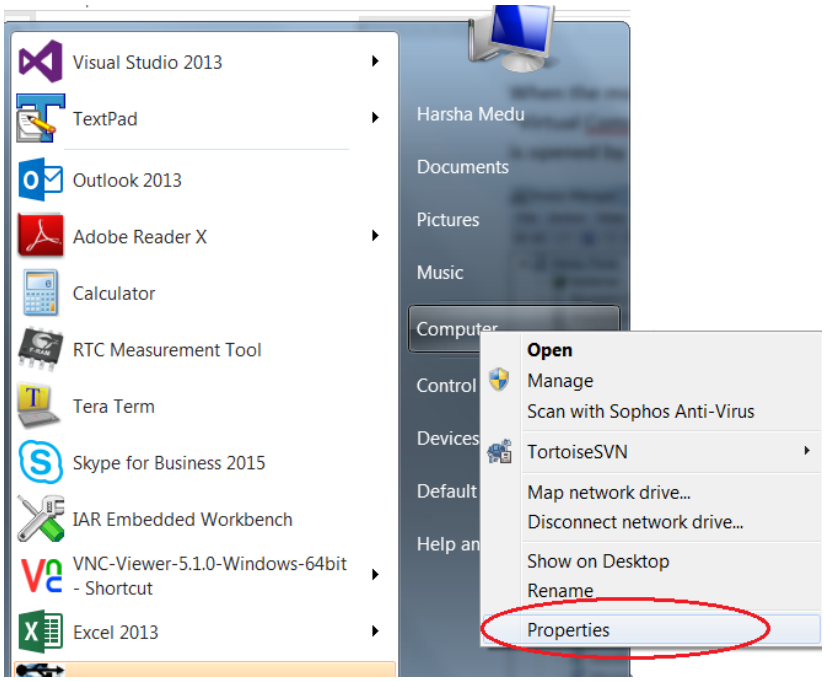


LED2 and LED5 turn green to indicate the board is powered from the USB port via the CN4 connector. LED3 is off indicating the board is powered in the Run mode. After connecting the FM4 MCU Evaluation Board to your PC through the USB port (CN4), wait for drivers to install. When drivers are successfully installed, follow the steps in 4.3 Spansion Virtual Communication Port Driver Installation to verify or install the Spansion Virtual Communications Port driver. Connecting the FM4 MCU Evaluation Board USB port ‘CN4’ to the PC should recognize the port as a ‘Spansion Virtual Communications Port’.

4.3 Spansion Virtual Communication Port Driver Installation

1. After connecting the FM4 MCU Base Board to your PC through the USB port (CN4), wait for drivers to install. When installed, follow steps 1 through 3 to verify if the driver is successfully installed. If the Spansion Virtual Communication Port driver is not installed, follow steps 1 through 8 to install the driver. Choose **Start** > **Computer** and right-click **Properties**, as shown in Figure 4-11.

Figure 4-11. Open Computer Properties

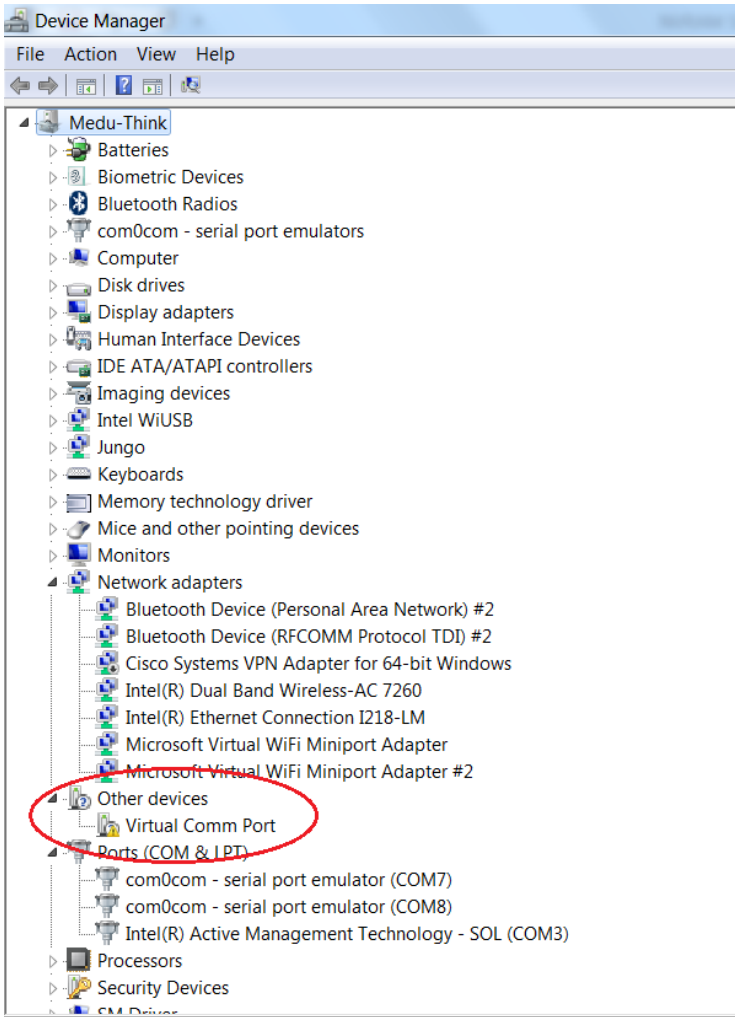


2. Click **Device Manager** as shown in Figure 4-12.

Figure 4-12. Open Device Manager

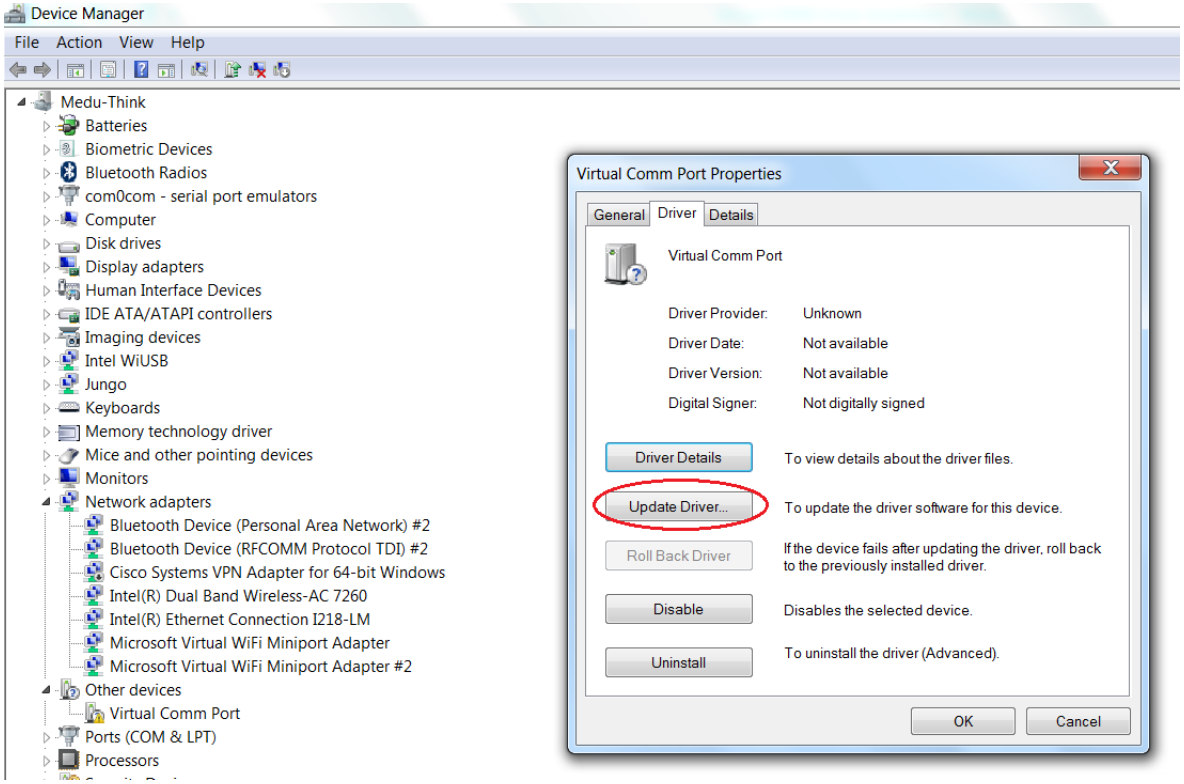
3. If the driver is installed, the board appears as **Spansion Virtual Communications Port** under **Ports (COM & LPT)** in the Device Manager as shown in Figure 4-18.
4. If the driver is not installed, the board appears as **Virtual Comm Port** under **Other devices** in the Device Manager as shown in Figure 4-13.

Figure 4-13. Other Devices - Virtual Comm Port



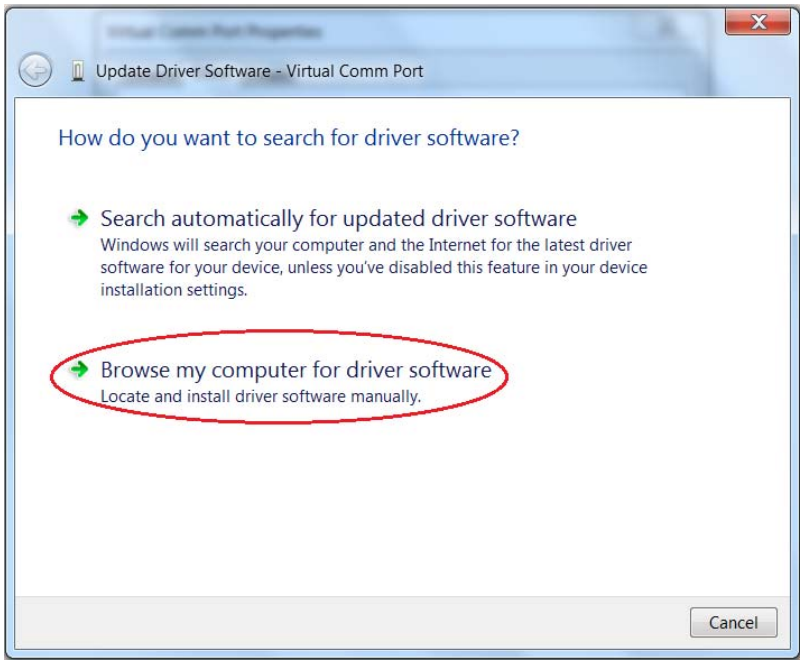
5. Right-click **Virtual Comm Port** and select **Properties** as shown in Figure 4-14. The Virtual Comm Port Properties window opens up; select **Update Driver** from the Driver tab.

Figure 4-14. Update Virtual Comm Port Driver



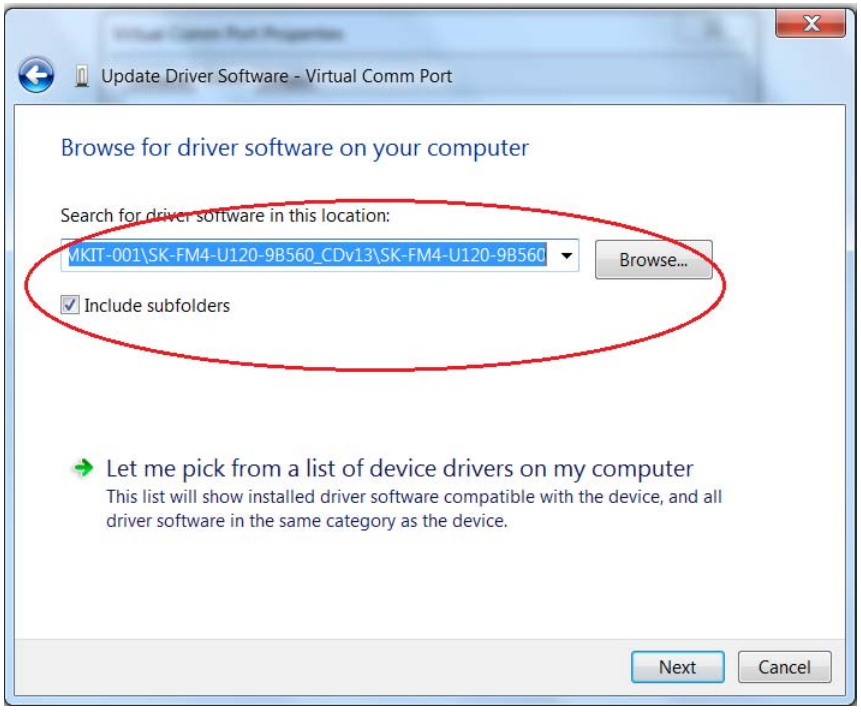
6. In the Update Driver window, select **Browse my computer for driver software** as shown in Figure 4-15.

Figure 4-15. Browse Virtual Comm Port Driver Software



7. Browse the downloaded **SK-FM4-U120-9B560** kit folder and select the **Include subfolders** check box. Click **Next**.

Figure 4-16. Virtual Comm Port Driver Software Link

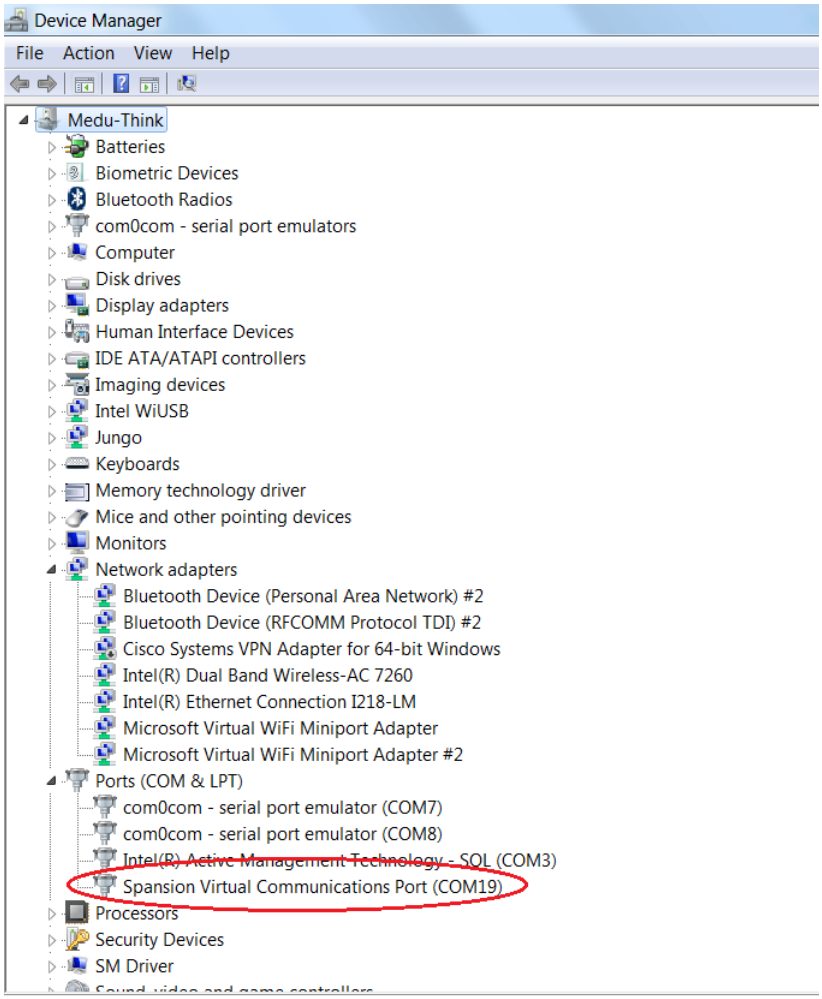


8. A Windows Security popup appears as below; select **Install this driver software anyway** (see Figure 4-17).

Figure 4-17. Install Virtual Comm Port Driver Software

9. When the driver is installed successfully, the board will appear as **Spansion Virtual Communications Port** under **Ports (COM & LPT)** in the Device Manager as shown in Figure 4-18. Now the board is ready for use with the CY14NVSRAMKIT-001 DVK software.

Figure 4-18. Verify Spansion Virtual Communication Port



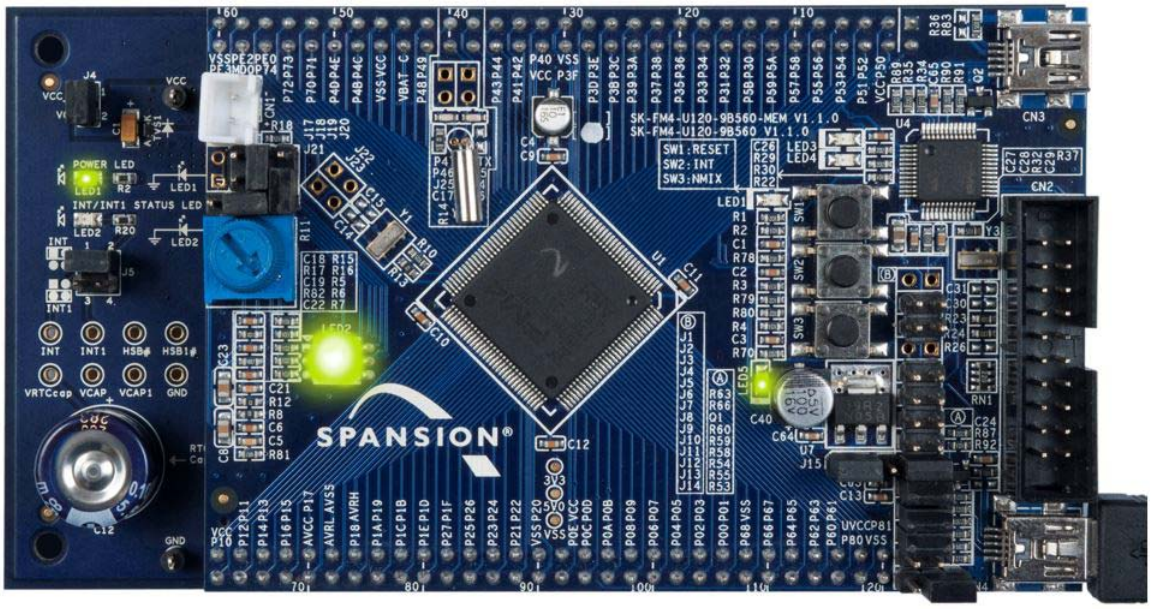
4.4 Development Kit Setup

After configuring the FM4 MCU Evaluation Board in Run mode, connect the nvSRAM DVK with the FM4 MCU Evaluation Board, as shown in Figure 4-19 to run the software.

CAUTION: Remove the USB connection to power off the FM4 MCU Evaluation Board before plugging on the CY14NVSRAMKIT-001 board.

Software details are provided in the Kit Software chapter on page 32.

Figure 4-19. Development Kit Setup in Run Mode



The following is the status of different LEDs when the setup is configured in Run mode and the FM4 MCU Evaluation Board is connected to the PC via USB connector CN4:

- LED5 on the FM4 MCU Evaluation Board glows green indicating the MCU is configured in Run mode.
- LED2 on the FM4 MCU Evaluation Board glows green indicating the MCU is successfully programmed with firmware.
- POWER LED (LED1) on the nvSRAM DVK glows green.
- INT/INT1 STATUS LED (LED2) on the nvSRAM DVK will blink at 1 Hz when the MCU is successfully programmed with the example firmware.

Note: The CY14NVSRAMKIT-001 DVK factory setting is 1 Hz square-wave output at the INT pin. This will blink the INT/INT1 STATUS LED (LED2) every second when the jumper J5 pin 1 and 2 is shorted with 3.3 V VCC power applied to the kit.

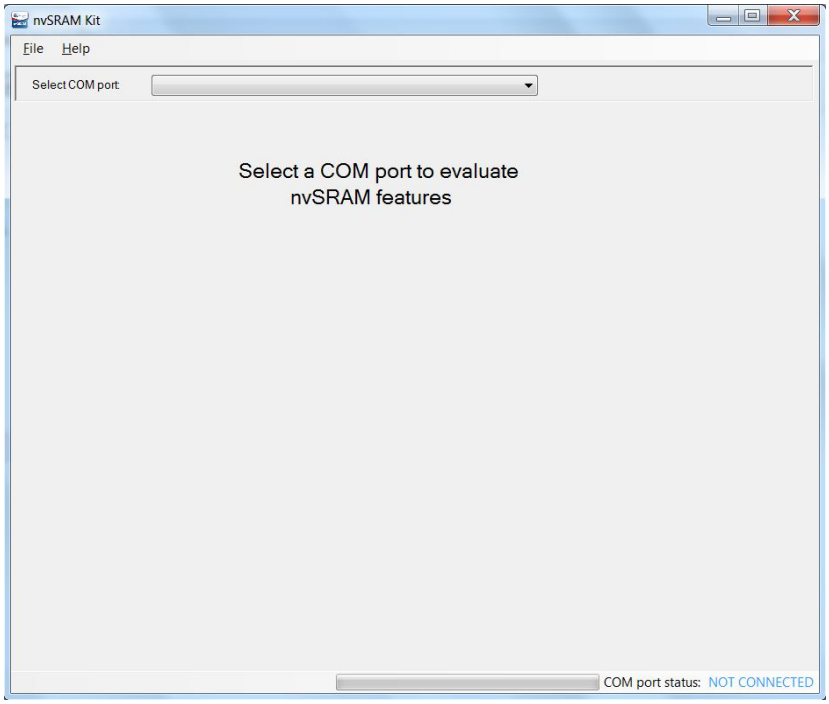
5. Kit Software

This section describes the nvSRAM kit software. Follow the instructions in sections 4.1 Program the FM4 MCU Evaluation Board on page 20, 4.2 Run the FM4 MCU Evaluation Board on page 24, and 4.4 Development Kit Setup on page 30 to set up the kit before using the nvSRAM kit software.

5.1 nvSRAM Kit Software

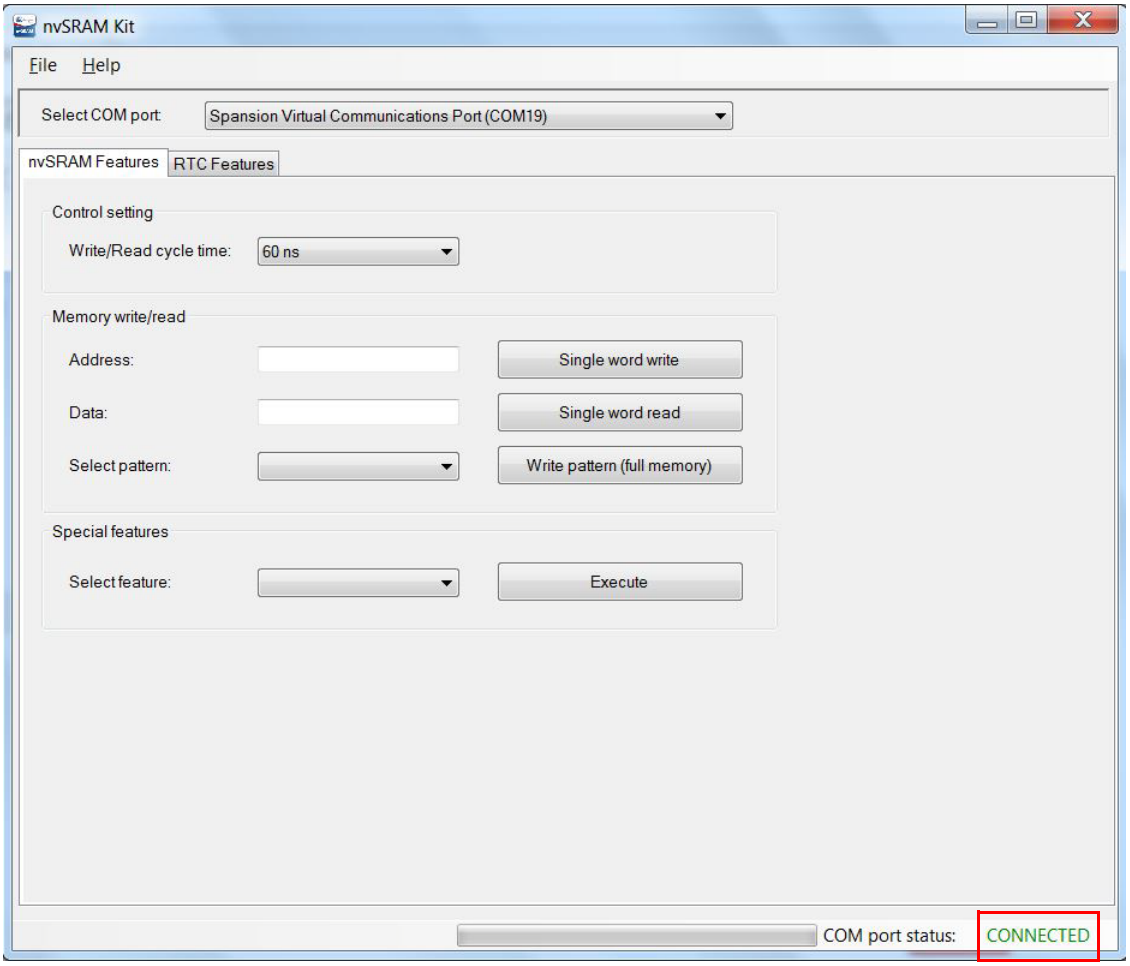
Open the nvSRAM kit software from **Start** > **All Programs** > **Cypress** > **nvSRAM Kit**.

Figure 5-1. nvSRAM Kit Software Startup Window



The kit will appear as "Spansion Virtual Communications Port". Select this COM port from the drop-down list. When the COM port is selected, the COM port status will change to CONENCTED as indicated in Figure 5-2.

Figure 5-2. nvSRAM Features



When the correct COM port is selected, you can evaluate the following features in the nvSRAM Features tab.

Table 5-1. nvSRAM Features

nvSRAM Feature	Description
Write/Read cycle time	This sets the cycle time for read/write operations. Options are 60 ns, 100 ns, 130 ns, 150 ns, and 190 ns.
Address	This box is writable with the nvSRAM address. It takes a maximum of five hexadecimal characters representing a 20-bit address, A0 to A19. Range is: 00000 to FFFEF to access the nvSRAM data memory. FFFF0 to FFFFF to access the 16 RTC registers.
Data	This box is writable and readable for nvSRAM data. It takes a maximum of four hexadecimal characters representing 16-bit data, DQ0 to DQ15. Range is 0000 to FFFF
Select pattern	Selects a pattern to write the entire memory, 00000 to FFFEF. Options are Data, Data/Data_b, Address, and Address/Address_b. Data: Write the entire memory with data specified in the ‘Data’ box. Data/Data_b: Write the entire memory with data and complement of data on alternate address locations. Address: Write the entire memory with the last 16 bits of the address. Address/Address_b: Write the entire memory with the last 16 bits of the address and its complement alternatively.
Single word write	Clicking this button will write the value in the 'Data' box to the specified address location in the 'Address' box.
Single word read	Clicking this button will read the value from the address location specified in the 'Address' box and display it in the 'Data' box.
Write pattern (full memory)	Clicking this button will write the selected pattern to the entire memory, 00000 to FFFEF.
Select feature	Select one of the following nvSRAM features: - Software Store: Initiates the Software Store in nvSRAM. - Software Recall: Initiates the Software Recall in nvSRAM. - Autostore Enable: Enables the AutoStore feature in nvSRAM. - Autostore Disable: Disables the AutoStore feature in nvSRAM. - HSB Store: Toggles HSB LOW to initiate the hardware store in nvSRAM. - Sleep: Drives nvSRAM ZZ# low and puts it in the SLEEP mode. - Wakeup: Drives nvSRAM ZZ# high and wakes it up from the SLEEP mode.
Execute	Clicking this button will execute the selected nvSRAM feature.

Selecting the RTC Features tab will display the following window, which allows you to evaluate RTC features.

Figure 5-3. RTC Features

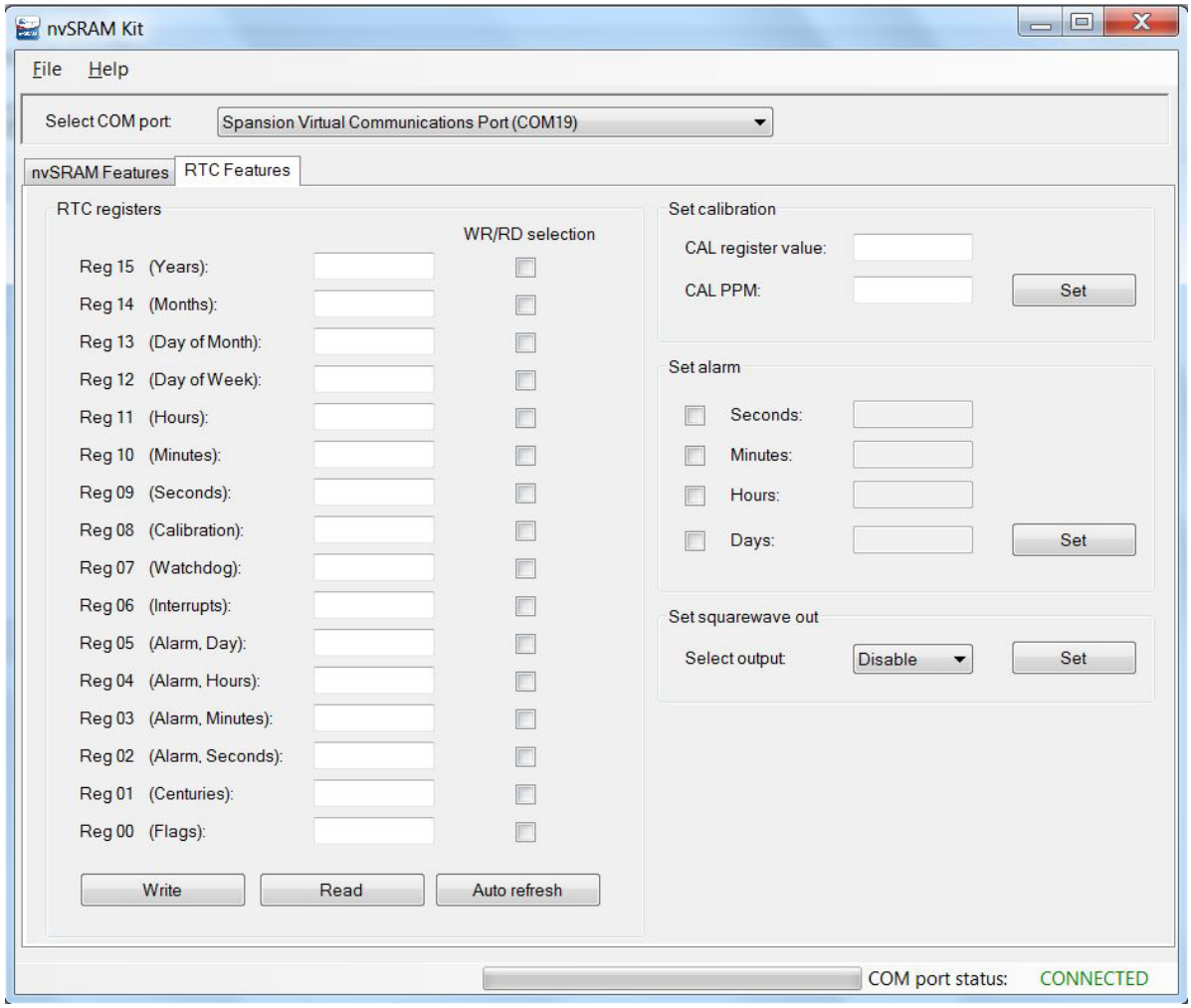


Table 5-2. RTC Features

RTC Feature	Description
RTC registers	This box lists the 16 RTC registers.
WR/RD selection	This checkbox against each RTC register indicates whether that particular register is selected for RTC write/read operation. Checking the box for a register indicates that the RTC register is part of RTC write/read operation.
Write	Clicking this button will write to the selected RTC registers. A write operation will set the 'W' bit automatically for RTC writing except for the Flags register. **Note:** After every write, the nvSRAM RTC registers are read back and the GUI is updated with data from the device.
Read	Clicking this button will read from the selected RTC registers. A read operation will set the 'R' bit automatically for the RTC reading except the Flags register.

Table 5-2. RTC Features

RTC Feature	Description
Auto refresh	Clicking this button will read the RTC registers every 500 ms until the Stop button is clicked. 'Auto refresh' will change to the Stop button while running. No other operation can be performed during this time.
Set calibration	This box sets the RTC calibration. You can enter calibration values either in binary form or in terms of PPM. Refer to the application note AN53313 - Real Time Clock Calibration in Cypress nvSRAM for more details. **Note:** After setting calibration, the nvSRAM RTC registers are read back and the GUI is updated with data from the device.
Set alarm	This box sets the RTC alarm. By default, the RTC alarm is disabled. You can enable the alarm by checking the box for the required alarm registers, setting appropriate values, and then clicking the **Set** button. **Note:** After setting alarm, the nvSRAM RTC registers are read back and the GUI is updated with data from the device.
Set squarewave out	This box sets the square wave on INT/INT1 pin. The options are: Disable 1 Hz 512 Hz 4096 Hz 32768 Hz **Note:** After setting squarewave, the nvSRAM RTC registers are read back and the GUI is updated with data from the device.

The File menu functions are shown in Figure 5-4.

Figure 5-4. Load/Dump Features

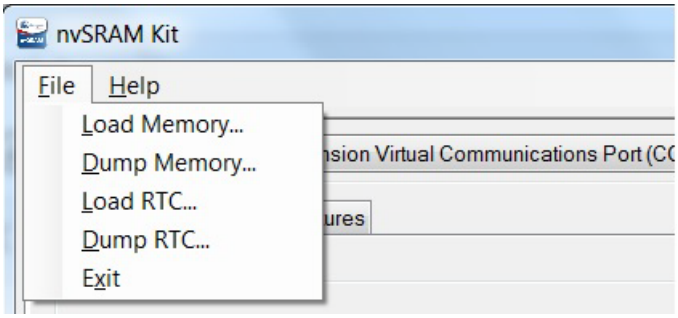


Figure 5-5. Load Memory

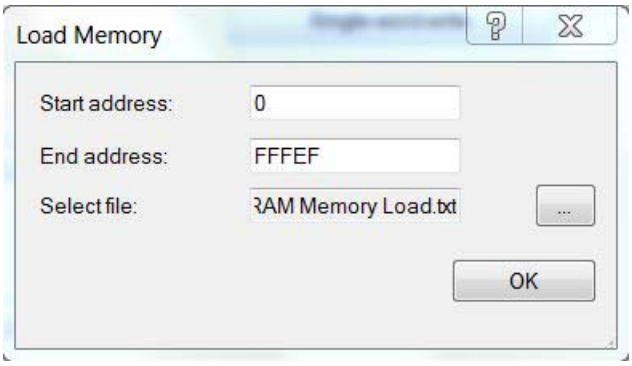


Figure 5-6. Dump Memory

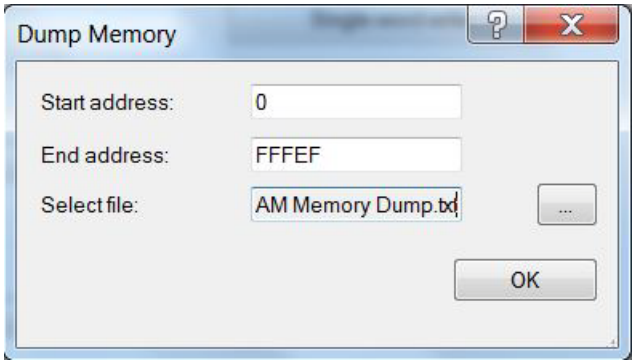


Figure 5-7. Load RTC Selection

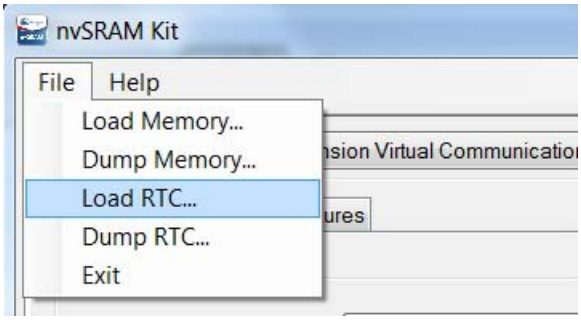


Figure 5-8. Load RTC

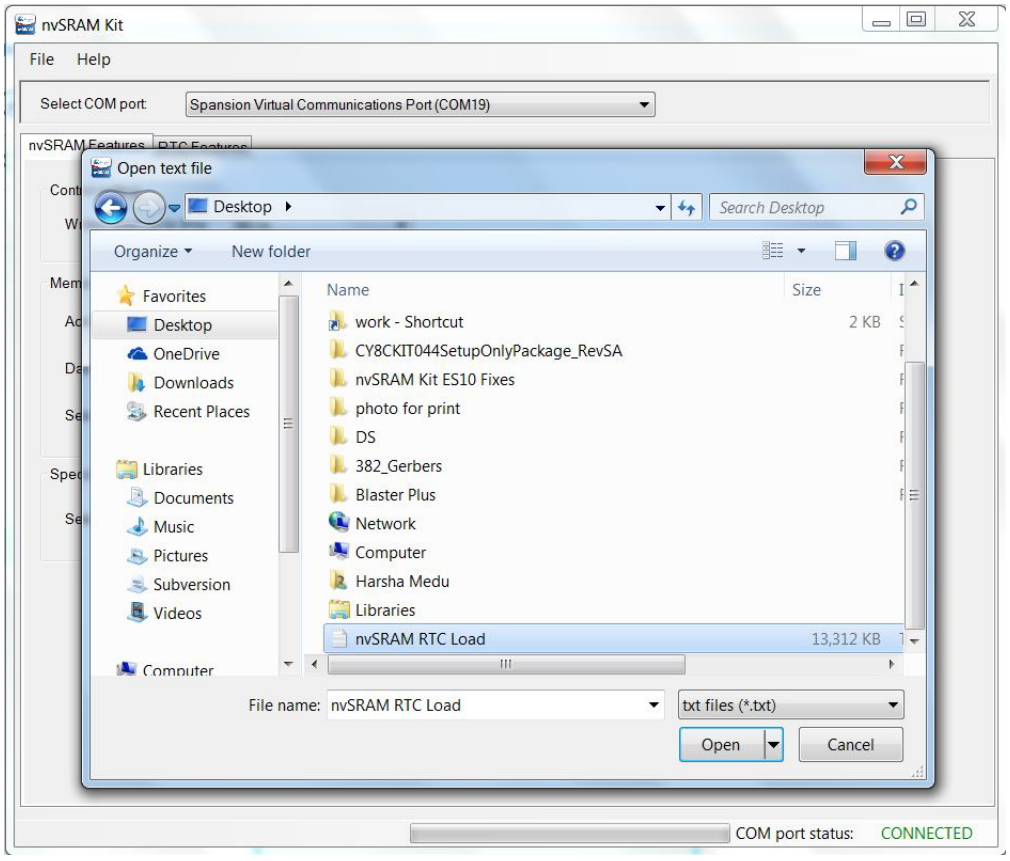


Figure 5-9. Dump RTC Selection

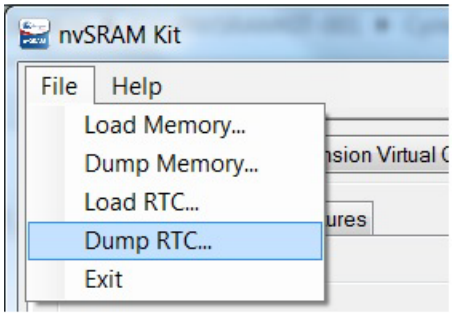


Figure 5-10. Dump RTC

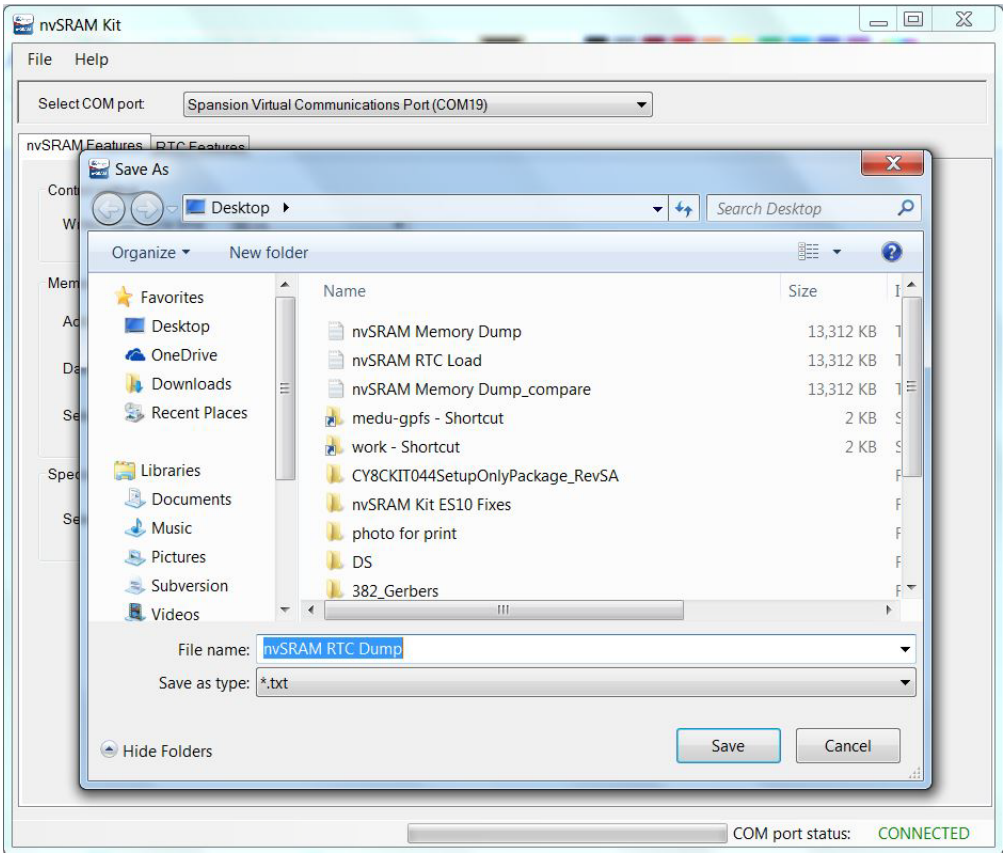


Table 5-3. File Menu Options

File Menu	Description
Load Memory…	This menu selection opens the 'Load Memory' dialog box, which specifies the starting address, ending address, and the file from which to load data to nvSRAM memory.
Dump Memory…	This menu selection opens the 'Dump Memory' dialog box, which specifies the starting address, ending address, and the file to which the data from nvSRAM memory should be saved.
Load RTC…	This menu selection will load the 16 bytes of data from a file into the nvSRAM RTC registers.
Dump RTC…	This menu selection will dump the 16 bytes of data from the nvSRAM RTC registers to a file.
Exit	This menu selection will exit the application.

The Help menu functions are shown in Figure 5-11.

Figure 5-11. Help Menu

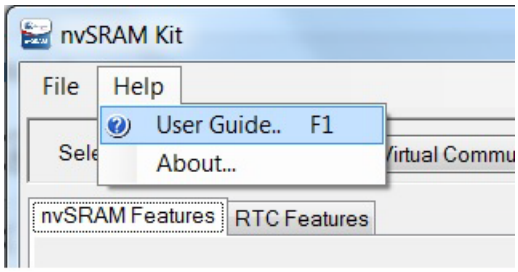


Table 5-4. Help Menu

Help Menu	Description
User Guide…	This menu selection (or pressing **[F1]**) will open the kit user guide.
About…	This menu selection provides information about the nvSRAM Kit Software

6. Kit Example Firmware

This chapter discusses the kit example firmware structure and function description for the nvSRAM access. The kit example firmware code is custom built for the nvSRAM access using the FM4 MCU Evaluation Board. You can leverage these example codes and functions to develop the nvSRAM access for the target controller platform.

6.1 Example Firmware Structure

The example firmware API is broken into three files:

- *GUIif.c* - This file contains the high-level function call used by the GUI.
- *CY14B116.c* - This file contains the low-level function calls used to communicate with the nvSRAM device.
- *EBItest.c* - This file contains FM4 MCU-specific functions for the hardware test.

These three files are stored in the nvSRAM folder of the example project. The example firmware project file path is shown in the following table.

Table 6-1. Example Project File Path

Project Files	File Path
Main project	`<Install_Directory>\CY14NVSRAMKIT-001 nvSRAM Development Kit\1.0\Firmware\Source\main_project\IAR`
nvSRAM project files	`<Install_Directory>\CY14NVSRAMKIT-001 nvSRAM Development Kit\1.0\Firmware\Source\cypress\nvp\nvSRAM\`
FM4 library	`<Install_Directory>\CY14NVSRAMKIT-001 nvSRAM Development Kit\1.0\Firmware\Source\library`
Bin file	`<Install_Directory>\CY14NVSRAMKIT-001 nvSRAM Development Kit\1.0\Firmware\Source\main_project\IAR\nvSRAM_Kit\Exe`

6.2 nvSRAM Access APIs

This section lists the nvSRAM access application programming interface (API) functions that are used in the FM4 MCU example firmware. nvSRAM APIs are defined in *CY14B116.c*. See 6.1 Example Firmware Structure for file description and access path.

Table 6-2. nvSRAM Access APIs (*CY14B116.h* and *CY14B116.c*)

Functions	Description	Modes
nvSRAMRead (uint32_t address, uint8_t length, uint8_t *txData)	Read from the nvSRAM, 1 to 255 bytes	None
nvSRAMWrite (uint32_t address, uint16_t data)	Write to the nvSRAM, one address location	
nvSRAMWriteFullMem (uint16_t data1, uint16_t data2)	Write the entire memory array (00000 to FFFEF) with 16-bit dataword1 (data1) and dataword2 (data2) at consecutive address locations	
nvSRAMReadRTC (uint8_t address, uint8_t length, uint8_t *txData)	Read RTC registers	
nvSRAMWriteRTC (uint8_t address, uint8_t data)	Write to RTC registers	
HSBStoreIF (void)	Triggers hardware store by toggling the HSB# pin low	
write_data_pattern (uint8_t pat, uint16_t data)	Writes a test pattern to the full nvSRAM array. "pat" sets the data pattern to be written. The pattern can be one of the four patterns: Data, Data_bar, Address, Address_bar. Data and Address are values set by the user to execute this function	DATA_PAT, DATAB_PAT, ADDR_PAT, ADDRB_PAT
AutoStore (boolean_t enable)	Enable/Disable Auto Store in nvSRAM	AUTOSTORE_ENABLE, AUTOSTORE_DISABLE
SoftwareStoreRecall (boolean_t mode)	Trigger a Software Store/Recall function in nvSRAM	SOFTSTORE, SOFTRECALL
SleepIF (boolean_t mode)	Enters nvSRAM sleep mode by toggling the ZZ# pin low	SLEEP_ENTRY, SLEEP_EXIT
SquareWave (uint8_t mode)	Set the squarewave output on the INT pin. By setting the correct mode, the square wave output can either be disabled or enabled with one of four output frequencies: 1 Hz, 512 Hz, 4096 Hz, or 32768 Hz	DISABLE_SQ_WAVE, ENABLE_1HZ, ENABLE_512HZ, ENABLE_4096HZ, ENABLE_32768HZ

The following sections provide details on the nvSRAM APIs.

6.2.1 nvSRAMRead (uint32_t address, uint8_t length, uint8_t *txData)

```
/*******************************************************************************
 ** \param address - memory address
 ** \param length - number of bytes to read
 ** \param txData - read data buffer
 **
```

```
 ***************************************************************************/
void nvSRAMRead (uint32_t address, uint8_t length, uint8_t *txData)
{
  uint16_t tempData;
  uint8_t  u8Counter;
  for (u8Counter = 0u; u8Counter < length; u8Counter = u8Counter+1)
  {
    tempData = *((uint16_t*)(nvSRAM_BASE_ADDRESS + ((address + u8Counter) * 2)));
    // MCU reads 16-bit data
    txData[(u8Counter*2)] = (uint8_t)(tempData>>8);
    //Stores lower byte of 16-bit read data
    txData[(u8Counter*2)+1] = (uint8_t)(tempData);
    //Stores upper byte of 16-bit read data
  }
}
```

6.2.2 void nvSRAMWrite (uint32_t address, uint16_t data)

```
/***************************************************************************
 ** \param address - memory address
 ** \param data - data word to write
 **
 ***************************************************************************/
void nvSRAMWrite (uint32_t address, uint16_t data)
{
  *(uint16_t*)(nvSRAM_BASE_ADDRESS + (address * 2)) = data;
  // MCU writes 16-bit data to nvSRAM
}
```

6.2.3 void nvSRAMWriteFullMem (uint16_t data1, uint16_t data2)

```
/***************************************************************************
 ** \param data1 - data word (data1) to write
 ** \param data2 - data word (data2) to write
 **
 ***************************************************************************/
void nvSRAMWriteFullMem (uint16_t data1, uint16_t data2)
{
  uint32_t u32Counter;
  for (u32Counter = 0u; u32Counter < nvSRAM_MEM_SIZE; u32Counter=u32Counter+2)
  {
    *(uint16_t*)(nvSRAM_BASE_ADDRESS + (u32Counter * 2)) = data1;
    *(uint16_t*)(nvSRAM_BASE_ADDRESS + ((u32Counter + 1) * 2)) = data2;
  }
}
```

6.2.4 void nvSRAMReadRTC (uint8_t address, uint8_t length, uint8_t *txData)

```
/***************************************************************************
 ** \param address - RTC address
 ** \param length - number of bytes to read
 ** \param txData - read data buffer
 **
 ***************************************************************************/
void nvSRAMReadRTC (uint8_t address, uint8_t length, uint8_t *txData)
{
  uint16_t tempData;
  uint8_t  u8Counter;
```

```
  for (u8Counter = 0u; u8Counter < length; u8Counter = u8Counter+1)
  {
  // 0x0FFFF0 is the RTC OFFSET address for x16 part
    tempData = *((uint16_t*)(nvSRAM_BASE_ADDRESS + ((nvSRAM_RTC_OFFSET + address +
u8Counter) * 2)));

    txData[u8Counter] = (uint8_t)(tempData);
  }
}
```

6.2.5 void nvSRAMWriteRTC (uint8_t address, uint8_t data)

```
/*****************************************************************************
 ** \param address - RTC address
 ** \param data - write data byte
 **
 *****************************************************************************/
void nvSRAMWriteRTC (uint8_t address, uint8_t data)
{

    *((uint16_t*)(nvSRAM_BASE_ADDRESS + ((nvSRAM_RTC_OFFSET + address) * 2))) =
data;
}
```

6.2.6 void HSBStoreIF(void)

```
/*****************************************************************************
 ** \param none
 **
 *****************************************************************************/
void HSBStoreIF(void)
{
  uint32_t temp = 0;
  BOARD_HSB = 0u;
  // HM: Set a standard value = 5us or 10 us
  while (temp < 500)
  {
    temp++;
  }
  BOARD_HSB = 1u;
}
```

6.2.7 void write_data_pattern (uint8_t pat, uint16_t data)

```
/*****************************************************************************
 ** \param pat - user data pattern type (0x01, 0x02, 0x03, 0x04)
 ** \param data - write data word
 **
 *****************************************************************************/

void write_data_pattern (uint8_t pat, uint16_t data)
{
     switch(pat)
     {
        case DATA_PAT: \\ pat = 0x00
          nvSRAMWriteFullMem(data, data);
          break;
```

```
        case DATAB_PAT: \\ pat = 0x01
          nvSRAMWriteFullMem(data, (data ^ 0xFFFF));
          break;
        case ADDR_PAT: \\ pat = 0x02
          nvSRAMWriteFullMemAddr();
          break;
        case ADDRB_PAT: \\ pat = 0x03
          nvSRAMWriteFullMemAddrb();
          break;
        default:
          break;
    }
}
```

6.2.8 void AutoStore (boolean_t enable)

```
/
*****************************************************************************
***********
 ** \param enable - true, enables AutoStore; false, disables AutoStore in nvSRAM
 **

*****************************************************************************
**********/

void AutoStore (boolean_t enable)
{
  uint8_t temp[2];

  if (enable)
  {
      nvSRAMRead (FUNCTION_MODE_0, 0x1, temp); \\ FUNCTION_MODE_0 is read address
0x4E38
      nvSRAMRead (FUNCTION_MODE_1, 0x1, temp); \\ FUNCTION_MODE_1 is read address
0XB1C7
      nvSRAMRead (FUNCTION_MODE_2, 0x1, temp); \\ FUNCTION_MODE_2 is read address
0x83E0
      nvSRAMRead (FUNCTION_MODE_3, 0x1, temp); \\ FUNCTION_MODE_3 is read address
0x7C1F
      nvSRAMRead (FUNCTION_MODE_4, 0x1, temp); \\ FUNCTION_MODE_4 is read address
0x703F
      nvSRAMRead (M_AUTOSTORE_ENABLE, 0x1, temp); \\ M_AUTOSTORE_ENABLE is read
address 0x4B46
  }

else
{
      nvSRAMRead (FUNCTION_MODE_0, 0x1, temp); \\ FUNCTION_MODE_0 is read address
0x4E38
      nvSRAMRead (FUNCTION_MODE_1, 0x1, temp); \\ FUNCTION_MODE_1 is read address
0XB1C7
      nvSRAMRead (FUNCTION_MODE_2, 0x1, temp); \\ FUNCTION_MODE_2 is read address
0x83E0
      nvSRAMRead (FUNCTION_MODE_3, 0x1, temp); \\ FUNCTION_MODE_3 is read address
0x7C1F
      nvSRAMRead (FUNCTION_MODE_4, 0x1, temp); \\ FUNCTION_MODE_4 is read address
0x703F
```

```
      nvSRAMRead (M_AUTOSTORE_DISABLE, 0x1, temp); \\ M_AUTOSTORE_ DISABLE is read
address 0x8B45
  }
}
```

6.2.9 void SoftwareStoreRecall (boolean_t mode)

```
/*****************************************************************************
 ** \param mode - true, enables Software Store; false, disables Software Store in
nvSRAM
 **

*****************************************************************************/
void SoftwareStoreRecall (boolean_t mode)
{
  uint8_t temp[2];

  if (mode)
  {
     // TRUE = SOFT STORE
      nvSRAMRead (FUNCTION_MODE_0, 0x1, temp); \\ FUNCTION_MODE_0 is read address
0x4E38
      nvSRAMRead (FUNCTION_MODE_1, 0x1, temp); \\ FUNCTION_MODE_1 is read address
0XB1C7
      nvSRAMRead (FUNCTION_MODE_2, 0x1, temp); \\ FUNCTION_MODE_2 is read address
0x83E0
      nvSRAMRead (FUNCTION_MODE_3, 0x1, temp); \\ FUNCTION_MODE_3 is read address
0x7C1F
      nvSRAMRead (FUNCTION_MODE_4, 0x1, temp); \\ FUNCTION_MODE_4 is read address
0x703F
      nvSRAMRead (M_SOFTSTORE_ENABLE, 0x1, temp); \\ M_SOFTSTORE_ENABLE is read
address 0x8FC0
  }

  else
  {
      // FALSE = SOFT RECALL
      nvSRAMRead (FUNCTION_MODE_0, 0x1, temp); \\ FUNCTION_MODE_0 is read address
0x4E38
      nvSRAMRead (FUNCTION_MODE_1, 0x1, temp); \\ FUNCTION_MODE_1 is read address
0XB1C7
      nvSRAMRead (FUNCTION_MODE_2, 0x1, temp); \\ FUNCTION_MODE_2 is read address
0x83E0
      nvSRAMRead (FUNCTION_MODE_3, 0x1, temp); \\ FUNCTION_MODE_3 is read address
0x7C1F
      nvSRAMRead (FUNCTION_MODE_4, 0x1, temp); \\ FUNCTION_MODE_4 is read address
0x703F
     nvSRAMRead (M_SOFTRECALL_ENABLE, 0x1, temp); \\ M_ SOFTRECALL_ENABLE is read
address 0x4C63
  }
}
```

6.2.10 void SleepIF (boolean_t mode)

```
/*****************************************************************************
 ** \param mode - true, enables nvSRAM sleep; false, disables nvSRAM sleep
 **
```

```
*****************************************************************************/

void SleepIF (boolean_t mode)
{

  if (mode)
  {
    BOARD_ZZ = 0u;
  }

 else
{
    BOARD_ZZ = 1u;
  }
}
```

6.2.11 void SquareWave (uint8_t mode)

```
/*****************************************************************************
 ** \param mode - true, enables square-wave on the INT pin; false, disables square-
wave
 **
*****************************************************************************/
void SquareWave (uint8_t mode)
{
    uint8_t temp;
    uint8_t tempData;

    nvSRAMReadRTC (0x06, 0x1, &temp); \\ Reads the RTC register 0x06 setting

    if (mode != DISABLE_SQ_WAVE)
    {
        temp = temp & 0xEC;
        temp = temp | (mode - 1) | 0x10;
    }

    else
    {
          temp = temp & 0xEF;
    }

    nvSRAMReadRTC(0x00, 0x1, &tempData);
    tempData = tempData | 0x02; // Set W bit
    nvSRAMWriteRTC(0x00, tempData);
    nvSRAMWriteRTC(0x06, temp);
    tempData = tempData & 0xFD; // Reset W bit
    nvSRAMWriteRTC(0x00, tempData);
}
```

6.3 Firmware Changes to Enable 54 TSOP II Access

This section describes changes to be made in the firmware to enable access for the 16-Mbit, 1Mx16 nvSRAM (CY14B116M) in the 54 TSOP II package. This package option is default DNI on the CY14NVSRAMKIT-001 DVK hardware. The hardware must be populated with the CY14B116M, 54 TSOP II nvSRAM to access this feature.

Update the Base Address to support the selected EBI and then initiate the EBI. The 165 FBGA package is connected to the CS4 (chip select control 4) and the 54 TSOP II package is connected to the CS3 (chip select control 3) of the FM4 MCU.

The following sections describe the changes to be made in the respective files.

6.3.1 Changes in *CY14B116.h*

```
// CS3 TSOP
//#define nvSRAM_BASE_ADDRESS  (0x63000000ul)  // Uncomment to enable the
//base address for CS3 control
// CS4 FBGA
//#define nvSRAM_BASE_ADDRESS  (0x64000000ul)  // Uncomment to enable the
//base address for CS4 control
```

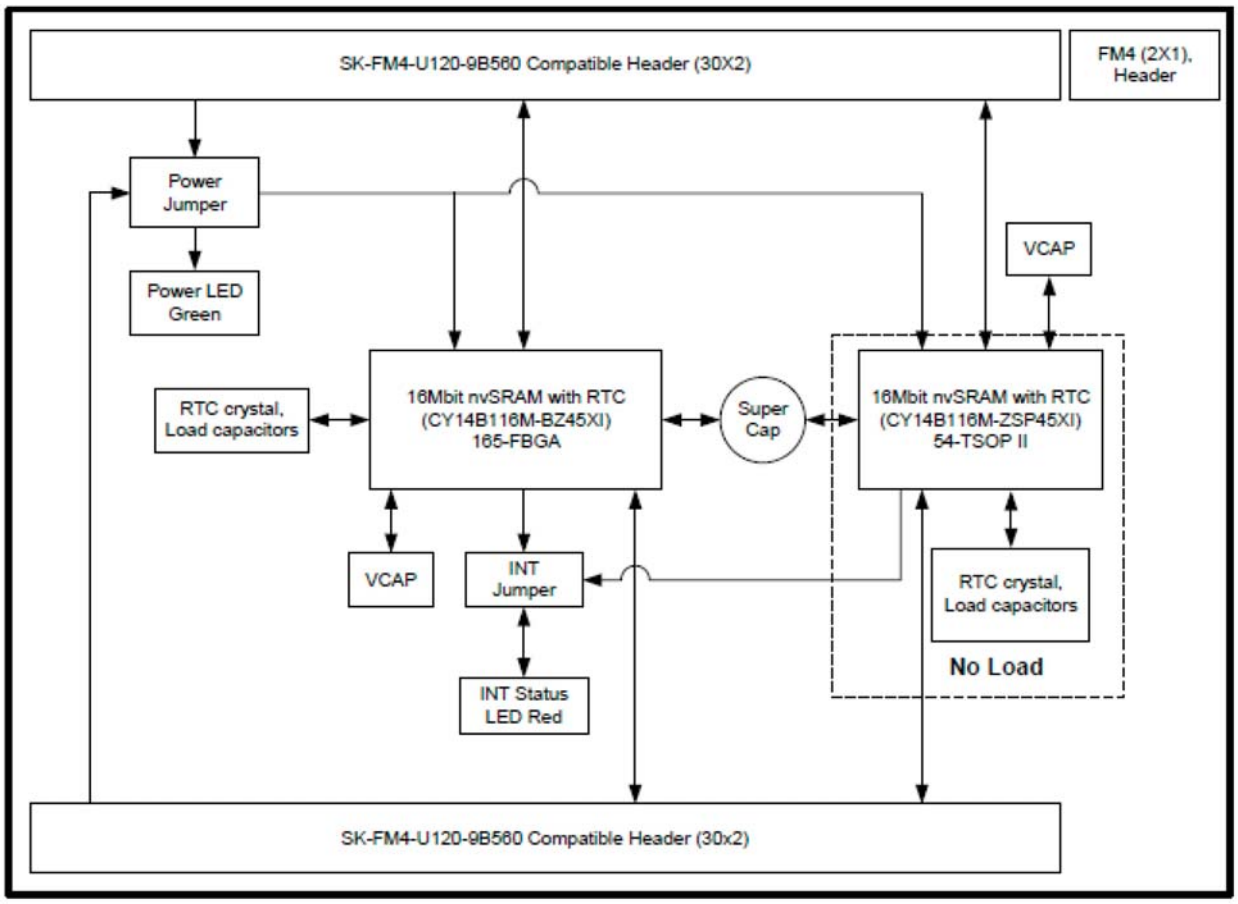
6.3.2 Changes in *CY14B116.c*

```
nvSRAM_Init(uint8_t cycles) function
// CS3 TSOP
// return (Extif_InitArea(3u, &stcExtIF)); // Uncomment to return for CS3
// CS4 FBGA
// return (Extif_InitArea(4u, &stcExtIF));  // Uncomment to return for CS4
```

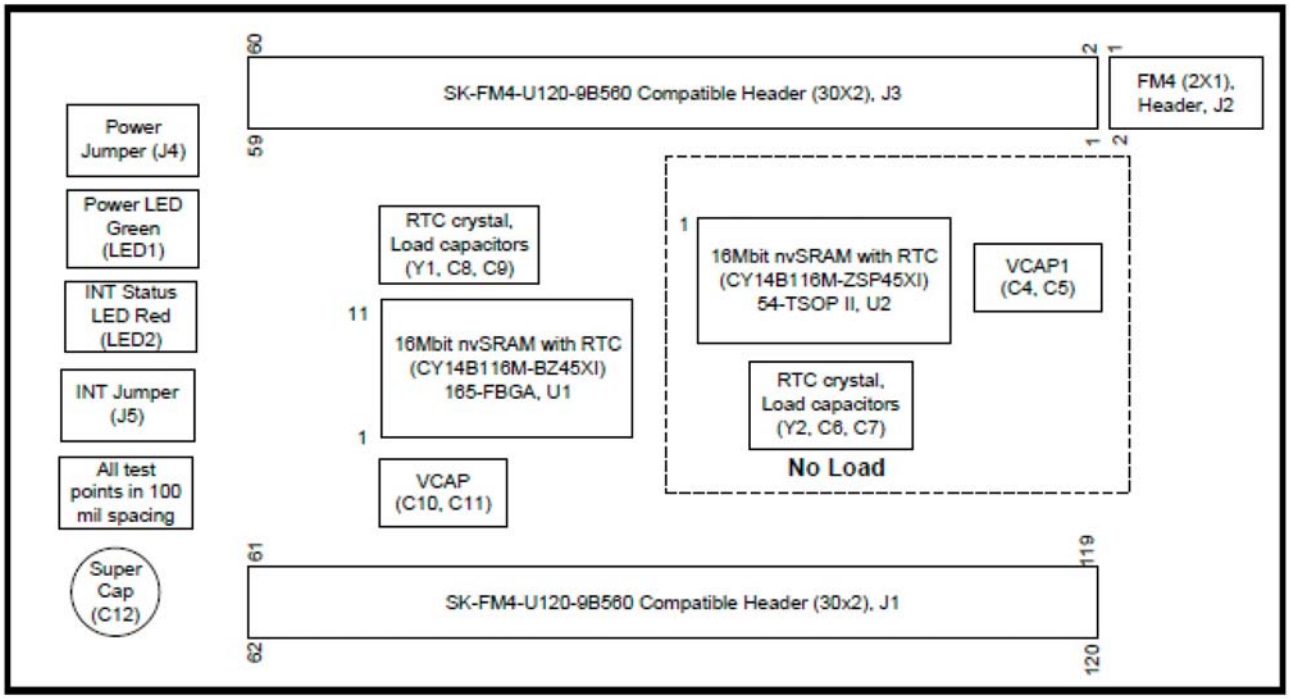
The sleep pin (ZZ#) is not available on the nvSRAM 54 TSOP II package. Hence, the Sleep and Wakeup features, described in Table 5-1 on page 34, is not applicable for the 54 TSOP II package.

A. Appendix

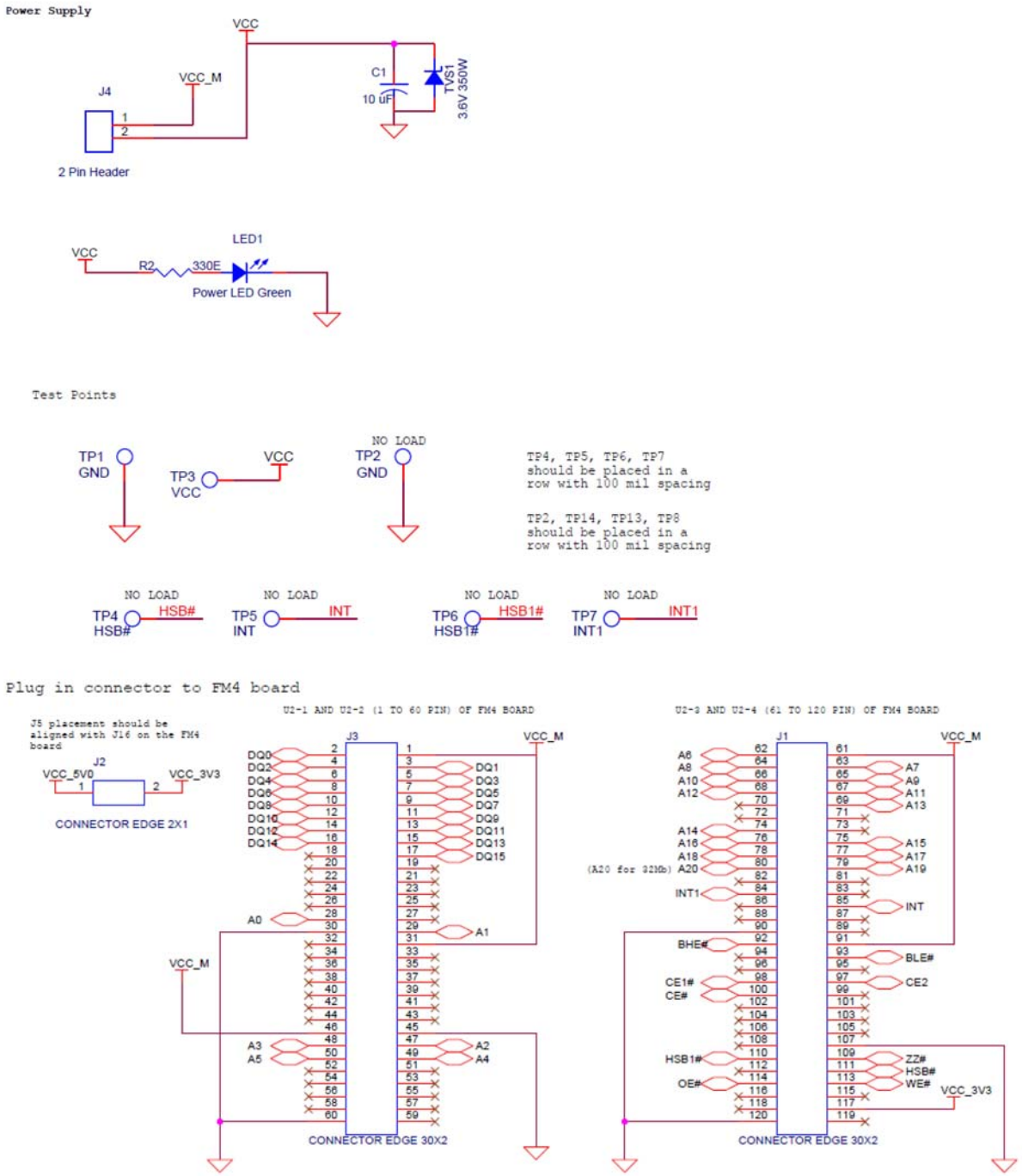
A.1 CY14NVSRAMKIT-001 Kit Block Diagram

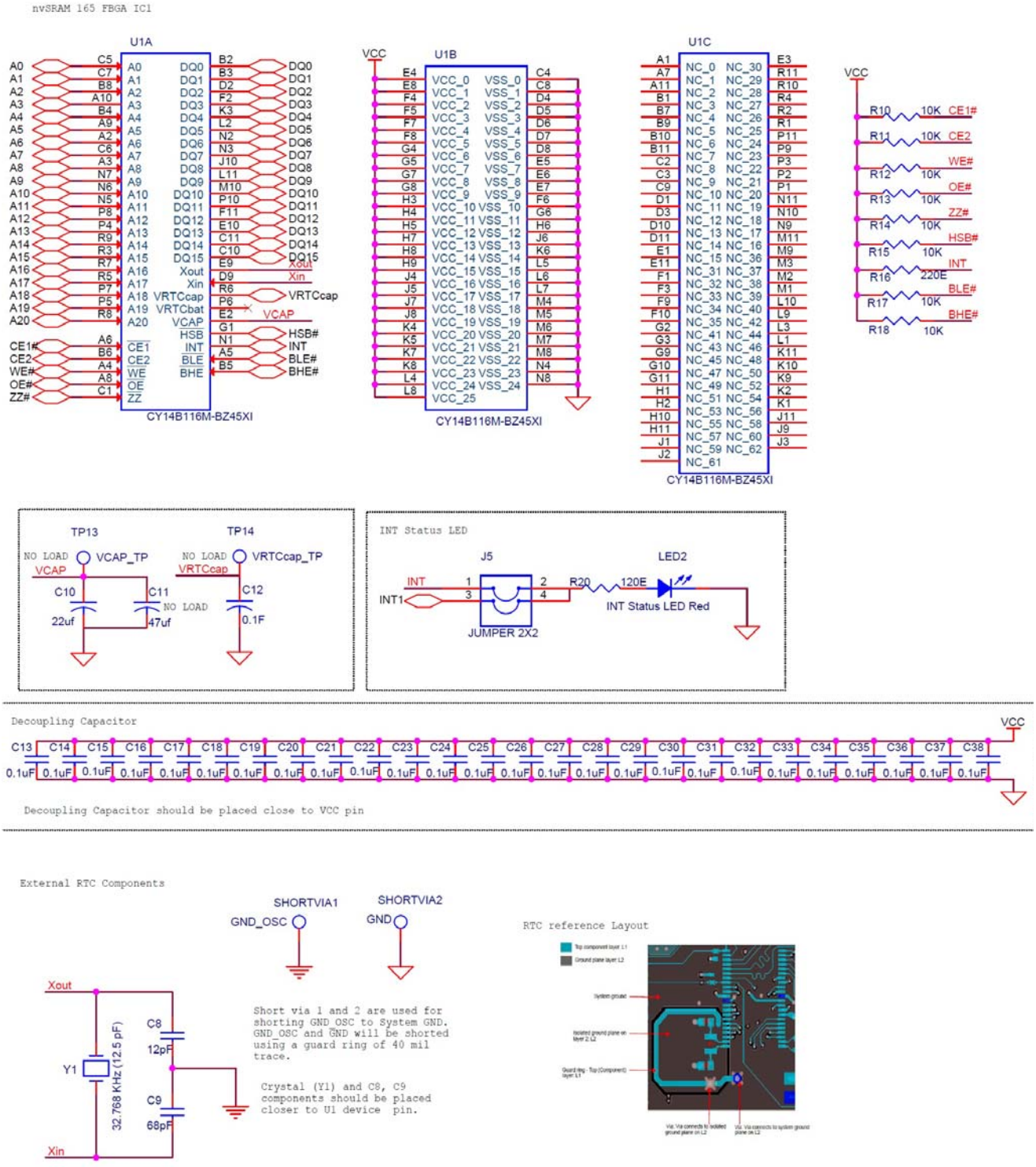


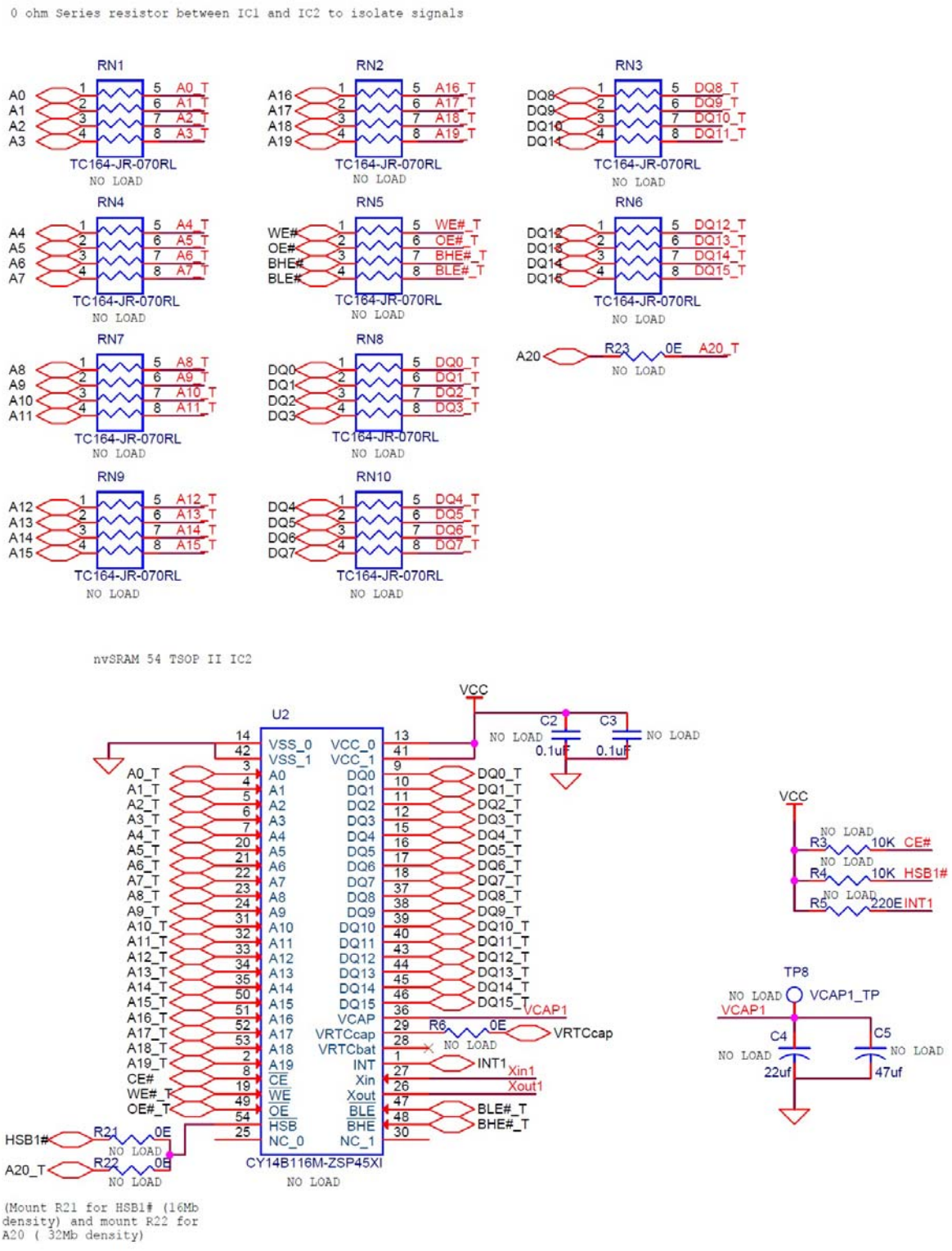
A.2 CY14NVSRAMKIT-001 Kit Components Placement



A.3 CY14NVSRAMKIT-001 Kit Schematic

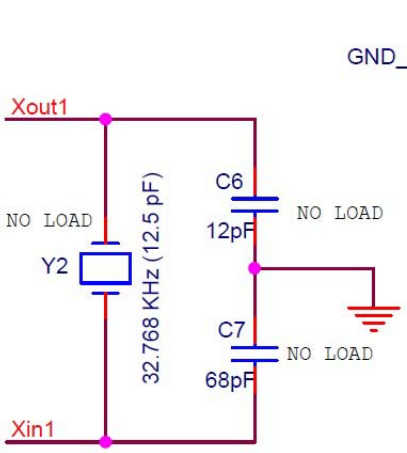


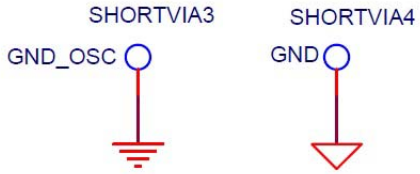

nvSRAM 165 FBGA IC1
U1A
CY14B116M-BZ45XI
U1B
CY14B116M-BZ45XI
U1C
CY14B116M-BZ45XI
VCC
R10 10K CE1#
R11 10K CE2
R12 10K WE#
R13 10K OE#
R14 10K ZZ#
R15 10K HSB#
R16 220E INT
R17 10K BLE#
R18 10K BHE#
TP13
NO LOAD VCAP_TP
VCAP
C10 22uf
C11 NO LOAD 47uf
TP14
NO LOAD VRTCcap_TP
VRTCcap
C12 0.1F
INT Status LED
J5
INT
INT1
JUMPER 2X2
R20 120E
LED2
INT Status LED Red
Decoupling Capacitor
VCC
C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38
0.1uF
Decoupling Capacitor should be placed close to VCC pin
External RTC Components
SHORTVIA1
GND_OSC
SHORTVIA2
GND
Xout
Xin
Y1
32.768 KHz (12.5 pF)
C8 12pF
C9 68pF
Short via 1 and 2 are used for shorting GND_OSC to System GND. GND_OSC and GND will be shorted using a guard ring of 40 mil trace.
Crystal (Y1) and C8, C9 components should be placed closer to U1 device pin.
RTC reference Layout


0 ohm Series resistor between IC1 and IC2 to isolate signals
RN1
A0 A1 A2 A3
A0_T A1_T A2_T A3_T
TC164-JR-070RL
NO LOAD
RN2
A16 A17 A18 A19
A16_T A17_T A18_T A19_T
TC164-JR-070RL
NO LOAD
RN3
DQ8 DQ9 DQ10 DQ11
DQ8_T DQ9_T DQ10_T DQ11_T
TC164-JR-070RL
NO LOAD
RN4
A4 A5 A6 A7
A4_T A5_T A6_T A7_T
TC164-JR-070RL
NO LOAD
RN5
WE# OE# BHE# BLE#
WE#_T OE#_T BHE#_T BLE#_T
TC164-JR-070RL
NO LOAD
RN6
DQ12 DQ13 DQ14 DQ15
DQ12_T DQ13_T DQ14_T DQ15_T
TC164-JR-070RL
NO LOAD
A20 R23 0E A20_T
NO LOAD
RN7
A8 A9 A10 A11
A8_T A9_T A10_T A11_T
TC164-JR-070RL
NO LOAD
RN8
DQ0 DQ1 DQ2 DQ3
DQ0_T DQ1_T DQ2_T DQ3_T
TC164-JR-070RL
NO LOAD
RN9
A12 A13 A14 A15
A12_T A13_T A14_T A15_T
TC164-JR-070RL
NO LOAD
RN10
DQ4 DQ5 DQ6 DQ7
DQ4_T DQ5_T DQ6_T DQ7_T
TC164-JR-070RL
NO LOAD
nvSRAM 54 TSOP II IC2
U2
VSS_0 VSS_1 VCC_0 VCC_1
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 CE WE OE HSB NC_0 NC_1
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 VCAP VRTCcap VRTCbat INT Xin Xout BLE BHE
CY14B116M-ZSP45XI
NO LOAD
VCC
C2 0.1uF
C3 0.1uF
NO LOAD
VCAP1
R6 0E
VRTCcap
NO LOAD
INT1
Xin1
Xout1
R21 0E
HSB1#
R22 0E
A20_T
NO LOAD
(Mount R21 for HSB1# (16Mb density) and mount R22 for A20 (32Mb density)
R3 10K CE#
R4 10K HSB1#
R5 220E INT1
TP8
VCAP1_TP
C4 22uf
C5 47uf

External RTC Components

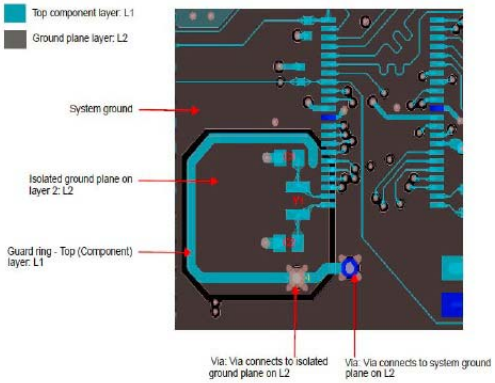
Crystal (Y2) and C6, C7 components should be placed closer to U2 device pin.





Short via 3 and 4 are used for shorting GND_OSC to System GND. GND_OSC and GND will be shorted using a guard ring of 40 mil trace.

RTC reference Layout



A.4 Pin Assignment Table

This section provides the pin map of the headers and their usage.

nvSRAM Pin	FM4 Board (Connector) Pin	MCU Pin	Pin Description	I/O Port
	1	1		
D0	2	2	MADATA00_0	Port 5_0
D1	3	3	MADATA01_0	Port 5_1
D2	4	4	MADATA02_0	Port 5_2
D3	5	5	MADATA03_0	Port 5_3
D4	6	6	MADATA04_0	Port 5_4
D5	7	7	MADATA05_0	Port 5_5
D6	8	8	MADATA06_0	Port 5_6
D7	9	9	MADATA07_0	Port 5_7
D8	10	10	MADATA08_0	Port 5_8
D9	11	11	MADATA09_0	Port 5_9
D10	12	12	MADATA10_0	Port 5_A
D11	13	13	MADATA11_0	Port 5_B
D12	14	14	MADATA12_0	Port 3_0
D13	15	15	MADATA13_0	Port 3_1
D14	16	16	MADATA14_0	Port 3_2
D15	17	17	MADATA15_0	Port 3_3
	18	18		
	19	19		
	20	20		
	21	21		
	22	22		
	23	23		
	24	24		
	25	25		
	26	26		
	27	27	MAD00_0	Port 3_D
A0	28	28	MAD01_0	Port 3_E
A1	29	29	MAD02_0	Port 3_F
	30	30		
	31	31		
	32	32		
	33	33		
	34	34		
	35	35		
	36	36		
	37	37		
	38	38		
	39	39		
	40	40		

nvSRAM Pin	FM4 Board (Connector) Pin	MCU Pin	Pin Description	I/O Port
	41	41		
	42	42		
	43	43		
	44	44		
	45	45		
	46	46		
A2	47	47	MAD03_0	Port 4_B
A3	48	48	MAD04_0	Port 4_C
A4	49	49	MAD05_0	Port 4_D
A5	50	50	MAD06_0	Port 4_E
	51	51		
	52	52		
	53	53		
	54	54		
	55	55		
	56	56		
	57	57		
	58	58		
	59	59		
	60	60		
	61	61		
A6	62	62	MAD07_0	Port 1_0
A7	63	63	MAD08_0	Port 1_1
A8	64	64	MAD09_0	Port 1_2
A9	65	65	MAD10_0	Port 1_3
A10	66	66	MAD11_0	Port 1_4
A11	67	67	MAD12_0	Port 1_5
A12	68	68	MAD13_0	Port 1_6
A13	69	69	MAD14_0	Port 1_7
	70	70		
	71	71		
	72	72		
	73	73		
A14	74	74	MAD15_0	Port 1_8
A15	75	75	MAD16_0	Port 1_9
A16	76	76	MAD17_0	Port 1_A
A17	77	77	MAD18_0	Port 1_B
A18	78	78	MAD19_0	Port 1_C
A19	79	79	MAD20_0	Port 1_D
A20 (32 Mb)	80	80	MAD21_0	Port 1_E
	81	81		
	82	82		
	83	83		

nvSRAM Pin	FM4 Board (Connector) Pin	MCU Pin	Pin Description	I/O Port
INT (54 TSOP)	84	84		Port 2_5
INT (165-FBGA)	85	85		Port 2_4
	86	86		
	87	87		
	88	88		
	89	89		
	90	90		
	91	91		
BHE#	92	92	MDQM1_0	Port 0_E
BLE#	93	93	MDQM0_0	Port 0_D
	94	94		
	95	95		
	96	96		
CE2 (165-FBGA)	97	97	MCSX5_0	Port 0_9
CE1# (165-FBGA)	98	98	MCSX4_0	Port 0_8
	99	99		
CE# (54-TSOP II)	100	100	MCSX3_0	Port 0_6
	101	101		
	102	102		
	103	103		
	104	104		
	105	105		
	106	106		
	107	107		
	108	108		
ZZ#	109	109		Port 6_7
HSB1# (54-TSOP)	110	110		Port 6_6
HSB# (165-FBGA)	111	111		Port 6_5
	112	112		Port 6_4
WE#	113	113	MWEX_0	Port 6_3
OE#	114	114	MOEX_0	Port 6_2
	115	115		
	116	116		
	117	117		
	118	118		
	119	119		
	120	120		

A.5 Bill of Materials (BOM)

Item	Qty	Reference	Value	Description	Manufacturer	Manufacturing Part Number
1	1	N/A	121.69 mm X 67.56 mm, 1.6mm thick, 35 micron, 6 Layer, Enig Finish, High Tg, Blue color Solder mask, white color silk-screen	Cypress Semiconductor		
2	1	C1	10 uF	CAP TANT 10UF 10V 20% 1206	AVX Corporation	TPSA106M010R1800
3	26	C13,C14,C15,C16, C17,C18,C19,C20, C21,C22,C23,C24, C25,C26,C27,C28, C29,C30,C31,C32, C33,C34,C35,C36, C37,C38	0.1uF	CAP CER 0.1UF 50V Y5V 0603	Murata Electronics	GRM188R71C104KA01D
4	1	C10	22uf	CAP TANT 22UF 6.3V 10% 1206	Kemet	T491A226K006AT
5	1	C8	12pF	Multilayer Ceramic Capacitors MLCC - SMD/ SMT 0603 12pF 50volts C0G 1%	Murata Electronics North America	GRM1885C1H120FA01D
6	1	C9	68pF	Multilayer Ceramic Capacitors MLCC - SMD/ SMT 0603 68pF 50volts C0G 1%	Murata Electronics North America	GRM1885C1H680FA01D
7	1	C12	0.1F	CAP 100mF 5.5V THROUGH HOLE	Cornell Dubilier Electronics (CDE)	EDLF104A5R5C
8	2	J1,J3	CONNECTOR EDGE 30X2	Connector Header 60 Position 0.100" (2.54mm) Tin Through Hole	Sullins Connector Solutions	PPTC302LFBN-RC
9	1	J2	CONNECTOR EDGE 2X1	Connector Header 2 Position 0.100" (2.54mm) Tin Through Hole	Sullins Connector Solutions	PPTC021LFBN-RC
10	1	J4	2 Pin Header	CONN HEADER VERT SGL 2POS GOLD	3M	961102-6404-AR
11	1	J5	JUMPER2 (2x2)	CONN HEADER VERT DUAL 4POS GOLD	3M	961204-6404-AR
12	1	LED1	LED Green	LED GREEN CLEAR 0805 SMD	Visual Communications Company - VCC	CMD17-21VGC/TR8
13	1	LED2	LED Red	LED RED CLEAR 0805 SMD	Visual Communications Company - VCC	CMD17-21VRC/TR8
14	1	R2	330E	RES SMD 330 OHM 1% 1/10W 0603	Panasonic Electronic Components	ERJ-3EKF3300V

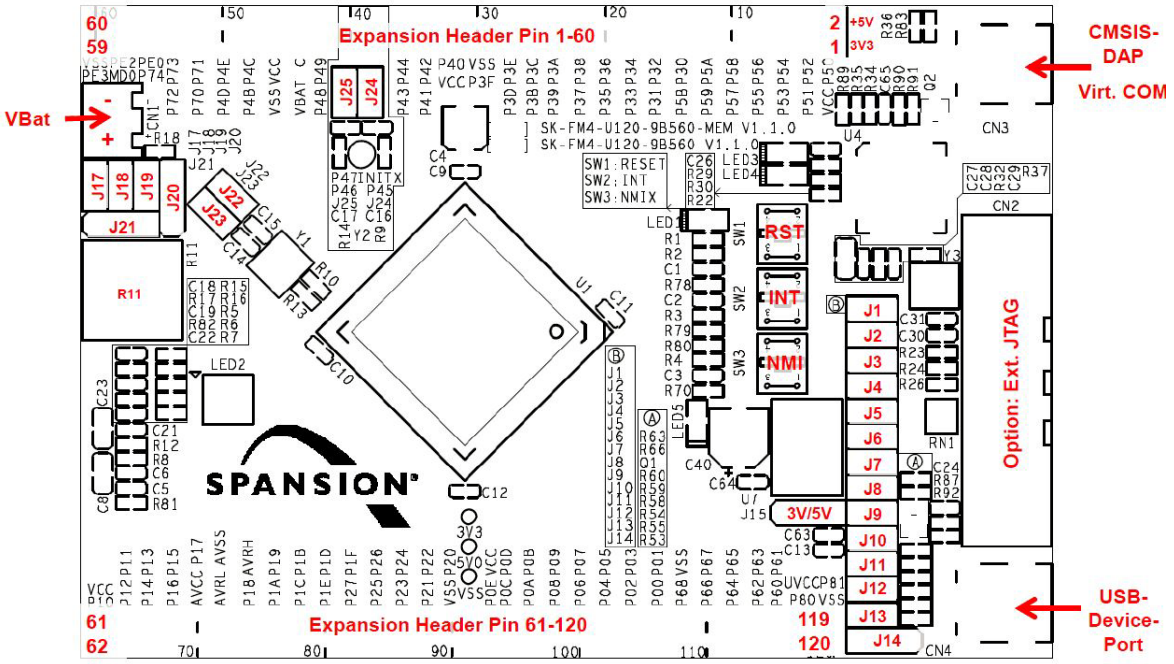
Item	Qty	Reference	Value	Description	Manufacturer	Manufacturing Part Number
15	1	R16	220E	RES SMD 220 OHM 1% 1/10W 0603	Panasonic Electronic Components	ERJ-3EKF2200V
16	8	R10,R11,R12,R13, R14,R15,R17,R18	10K	RES SMD 10K OHM 1% 1/10W 0603	Panasonic Electronic Components	ERJ-3EKF1002V
17	1	R20	120E	RES 120 OHM 1/10W 1% 0603 SMD	Panasonic - ECG	ERJ-3EKF1200V
18	1	TP1	GND	TEST POINT PC MINI .040"D Black	Keystone Electronics	5001
19	1	TP3	VCC	TEST POINT PC MINI .040"D Black	Keystone Electronics	5001
20	1	TVS1	3.6V 350W	TVS DIODE 3VWM 12VC SOD523	Vishay Semiconductor Diodes Division	VESD03-02V-G-08
21	1	U1	CY14B116M-BZ45XI	IC nvSRAM 16Mbit X16 45ns 165FBGA	Cypress Semiconductor	CY14B116M-BZ45XI
22	1	Y1	32.768 KHz (12.5 pF)	Crystal 32.7680kHz 20ppm 12.5pF 50 kOhm -40°C - 85°C Surface Mount Cylindrical Can, Radial	Citizen Finedevice Co Ltd	CMR200T32.768KDZF-UT
23	2	N/A	N/A	Headers & Wire Housings 2.54MM SHUNT	3M	969102-0000-DA
24	4	N/A	N/A	BUMPER CYLINDRICAL .312X.215 BLACK	Bumpon Protective Products Rollstock	SJ61A6
No Load Components						
25	2	C5,C11	47uf	CAP TANT 47UF 6.3V 20% 1206	Kemet	T491A476M006AT
26	1	TP4	HSB#	TEST POINT PC MINI .040"D Black	Keystone Electronics	5001
27	1	TP6	HSB1#	TEST POINT PC MINI .040"D Black	Keystone Electronics	5001
28	1	TP7	INT1	TEST POINT PC MINI .040"D Black	Keystone Electronics	5001
29	1	TP2	GND	TEST POINT PC MINI .040"D Black	Keystone Electronics	5001
30	1	TP5	INT	TEST POINT PC MINI .040"D Black	Keystone Electronics	5001
31	1	TP8	VCAP1_TP	TEST POINT PC MINI .040"D Black	Keystone Electronics	5001
32	1	TP13	VCAP_TP	TEST POINT PC MINI .040"D Black	Keystone Electronics	5001
33	1	TP14	VRTCcap_TP	TEST POINT PC MINI .040"D Black	Keystone Electronics	5001
34	1	Y2	32.768 KHz (12.5 pF)	Crystal 32.7680kHz 20ppm 12.5pF 50 kOhm -40°C - 85°C Surface Mount Cylindrical Can, Radial	Citizen Finedevice Co Ltd	CMR200T32.768KDZF-UT

Item	Qty	Reference	Value	Description	Manufacturer	Manufacturing Part Number
35	1	U2	CY14B116M-ZSP45XI	IC NVSRAM 16MBIT X16 45NS 54 TSOP II	Cypress Semiconductor	CY14B116M-ZSP45XI
36	10	RN1,RN2,RN3,RN4,RN5,RN6,RN7,RN8,RN9,RN10	TC164-JR-070RL	RES ARRAY ZERO OHM 4 RES 1206	Yageo	TC164-JR-070RL
37	4	R6,R21,R22,R23	0E	RES 0.0 OHM 1/10W 0603 SMD	Panasonic - ECG	ERJ-3GEY0R00V
38	2	C2,C3	0.1uF	CAP CER 0.1UF 50V Y5V 0603	Murata Electronics	GRM188R71C104KA01D
39	1	C4	22uf	CAP TANT 22UF 6.3V 10% 1206	Kemet	T491A226K006AT
40	1	C6	12pF	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0603 12pF 50volts C0G 1%	Murata Electronics North America	GRM1885C1H120FA01D
41	1	C7	68pF	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0603 68pF 50volts C0G 1%	Murata Electronics North America	GRM1885C1H680FA01D
42	1	R5	220E	RES SMD 220 OHM 1% 1/10W 0603	Panasonic Electronic Components	ERJ-3EKF2200V
43	2	R3,R4	10K	RES SMD 10K OHM 1% 1/10W 0603	Panasonic Electronic Components	ERJ-3EKF1002V
Special Jumper Installation Instructions						
44	1	J4	Install jumper across pins 1 and 2	Headers & Wire Housings 2.54MM SHUNT	3M	969102-0000-DA
45	1	J5	Install jumper across pins 1 and 2 for INT output	Headers & Wire Housings 2.54MM SHUNT	3M	969102-0000-DA
Label						
46	1	N/A	N/A	LBL, PCA Label, Vendor Code, Datecode, Serial Number 121-60231-01 REV 01 (YYWWVVXXXXX)	Cypress Semiconductor	
47	1	N/A	N/A	LBL, CY14NVSRAMKIT-001 QR Code, 10mm X 10mm	Cypress Semiconductor	
48	1	N/A	N/A	LBL, Anti-Static Warning, ULINE PN S-6516, 5/8" x 2", "Attention Observe Precautions	"Cypress Semiconductor	
Install on Bottom of PCB As per the Silk Screen in the Corners						
49	4	N/A	N/A	BUMPER CYLINDRICAL .312X.215 BLACK	Bumpon Protective Products Rollstock	SJ61A6

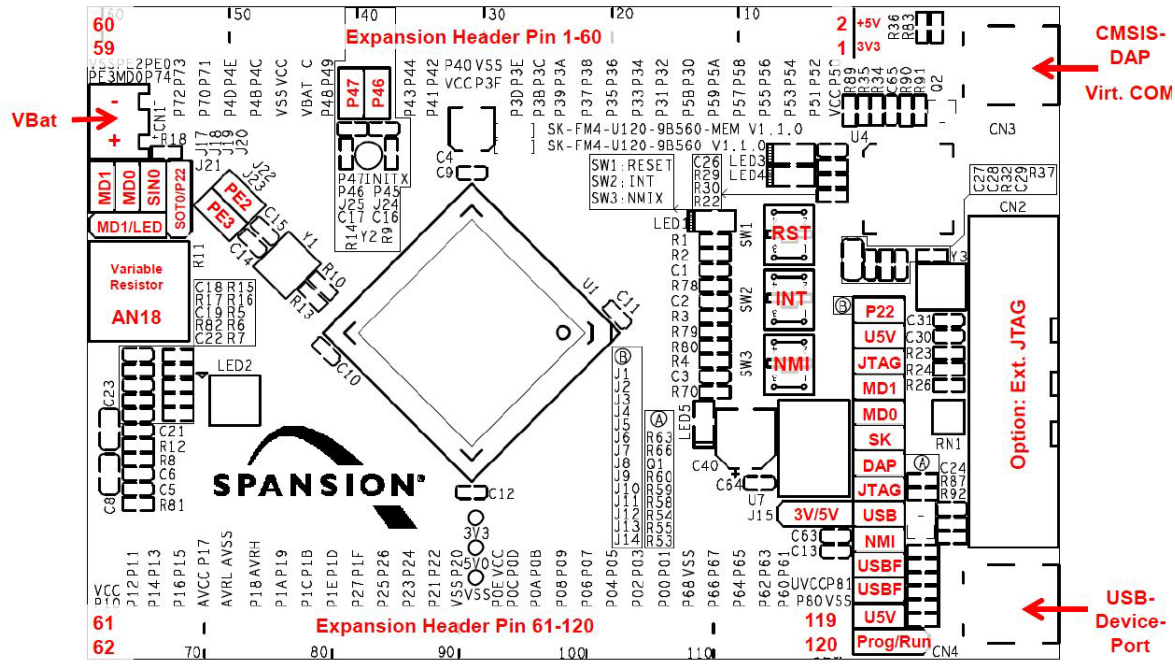
A.6 FM4 MCU Evaluation Board

This section provides details on the SK-FM4-U120-9B560 FM4 MCU Evaluation Board jumpers and their settings in Program and Run modes.

A.6.1 FM4 MCU Evaluation Hardware (Top Side) - Jumper Details



A.6.2 FM4 MCU Evaluation Hardware (Top Side) - Jumper Function Overview



A.6.3 Jumper Setting Table - SK-FM4-U120-9B560 FM4 MCU Evaluation Board

Table A-1. FM4 MCU Evaluation Board

Jumper	No of Pins	Jumper Function	SK-FM4-U120-9B560 Board (Default setting marked bold)
J1	2	CMSIS-DAP Crystal (P22) (Do not change!)	**Open: 4MHz** Closed: 48MHz
J2	2	VBUS detection of CMSIS-DAP	**Open: 3V3** Closed: 5V (only for SK-FM4-U120-9B560)
J3	2	CMSIS-DAP reset	**Open: CMSIS-DAP normal operation** Closed: CMSIS-DAP reset assert
J4	2	Operation of MD1 (CMSIS-DAP)	**Open: Run-Mode** Closed: Test-Mode
J5	2	Operation of MD0 (CMSIS-DAP)	**Open: Run-Mode (CMSIS-DAP)** Closed: Firmware update of CMSIS-DAP
J6	2	Power Supply Source Select only one power source!	**J9: USB Host powered (CN4)** J8: JTAG powered (CN2) J7: CMSIS-DAP powered (CN3) J6: Powered by SK-FM4-U-PERIPHERAL (J16)
J7	2		
J8	2		
J9	2		
J10	2	SW3 NMI Jumper J10 needs to be opened for programming	Open: Button SW3 disconnected / Programming mode **Closed: Button SW3 (NMI) is connected**
J11	2	USB D+	Open: USB is disconnected **Closed: USB is connected**
J12	2	USB D–	Open: USB is disconnected **Closed: USB is connected**
J13	2	VBUS detection	**Open: 3V3** Closed: 5V (only for SK-FM4-U120-9B560)
J14	3	USB VBUS detection See also J10	**1-2: VBUS is connected to INT03_2 (Run-Mode)** 2-3: VBUS is connected to NMIX (Programming Mode)
J15	3	MCU voltage selection SK-FM4-U120-9B560	**1-2: MCU is powered from 3V3** 2-3: MCU is powered from 5V
J16	2	Can be powered by peripheral base-board	See note in J6-J9 setting
J17	2	Operation of MD1 (Do not change!)	**Open: Run-Mode and Programming-Mode** Closed: Test-Mode
J18	2	Operation of MD0	**Open: Run-Mode** Closed: Programming-Mode
J19	2	CMSIS-DAP Virtual COM port (SIN0_0)	Open: SIN0 is disconnected from CMSIS-DAP **Closed: CMSIS-DAP's virtual COM port is connect**

Table A-1. FM4 MCU Evaluation Board

Jumper	No of Pins	Jumper Function	SK-FM4-U120-9B560 Board (Default setting marked bold)
J20	3	CMSIS-DAP Virtual COM port (SOT0_0)	2-3: SOT0/P22 is used for USB programming **1-2: CMSIS-DAP's virtual COM port is connected**
J21	3	MD1/PE0 See also J17	1-2: MD1 (Programming-Mode) **2-3: PE0 (LED Blue)**
J22	2	X0/PE2 Do not close J22 if crystal Y1 is assembled.	**Open: PE2 is disconnected** Closed: PE2 is connected to pin header U2
J23	2	X1/PE3 Do not close J23 if crystal Y1 is assembled.	**Open: PE3 is disconnected** Closed: PE3 is connected to pin header U2
J24	2	X0A/P46 Do not close J24 if crystal Y2 is assembled.	**Open: P46 is disconnected** Closed: PE2 is connected to pin header U2
J25	2	X1A/P47 Do not close J25 if crystal Y2 is assembled.	**Open: P47 is disconnected** Closed: PE2 is connected to pin header U2

A.6.4 Jumper Setting Table - FM4 MCU Evaluation Board Programming Mode

Table A-2. Programming Mode

Jumper Reference	Jumper Name	Jumper Function
J7	DAP	CMSIS-DAP powered (CN3)
J10	NMI	Retain as is to default jumper setting
J11	USBF	Retain as is to default jumper setting
J12	USBF	Retain as is to default jumper setting
J14	Prog	Configures the FM4 MCU in programming mode
J15	3V	Configures the 3.3 V operation
J18	MD0	Sets Mode 0 pin (MD0) for programming
J19	SIN0	Sets serial interface channel 1 input pin (SIN0) for programming
J20	SOT0	Sets serial interface channel 0 output (SOT0) for programming
J21	MD1	Sets Mode 1 pin (MD1) for programming
J1-J6, J8, J9, J13, J16, J17, J22-J25	See Table A-1	These jumpers are not populated by default (Open) on the FM4 MCU Evaluation Board

A.6.5 Jumper Setting Table - FM4 MCU Evaluation Board Run Mode

Table A-3. Run Mode

Jumper Reference	Jumper Name	Jumper Function
J9	USB	USB Host powered (CN4)
J10	NMI	Retain as is to default jumper setting
J11	USBF	Retain as is to default jumper setting
J12	USBF	Retain as is to default jumper setting
J14	Run	Configures the FM4 MCU in run mode
J15	3V	Configures the 3.3 V operation
J18	MD0	Sets Mode 0 pin (MD0) for programming
J19	SIN0	Sets serial interface channel 1 input pin (SIN0) for CMSIS-DAP's virtual COM port
J20	SOT0	Sets serial interface channel 0 output (SOT0) for CMSIS-DAP's virtual COM port
J21	LED	Sets jumper for blue LED (LED2)
J1-J8, J13, J16, J17, J22-J25	See Table A-1	These jumpers are not populated by default (Open) on the FM4 MCU Evaluation Board

Revision History

Document Revision History

CY14NVSRAMKIT-001 nvSRAM Development Kit User Guide Revision History

Document Title: CY14NVSRAMKIT-001 nvSRAM Development Kit User Guide Document Number: 002-03522				
Revision	**ECN#**	**Issue Date**	**Origin of Change**	**Description of Change**
**	5052981	12/16/2015	ZSK	Initial version of kit guide.
*A	5713267	04/26/2017	SHEA	Updated logo and copyright