

## 74ABT2952 Octal Registered Transceiver

### General Description

The ABT2952 is an octal registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-STATE output enable signals are provided for each register. The output pins are guaranteed to source 32 mA and to sink 64 mA.

### Features

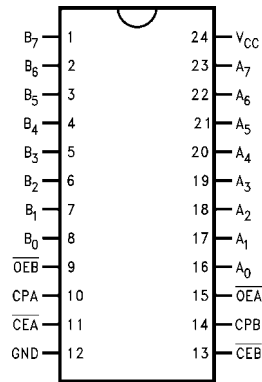
- Separate clock, clock enable and 3-STATE output enable provided for each register
- A and B output sink capability of 64 mA source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

### Ordering Code:

| Order Number  | Package Number | Package Description   |
|---------------|----------------|---|
| 74ABT2952CSC  | M24B           | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body |
| 74ABT2952CMSA | MSA24          | 24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide           |
| 74ABT2952CMTC | MTC24          | 24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide     |

Device also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



### Pin Descriptions

| Pin Names                      | Description                                  |
|--------------------------------|--|
| A <sub>0</sub> -A <sub>7</sub> | A-Register Inputs/B-Register 3-STATE Outputs |
| B <sub>0</sub> -B <sub>7</sub> | B-Register Inputs/A-Register 3-STATE Outputs |
| $\overline{\text{OEA}}$        | Output Enable A-Register                     |
| CPA                            | A-Register Clock                             |
| $\overline{\text{CEA}}$        | A-Register Clock Enable                      |
| $\overline{\text{OEB}}$        | Output Enable B-Register                     |
| CPB                            | B-Register Clock                             |
| $\overline{\text{CEB}}$        | B-Register Clock Enable                      |

### Truth Table

Output Control

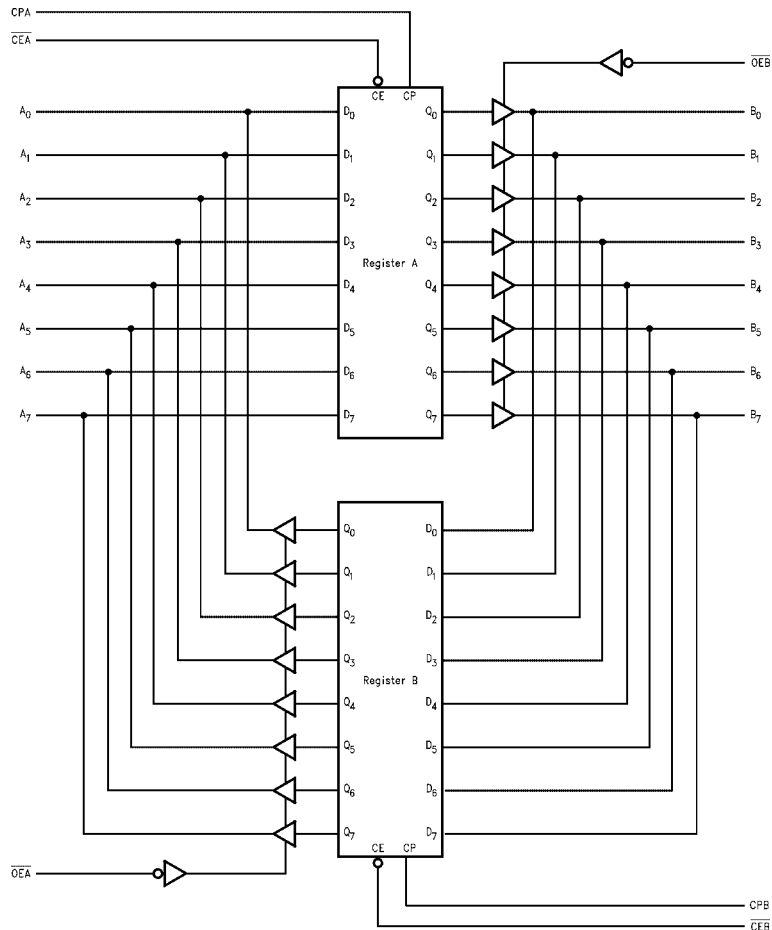
| $\overline{OE}$ | Internal Q | Output | Function        |
|-----------------|------------|--------|-----------------|
| H               | X          | Z      | Disable Outputs |
| L               | L          | L      | Enable Outputs  |
| L               | H          | H      |                 |

Register Function Table (Applies to A or B Register)

| Inputs |    |                 | Internal | Function  |
|--------|----|-----------------|----------|-----------|
| D      | CP | $\overline{CE}$ | Q        |           |
| X      | X  | H               | NC       | Hold Data |
| L      | ↗  | L               | L        | Load Data |
| H      | ↗  | L               | H        |           |

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = HIGH Impedance  
 ↗ = LOW-to-HIGH Transition  
 NC = No Change

### Block Diagram



**Absolute Maximum Ratings**(Note 1)

|   |                                      |
|---|--------------------------------------|
| Storage Temperature   | -65°C to +150°C                      |
| Ambient Temperature under Bias  | -55°C to +125°C                      |
| Junction Temperature under Bias                                       | -55°C to +150°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin                           | -0.5V to +7.0V                       |
| Input Voltage (Note 2)  | -0.5V to +7.0V                       |
| Input Current (Note 2)  | -30 mA to +5.0 mA                    |
| Voltage Applied to Any Output<br>in the Disable or<br>Power-Off State | -0.5V to +5.5V                       |
| in the HIGH State   | -0.5V to V <sub>CC</sub>             |
| Current Applied to Output<br>in LOW State (Max)                       | twice the rated I <sub>OL</sub> (mA) |
| DC Latchup Source Current   | -500 mA                              |
| Over Voltage Latchup (I/O)  | 10V                                  |

**Recommended Operating Conditions**

|   |                |
|---|----------------|
| Free Air Ambient Temperature                    | -40°C to +85°C |
| Supply Voltage                                  | +4.5V to +5.5V |
| Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) |                |
| Data Input                                      | 50 mV/ns       |
| Enable Input                                    | 20 mV/ns       |
| Clock Input                                     | 100 mV/ns      |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

| Symbol                             | Parameter                               | Min        | Typ | Max      | Units  | V <sub>CC</sub> | Conditions  |
|------------------------------------|---|------------|-----|----------|--------|-----------------|---|
| V <sub>IH</sub>                    | Input HIGH Voltage                      | 2.0        |     |          | V      |                 | Recognized HIGH Signal  |
| V <sub>IL</sub>                    | Input LOW Voltage                       |            |     | 0.8      | V      |                 | Recognized LOW Signal   |
| V <sub>CD</sub>                    | Input Clamp Diode Voltage               |            |     | -1.2     | V      | Min             | I <sub>IN</sub> = -18 mA (Non I/O Pins)   |
| V <sub>OH</sub>                    | Output HIGH Voltage                     | 2.5<br>2.0 |     |          |        |                 | I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> )<br>I <sub>OH</sub> = -32 mA (A <sub>n</sub> , B <sub>n</sub> )                     |
| V <sub>OL</sub>                    | Output LOW Voltage                      |            |     | 0.55     | V      | Min             | I <sub>OL</sub> = 64 mA (A <sub>n</sub> , B <sub>n</sub> )  |
| V <sub>ID</sub>                    | Input Leakage Test                      | 4.75       |     |          | V      | 0.0             | I <sub>ID</sub> = 1.9 μA (Non-I/O Pins)<br>All Other Pins Grounded  |
| I <sub>IH</sub>                    | Input HIGH Current                      |            |     | 1<br>1   | μA     | Max             | V <sub>IN</sub> = 2.7V (Non-I/O Pins) (Note 3)<br>V <sub>IN</sub> = V <sub>CC</sub> (Non-I/O Pins)  |
| I <sub>BVI</sub>                   | Input HIGH Current Breakdown Test       |            |     | 7        | μA     | Max             | V <sub>IN</sub> = 7.0V (Non-I/O Pins)   |
| I <sub>BVIT</sub>                  | Input HIGH Current Breakdown Test (I/O) |            |     | 100      | μA     | Max             | V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )   |
| I <sub>IL</sub>                    | Input LOW Current                       |            |     | -1<br>-1 | μA     | Max             | V <sub>IN</sub> = 0.5V (Non-I/O Pins) (Note 3)<br>V <sub>IN</sub> = 0.0V (Non-I/O Pins)   |
| I <sub>IH</sub> + I <sub>OZH</sub> | Output Leakage Current                  |            |     | 10       | μA     | 0V-5.5V         | V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> );<br>OE <sub>A</sub> or OE <sub>B</sub> = 2.0V                                      |
| I <sub>IL</sub> + I <sub>OZL</sub> | Output Leakage Current                  |            |     | -10      | μA     | 0V-5.5V         | V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> );<br>OE <sub>A</sub> or OE <sub>B</sub> = 2.0V                                      |
| I <sub>OS</sub>                    | Output Short-Circuit Current            | -100       |     | -275     | mA     | Max             | V <sub>OUT</sub> = 0V (A <sub>n</sub> , B <sub>n</sub> )  |
| I <sub>CEX</sub>                   | Output HIGH Leakage Current             |            |     | 50       | μA     | Max             | V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> , B <sub>n</sub> )   |
| I <sub>ZZ</sub>                    | Bus Drainage Test                       |            |     | 100      | μA     | 0.0V            | V <sub>OUT</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> );<br>All Others GND   |
| I <sub>CCH</sub>                   | Power Supply Current                    |            |     | 250      | μA     | Max             | All Outputs HIGH  |
| I <sub>CCL</sub>                   | Power Supply Current                    |            |     | 30       | mA     | Max             | All Outputs LOW   |
| I <sub>CCZ</sub>                   | Power Supply Current                    |            |     | 50       | μA     | Max             | Outputs 3-STATE;<br>All Others GND  |
| I <sub>CCT</sub>                   | Additional I <sub>CC</sub> /Input       |            |     | 2.5      | mA     | Max             | V <sub>I</sub> = V <sub>CC</sub> - 2.1V; All Others<br>at V <sub>CC</sub> or GND  |
| I <sub>CCD</sub>                   | Dynamic I <sub>CC</sub><br>(Note 4)     | No Load    |     | 0.18     | mA/MHz | Max             | Outputs Open<br>OE <sub>A</sub> or OE <sub>B</sub> = GND,<br>Non-I/O = GND or V <sub>CC</sub><br>One Bit toggling, 50% duty cycle<br>(Note 4) |

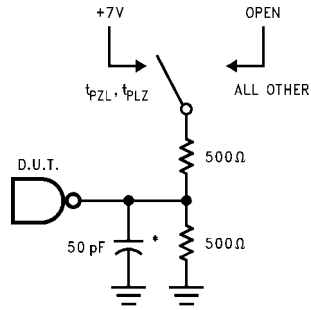
**Note 3:** Guaranteed, but not tested.

**Note 4:** For 8-bit toggling, I<sub>CCD</sub> < 1.4 mA/MHz.

| DC Electrical Characteristics   |  |   |      |   |   |                 |  |
|---|--|---|------|---|---|-----------------|--|
| (SOIC Package)  |  |   |      |   |   |                 |  |
| Symbol  | Parameter  | Min   | Typ  | Max   | Units   | V <sub>CC</sub> | Conditions<br>C <sub>L</sub> = 50 pF,<br>R <sub>L</sub> = 500Ω |
| V <sub>OLP</sub>  | Quiet Output Maximum Dynamic V <sub>OL</sub>   |   | 0.6  | 0.8   | V   | 5.0             | T <sub>A</sub> = 25°C (Note 5)                                 |
| V <sub>OLV</sub>  | Quiet Output Minimum Dynamic V <sub>OL</sub>   | -1.2  | -1.0 |   | V   | 5.0             | T <sub>A</sub> = 25°C (Note 5)                                 |
| V <sub>OHV</sub>  | Minimum HIGH Level Dynamic Output Voltage  | 2.5   | 3.0  |   | V   | 5.0             | T <sub>A</sub> = 25°C (Note 6)                                 |
| V <sub>IHD</sub>  | Minimum HIGH Level Dynamic Input Voltage   | 2.0   | 1.7  |   | V   | 5.0             | T <sub>A</sub> = 25°C (Note 7)                                 |
| V <sub>ILD</sub>  | Maximum LOW Level Dynamic Input Voltage  |   | 1.2  | 0.8   | V   | 5.0             | T <sub>A</sub> = 25°C (Note 7)                                 |
| <p><b>Note 5:</b> Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.</p> <p><b>Note 6:</b> Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.</p> <p><b>Note 7:</b> Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). Guaranteed, but not tested.</p> |  |   |      |   |   |                 |  |
| AC Electrical Characteristics   |  |   |      |   |   |                 |  |
| (SOIC and SSOP Package)   |  |   |      |   |   |                 |  |
| Symbol  | Parameter  | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |      |   | T <sub>A</sub> = -40°C to +85°C<br>V <sub>CC</sub> = 4.5V to 5.5V<br>C <sub>L</sub> = 50 pF |                 | Units  |
|   |  | Min   | Typ  | Max   | Min   | Max             |  |
| f <sub>MAX</sub>  | Maximum Clock Frequency  | 200   |      |   | 200   |                 | MHz  |
| t <sub>PLH</sub><br>t <sub>PHL</sub>  | Propagation Delay<br>CPA or CPB to<br>A <sub>n</sub> or B <sub>n</sub>                     | 1.5   | 3.4  | 5.3   | 1.5   | 5.3             | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub>  | Output Enable Time<br>OE $\bar{A}$ or OE $\bar{B}$ to<br>A <sub>n</sub> or B <sub>n</sub>  | 1.5   | 3.2  | 5.5   | 1.5   | 5.5             | ns   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub>  | Output Disable Time<br>OE $\bar{A}$ or OE $\bar{B}$ to<br>A <sub>n</sub> or B <sub>n</sub> | 1.5   | 3.6  | 6.0   | 1.5   | 6.0             | ns   |
| AC Operating Requirements   |  |   |      |   |   |                 |  |
| Symbol  | Parameter  | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |      | T <sub>A</sub> = -40°C to +85°C<br>V <sub>CC</sub> = 4.5V to 5.5V<br>C <sub>L</sub> = 50 pF |   | Units           |  |
|   |  | Min   | Max  | Min   | Max   |                 |  |
| t <sub>S</sub> (H)<br>t <sub>S</sub> (L)  | Setup Time, HIGH<br>or LOW A <sub>n</sub> or B <sub>n</sub><br>to CPA or CPB               | 2.5   |      | 2.5   |   | ns              |  |
| t <sub>H</sub> (H)<br>t <sub>H</sub> (L)  | Hold Time, HIGH<br>or LOW A <sub>n</sub> or B <sub>n</sub><br>to CPA or CPB                | 1.5   |      | 1.5   |   | ns              |  |
| t <sub>S</sub> (H)<br>t <sub>S</sub> (L)  | Setup Time, HIGH<br>or LOW CEA or CEB<br>to CPA or CPB                                     | 2.5   |      | 2.5   |   | ns              |  |
| t <sub>H</sub> (H)<br>t <sub>H</sub> (L)  | Hold Time, HIGH<br>or LOW CEA or CEB<br>to CPA or CPB                                      | 1.5   |      | 1.5   |   | ns              |  |
| t <sub>W</sub> (H)<br>t <sub>W</sub> (L)  | Pulse Width,<br>HIGH or LOW<br>CPA or CPB  | 3.0   |      | 3.0   |   | ns              |  |

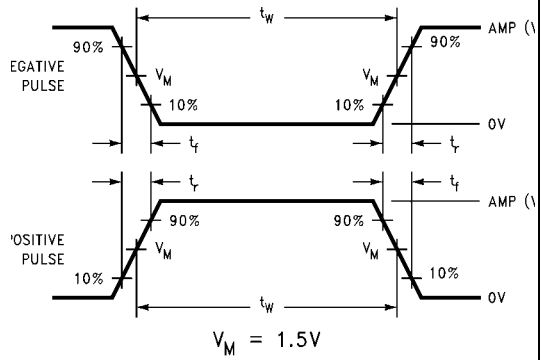
| Extended AC Electrical Characteristics   |  |  |       |  |     |  |      |       |
|--|--|--|-------|--|-----|--|------|-------|
| (SOIC Package)   |  |  |       |  |     |  |      |       |
| Symbol   | Parameter  | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$<br>$V_{CC} = 4.5\text{V to } 5.5\text{V}$<br>$C_L = 50\text{ pF}$<br>8 Outputs Switching<br>(Note 8) |       | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$<br>$V_{CC} = 4.5\text{V to } 5.5\text{V}$<br>$C_L = 250\text{ pF}$<br>(Note 9)                       |     | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$<br>$V_{CC} = 4.5\text{V to } 5.5\text{V}$<br>$C_L = 250\text{ pF}$<br>8 Outputs Switching<br>(Note 10) |      | Units |
|  |  | Min  | Max   | Min  | Max | Min  | Max  |       |
| $t_{PLH}$  | Propagation Delay                                      | 1.5  | 6.0   | 2.0  | 8.0 | 2.5  | 10.5 | ns    |
| $t_{PHL}$  | CPA or CPB to $A_n$ or $B_n$                           | 1.5  | 6.0   | 2.0  | 8.0 | 2.5  | 10.5 |       |
| $t_{PZH}$  | Output Enable Time                                     | 1.5  | 6.0   | 2.0  | 8.0 | 2.5  | 11.5 | ns    |
| $t_{PZL}$  | $\overline{OEA}$ or $\overline{OEB}$ to $A_n$ or $B_n$ | 1.5  | 6.0   | 2.0  | 8.0 | 2.5  | 11.5 |       |
| $t_{PHZ}$  | Output Disable Time                                    | 1.5  | 6.0   | (Note 11)  |     | (Note 11)  |      | ns    |
| $t_{PZL}$  | $\overline{OEA}$ or $\overline{OEB}$ to $A_n$ or $B_n$ | 1.5  | 6.0   |  |     |  |      |       |
| <p><b>Note 8:</b> This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).</p> <p><b>Note 9:</b> This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.</p> <p><b>Note 10:</b> This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.</p> <p><b>Note 11:</b> The 3-STATE delays are dominated by the RC network (500<math>\Omega</math>, 250 pF) on the output and has been excluded from the datasheet.</p>   |  |  |       |  |     |  |      |       |
| Skew   |  |  |       |  |     |  |      |       |
| (SOIC Package)   |  |  |       |  |     |  |      |       |
| Symbol   | Parameter  | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$<br>$V_{CC} = 4.5\text{V} - 5.5\text{V}$<br>$C_L = 50\text{ pF}$<br>8 Outputs Switching<br>(Note 12)  |       | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$<br>$V_{CC} = 4.5\text{V} - 5.5\text{V}$<br>$C_L = 250\text{ pF}$<br>8 Outputs Switching<br>(Note 13) |     | Units  |      |       |
|  |  | Max  |       | Max  |     |  |      |       |
| $t_{OSHL}$<br>(Note 14)  | Pin to Pin Skew<br>HL Transitions                      | 1.0  |       | 1.5  |     | ns   |      |       |
| $t_{OSLH}$<br>(Note 14)  | Pin to Pin Skew<br>LH Transitions                      | 1.0  |       | 2.0  |     | ns   |      |       |
| $t_{PS}$<br>(Note 15)  | Duty Cycle<br>LH-HL Skew                               | 2.0  |       | 4.5  |     | ns   |      |       |
| $t_{OST}$<br>(Note 14)   | Pin to Pin Skew<br>LH/HL Transitions                   | 2.1  |       | 4.5  |     | ns   |      |       |
| $t_{PV}$<br>(Note 16)  | Device to Device Skew<br>LH/HL Transitions             | 2.5  |       | 5.0  |     | ns   |      |       |
| <p><b>Note 12:</b> This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).</p> <p><b>Note 13:</b> This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.</p> <p><b>Note 14:</b> Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (<math>t_{OSHL}</math>), LOW to HIGH (<math>t_{OSLH}</math>), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (<math>t_{OST}</math>). This specification is guaranteed but not tested.</p> <p><b>Note 15:</b> This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.</p> <p><b>Note 16:</b> Propagation delay variation for a given set of conditions (i.e., temperature and <math>V_{CC}</math>) from device to device. This specification is guaranteed but not tested.</p> |  |  |       |  |     |  |      |       |
| Capacitance  |  |  |       |  |     |  |      |       |
| Symbol   | Parameter  | Typ  | Units | Conditions<br>$T_A = 25^\circ\text{C}$   |     |  |      |       |
| $C_{IN}$   | Input Capacitance                                      | 5  | pF    | $V_{CC} = 0\text{V}$ (Non I/O Pins)  |     |  |      |       |
| $C_{I/O}$ (Note 17)  | Output Capacitance                                     | 11   | pF    | $V_{CC} = 5.0\text{V}$ ( $A_n, B_n$ )  |     |  |      |       |
| <p><b>Note 17:</b> <math>C_{I/O}</math> is measured at frequency <math>f = 1\text{ MHz}</math>, per MIL-STD-883, Method 3012.</p>  |  |  |       |  |     |  |      |       |

**AC Loading**



\*Includes jig and probe capacitance

**FIGURE 1. Standard AC Test Load**

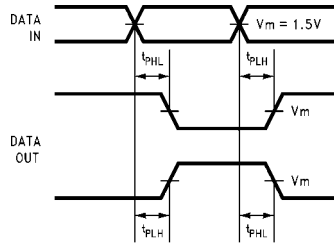


**FIGURE 2. Test Input Signal Levels**

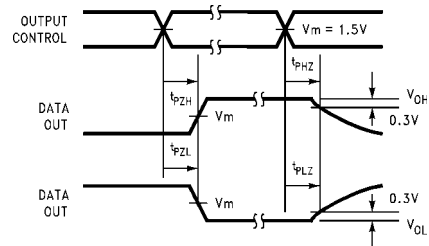
| Amplitude | Rep. Rate | $t_w$  | $t_r$  | $t_f$  |
|-----------|-----------|--------|--------|--------|
| 3.0V      | 1 MHz     | 500 ns | 2.5 ns | 2.5 ns |

**FIGURE 3. Input Signal Requirements**

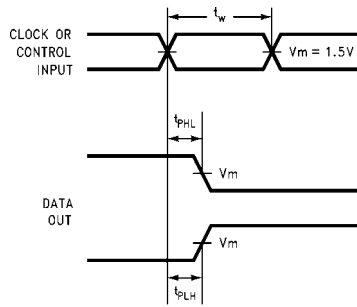
**AC Waveforms**



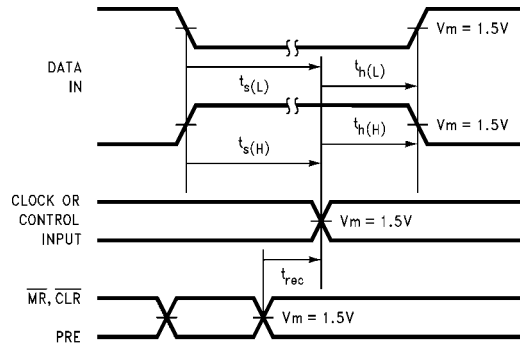
**FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**



**FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times**

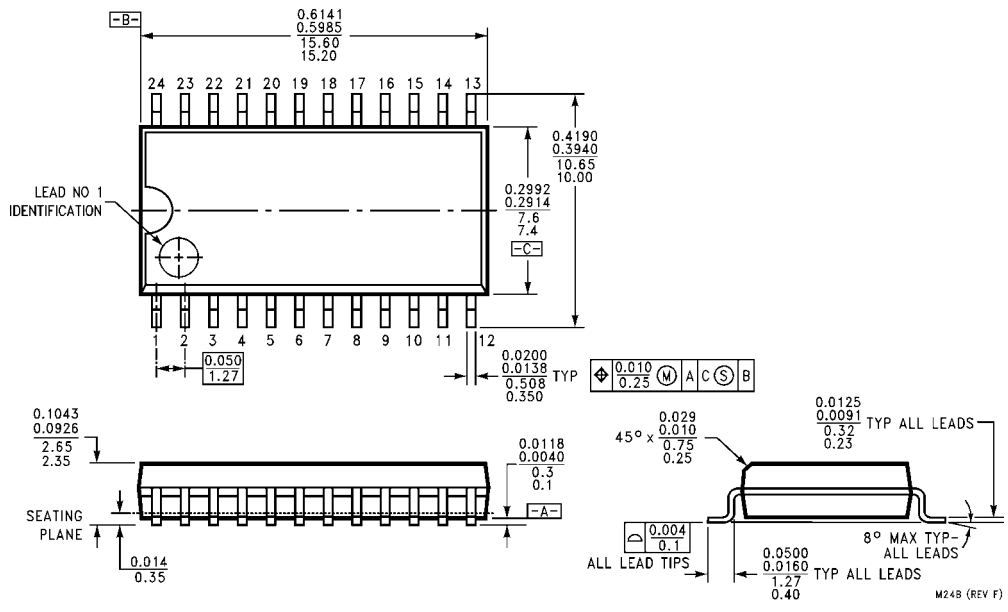


**FIGURE 5. Propagation Delay, Pulse Width Waveforms**

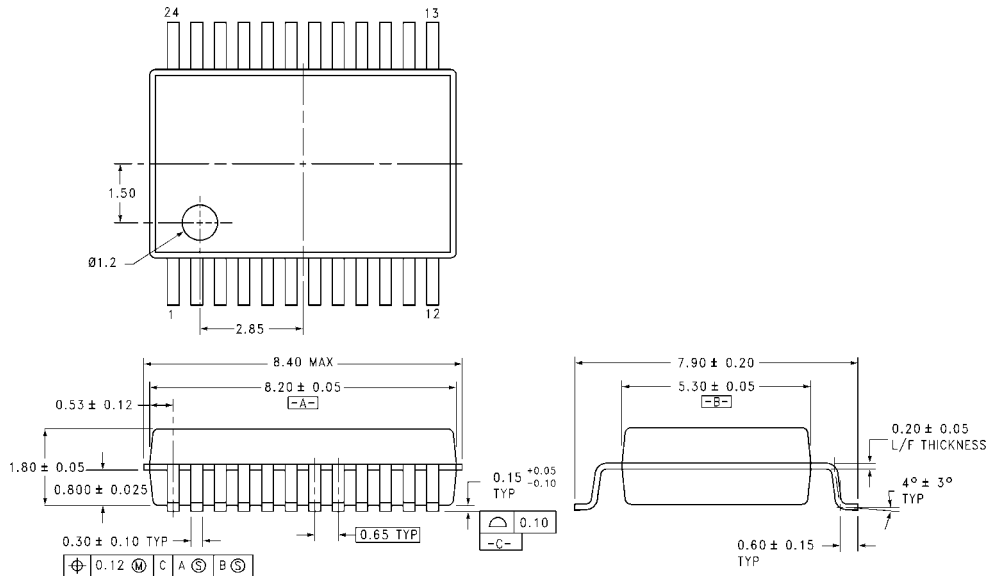


**FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms**

**Physical Dimensions** inches (millimeters) unless otherwise noted

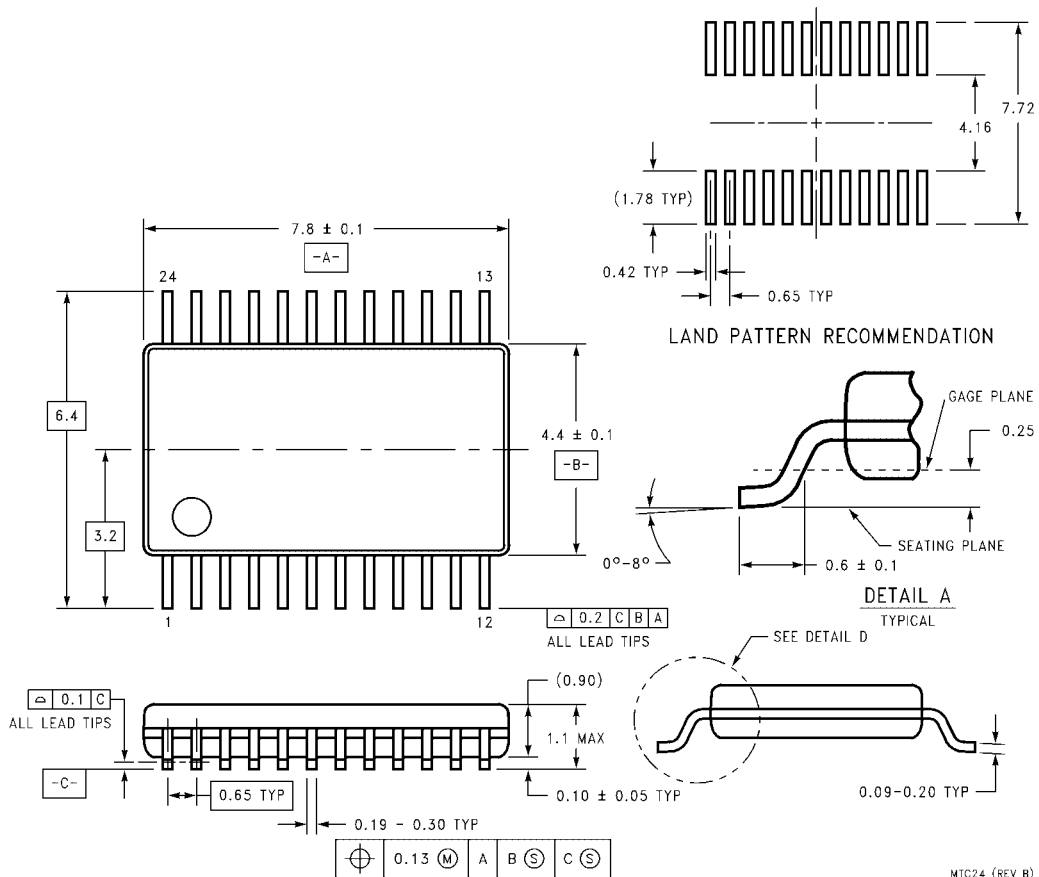


**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body  
Package Number M24B**



**24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide  
Package Number MSA24**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC24**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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