Demo Board User Manual for SiP12107 (3 A) and SiP12108 (5 A), 2.7 V to 5.5 V Synchronous Buck Regulators

THE CHIP

DESCRIPTION

The SiP12107/SiP12108 is a high frequency current-mode constant on-time (CM-COT) synchronous buck regulator with integrated high-side and low-side power MOSFETs. Its power stage is capable of supplying 5 A (3 A for the SiP12107) continuous current at 4 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.6 V from a 2.8 V to 5.5 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiP12107/SiP12108's CM-COT architecture delivers ultra-fast transient response with minimum output capacitance and tight ripple regulation at very light load. The part is stable with any capacitor type and no ESR network is required for loop stability. The device also incorporates a power saving scheme that significantly increases light load efficiency. The SiP12107/SiP12108 integrates a full protection feature set, including output overvoltage protection (OVP), output undervoltage protection (UVP) and thermal shutdown (OTP). The “A” version of the 5 A device, the SiP12108A, does not have the UVP feature. The devices also incorporate UVLO for the input rail and an internal soft-start ramp.

The SiP12107/SiP12108/SiP12108A are available in a lead (Pb)-free power enhanced 3 mm x 3 mm QFN-16 package.

FEATURES

- 2.8 V to 5.5 V input voltage
- Adjustable output voltage down to 0.6 V
- 3 A continuous output current for SiP12107
- 5 A continuous output current for SiP12108A
- Programmable switching frequency up to 4 MHz
- 95 % peak efficiency
- Stable with any capacitor. No external ESR network required
- Ultrafast transient response
- Selectable power saving (PSM) mode or forced continuous mode
- ± 1 % accuracy of V_{OUT} setting
- Pulse-by-pulse current limit
- SiP12107 / SiP12108 is fully protected with OTP, SCP, UVP, OVP
- SiP12108A is fully protected with OTP, SCP, OVP
- PGOOD indicator
- PowerCAD simulation software available at www.vishay.transim.com/login.aspx
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

Point of load regulation for low-power processors, network processors, DSPs, FPGAs, and ASICs

- Low voltage, distributed power architectures with 3.3 V or 5 V rails
- Computing, broadband, networking, LAN/WAN, optical, test and measurement
- A/V, high density cards, storage, DSL, STB, DVR, DTV, Industrial PC

ORDERING INFORMATION	
DEMO BOARD PART NUMBER	MAX. OUTPUT CURRENT
SiP12107DB	3 A
SiP12108DB	5 A

POWER UP PROCEDURE

This reference board allows the end user to evaluate the SiP12107/SiP12108 chip for its features and all functionalities. It can also be a reference design for a user's application.

To turn-on the reference board, apply a voltage between 2.8 V and 5.5 V to V_{IN} and EN pins, the board will come up in PWM mode with an output voltage preset to 1.8 V. To disable the part, tie the EN pin to GND. To set the part into power save mode, tie the AUTO pin to GND. This will allow much higher efficiency due to a very lower switching frequency at very light loads. As the load increases the frequency will increase until the nominal set frequency (preset to ~1 MHz) is reached. P_{GOOD} indicator can be probed from P_{GOOD} pin.

SPECIFICATION

Input voltage : 2.8 V to 5.5 V
Output voltage: 0.6 V to 3.3 V

Output current: 0 A to 3 A for SiP12107, and 0 A to 5 A for SiP12108/SiP12108A

CONNECTION AND SIGNAL/TEST POINTS

Power Test Points

V_{IN} (J1), **GND (J4)**: Input voltage source with **V_{IN}** to be positive. Connect to a 2.8 V to 5.5 V source that powers SiP12107/SiP12108.

V_{OUT} (J2), **GND (J3)**: Output voltage with **V_{OUT}** to be positive. Connect to a load that draws less than the max. current of the part.

Signal and test leads

MODE (J5) Connecting this pin to GND enables power save mode at very light loads.

PGOOD (J6) This flag will go HI once FB pin threshold voltage is reached or V_{OUT} reaches regulation.

EN (J7) Connecting this pin to V_{IN} enables the part and to GND disables the part

COMMON ADJUSTMENTS MADE TO THE REFERENCE BOARD

OUTPUT VOLTAGE ADJUSTMENT

The reference board is configured for a 1.8 V output. If a different output voltage is needed, simply change the value of Vout and solve for R7 based on the following formula:

$$R7 = R6 \times \frac{V_{REF}}{V_{OUT\ max.} - V_{REF}} = 5.11K \times \frac{0.6\ V}{1.8\ V - 0.6\ V} = 2.55K$$

CHANGING SWITCHING FREQUENCY

The following equation illustrates the relationship between ON-time, V_{IN}, V_{OUT} and R_{ON} value:

$$t_{ON} = R_{ON} \times K \times \frac{V_{OUT}}{V_{IN}}$$

where K is a constant set internally ($K = 10.45 \times 10^{-12}$).

Once ON time is set, pseudo constant frequency is then determined by the following equation:

$$F_{sw} = \frac{D}{t_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{\frac{V_{OUT}}{V_{IN}} \times R_{ON} \times K} = \frac{1}{R_{ON} \times K}$$

OUTPUT RIPPLE VOLTAGE

Output ripple voltage can be measured across J2 and J3, but it is better to use a tip and barrel measurement since the ripple will be very small. Typically output ripple voltage is set to 3 % to 5 % of the output voltage, with an all ceramic output solution the output ripple can be very small. Voltage mode based COT controllers will have stability issues with an all ceramic solution, because they require the ripple voltage to provide the ramp needed by the controller. This is not a problem for the SiP12107/SiP12108 which are current mode COT controllers. The SiP12107/SiP12108 can work with any type of output capacitors that suit your needs.

INPUT CAPACITORS

The input capacitors are chosen as a combination of bulk and ceramic capacitors, to satisfy cost, RMS current, ESR, input voltage ripple requirements and a source for instantaneous energy and filtering that the converter may require.

INDUCTOR SELECTION

Knowing V_{IN}, V_{OUT}, F_{sw}, full load current and choosing a ripple current (•I) percentage that's between 20 % to 50 % of full load current, we can calculate an inductor value. For SiP12108, the max I_{OUT} is 5 A.

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{F_{sw} \times V_{IN} \times \Delta I \times I_{OUT\ max.}}$$

$$= (3.3\ V - 1.8\ V) \times \frac{1.8\ V}{1 \times 10^6 \times 5\ V \times 0.25 \times 5\ A} = 1.066\ \mu H$$

INDUCTORS

Other than the inductance the DCR and saturation current parameters are key values. The DCR causes an I^2R loss which will decrease the system efficiency and generate heat. The saturation current has to be higher than the maximum output current plus 1/2 the ripple current. In over current condition the inductor current may be very high. All

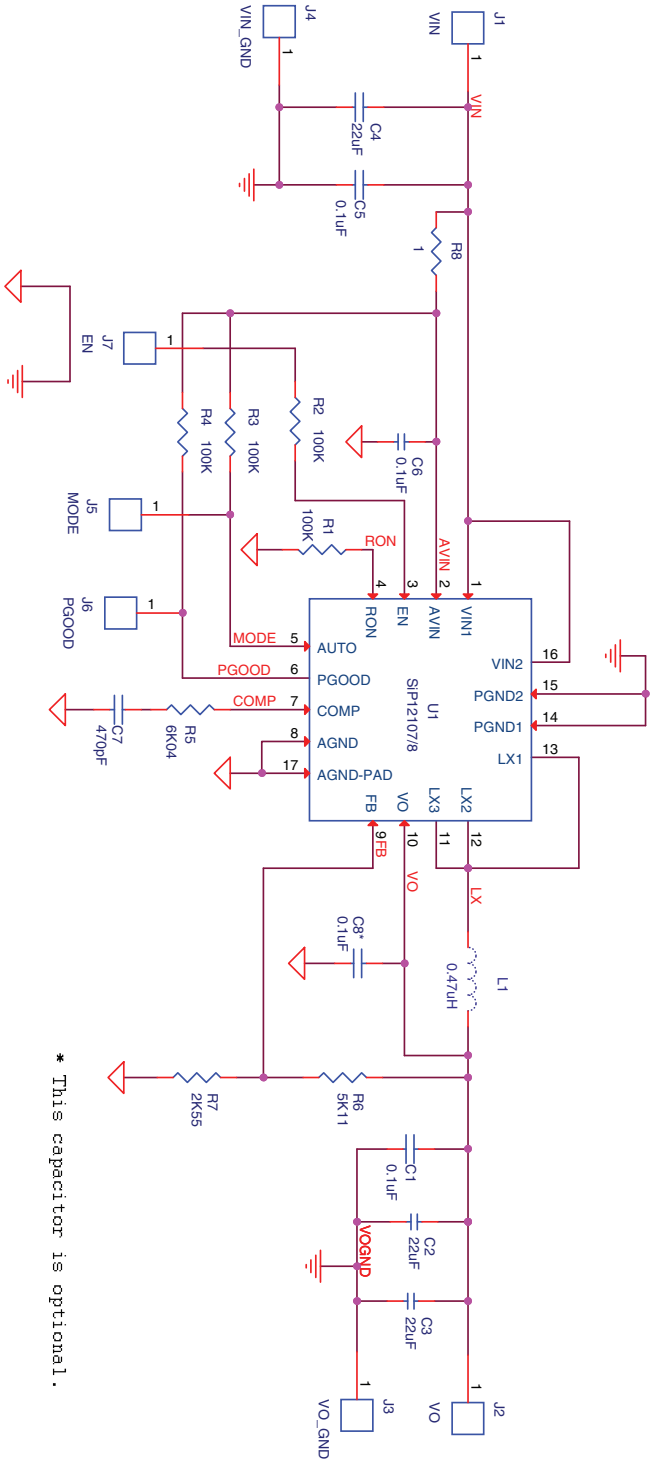
this needs to be considered when selecting the inductor.

On this board Vishay IHLP1616 series inductors are used to achieve a compact yet efficient design. This family of inductors utilize a material that has incredible saturation levels compared to competing products.

OUTPUT CAPACITORS

Ceramics capacitors were chosen to show the advantages the SiP12107/SiP12108 current mode constant on time controllers have over the voltage mode controllers which require a minimum output ripple voltage in order to operate stably.

SCHEMATIC OF DEMO BOARD



BILL of MATERIAL						
ITEM	QTY	REFERENCE	FOOTPRINT	COMP_VALUE	PART NUMBER	MANUFACTURER
1	2	C1, C5	C0402	10 V/0.1 µF	VJ0402Y104MXQCW1BC	Vishay
2	1	C7	C0402	50 V/470 pF	VJ0402A471JXACW1BC	Vishay
3	1	C6	C0603	16 V/0.1 µF	GRM188R71C104KA01D	Murata
4	1	C8	C0603	DNP	-	-
5	3	C2, C3, C4	C0805	10 V/22 µF	LMK212BJ226MG-T	Taiyo Yuden
6	1	L1	IHLP1616	1 µH	IHLP1616BZER1ROM11	Vishay
7	1	U1	MLP33-16	SiP12107, SiP12108	SiP12107, SiP12108	Vishay
8	4	R1, R2, R3, R4	R0402	100K	CRCW0402100KFKED	Vishay
9	1	R5	R0402	6K04	TNPW04026K04BETD	Vishay
10	1	R6	R0402	5K11	CRCW04025K11FKED	Vishay
11	1	R7	R0402	2K55	TNPW04022K55BETD	Vishay
12	6	J1, J2, J3, J4, J5, J6	TP30	Test Pin	5002K-ND	-

REFERENCE BOARD PCB LAYOUT

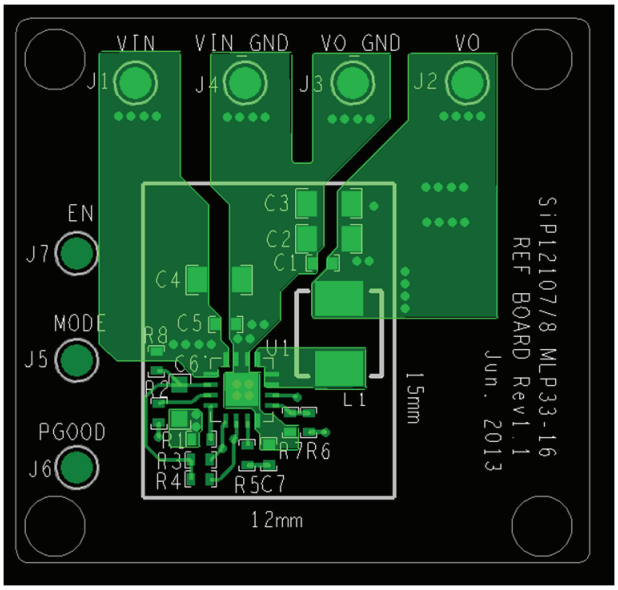


Fig. 1 - Top of the PCB

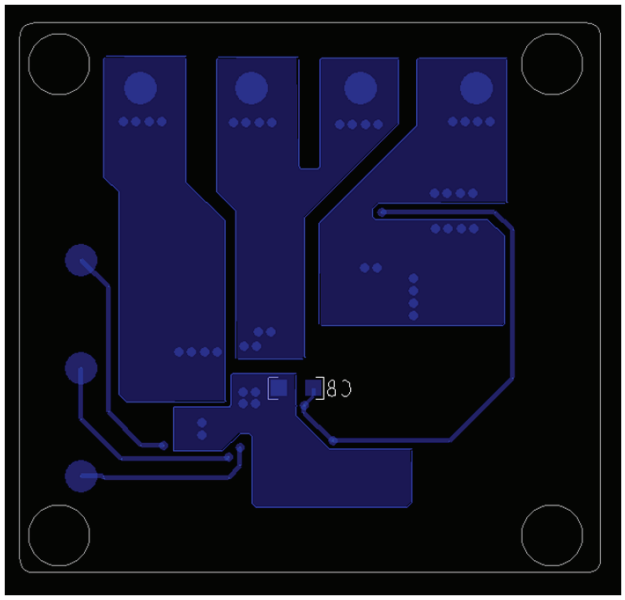


Fig. 2 - Bottom of the PCB

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