

4.70 mm (0.180") 8-Character 5x7 Dot Matrix Alphanumeric Programmable Display™

Lead (Pb) Free Product - RoHS Compliant

| | |
|------------------------------|-----------------|
| Red | PDSP1880 |
| Yellow | PDSP1881 |
| High Efficiency Red | PDSP1882 |
| Green | PDSP1883 |
| High Efficiency Green | PDSP1884 |



DESCRIPTION

The PDSP1880 (Red), PDSP1881 (Yellow), PDSP1882 (High Efficiency Red), PDSP1883 (Green), and PDSP1884 (High Efficiency Green) are eight digit, 5 x 7 dot matrix, alphanumeric Programmable Displays. The 4.70 mm (0.180") high digits are packaged in a rugged, high quality, optically transparent, 7.62 mm (0.300") lead spacing, 30 pin plastic DIP.

The on-board CMOS has a built-in 128 character ROM. The PDSP188X also has a user definable character (UDC) feature, which uses a RAM that permits storage of 16 arbitrary characters, symbols or icons that are software-definable by the user. The character ROM itself is mask programmable and easily modified by the manufacturer to provide specified custom characters.

The PDSP188X is designed for standard microprocessor interface techniques, and is fully TTL compatible. The Clock I/O and Clock Select pins allow the user to cascade multiple display modules.

FEATURES

- Eight 4.70 mm (0.180") Dot Matrix Characters in Red, Yellow, High Efficiency Red, Green, or High Efficiency Green
- Built-in 128 Character ROM, Mask Programmable for Custom Fonts
- Readable from 2.5 meters (8 Feet)
- Built-in Decoders, Multiplexers and Drivers
- Wide Viewing Angle, X Axis $\pm 55^\circ$, Y Axis 65°
- Programmable Features:
 - Individual Flashing Character
 - Full Display Blinking
 - Multi-Level Dimming and Blanking
 - Clear Function
 - Self Test
- Internal or External Clock
- End Stackable Dual-In-Line Plastic Package
- Read/Write Capability
- 16 User Definable Characters

ESD Warning: Standard precautions for CMOS handling should be observed.

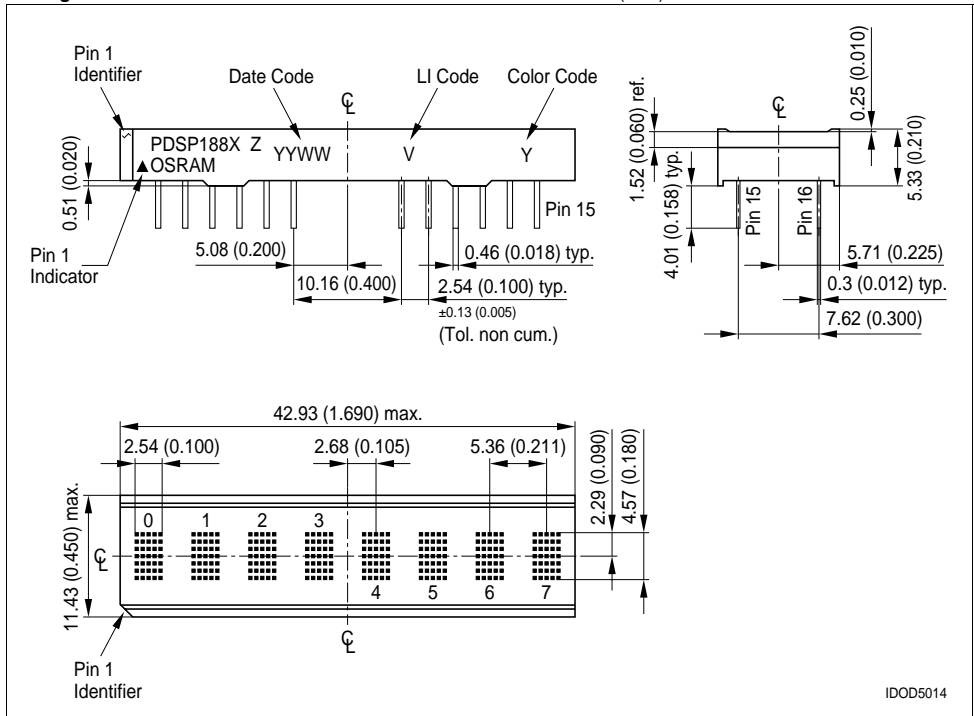
PDSP1880, PDSP1881, PDSP1882, PDSP1883, PDSP1884

Ordering Information

| Type | Color of Emission | Character Height mm (inch) | Ordering Code |
|----------|-----------------------|-------------------------------|---------------|
| PDSP1880 | red | 4.70 (0.180) | Q68000A9105 |
| PDSP1881 | yellow | | Q68000A9106 |
| PDSP1882 | high efficiency red | | Q68000A9107 |
| PDSP1883 | green | | Q68000A9108 |
| PDSP1884 | high efficiency green | | Q68000A9109 |

Package Outlines

Dimensions in mm (inch)



Maximum Ratings ($T_A=25^\circ\text{C}$)

| Parameter | Symbol | Value | Unit |
|---|-----------|------------------------|------------------|
| Operating temperature range | T_{op} | - 40 ... + 85 | $^\circ\text{C}$ |
| Storage temperature range | T_{stg} | - 55 ... + 100 | $^\circ\text{C}$ |
| DC Supply Voltage, V_{CC} to GND (max. voltage with no LEDs on) | V_{CC} | -0.3 to + 7.0 | V |
| Operating Voltage, V_{CC} to GND (max. voltage with 20 dots/digits on) | | 5.5 | V |
| Input Voltage Levels, all inputs | | -0.3 to V_{CC} + 0.3 | V |
| Solder Temperature 1.59 mm (0.063") below seating plane, $t < 5.0$ s | T_s | 260 | $^\circ\text{C}$ |
| Relative Humidity (non-condensing) | | 85 | % |
| ESD (100 pF, 1.5 k Ω) (each pin) | V_Z | 4.0 | kV |

Optical Characteristics at 25°C

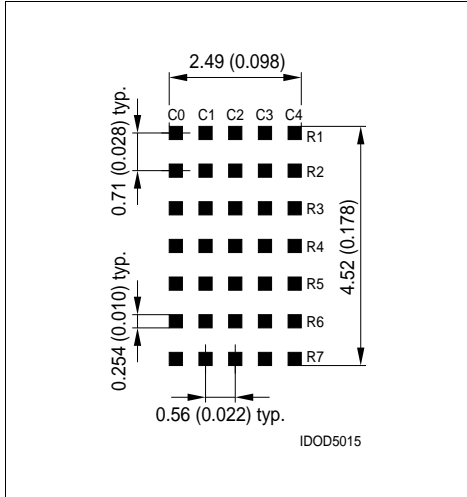
($V_{CC}=5.0$ V at 100% brightness level)

| Description | Symbol | Values | | | | | Unit |
|---|------------------|-----------------|--------------------|---------------------------------|-------------------|-----------------------------------|--|
| | | Red PDSP1880 | Yellow PDSP1881 | High Efficiency Red PDSP1882 | Green PDSP1883 | High Efficiency Green PDSP1884 | |
| Peak Luminous Intensity (min.) (typ.) | I_{peak} | 70 125 | 125 205 | 125 350 | 125 275 | 125 500 | $\mu\text{cd/dot}$ $\mu\text{cd/dot}$ |
| Peak Wavelength (typ.) | λ_{peak} | 660 | 583 | 630 | 565 | 568 | nm |
| Dominant Wavelength (typ.) | λ_{dom} | 639 | 585 | 626 | 570 | 574 | nm |

PDSP1880, PDSP1881, PDSP1882, PDSP1883, PDSP1884

Enlarged Character Format

Dimensions in mm (inch)

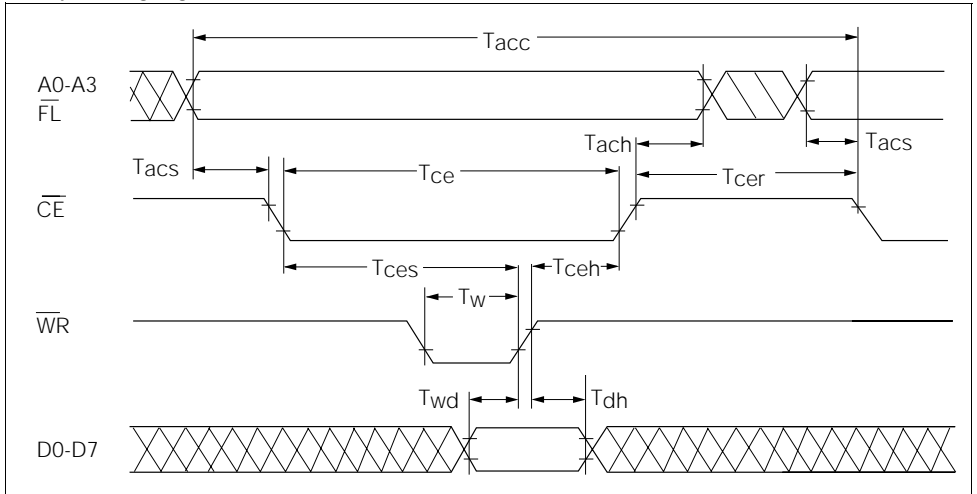


Switching Specifications

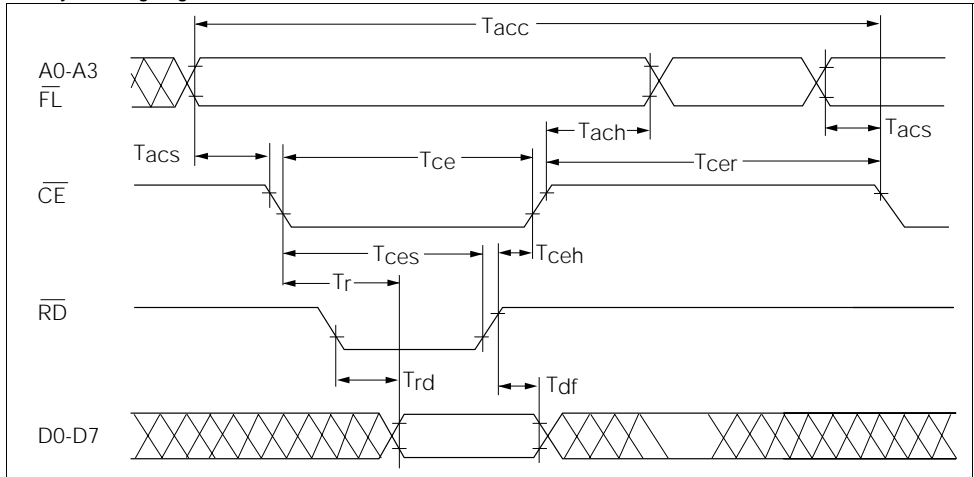
(over operating temperature range and $V_{CC}=4.5\text{ V}$)

| Symbol | Description | Min. | Units |
|-----------|--|------|-------|
| T_{acc} | Display Access Time—Write | 210 | ns |
| T_{acc} | Display Access Time—Read | 230 | ns |
| T_{acs} | Address Setup Time to \overline{CE} | 10 | ns |
| T_{ce} | Chip Enable Active Time—Write | 140 | ns |
| T_{ce} | Chip Enable Active Time—Read | 160 | ns |
| T_{ach} | Address Hold Time to \overline{CE} | 20 | ns |
| T_{cer} | Chip Enable Recovery Time | 60 | ns |
| T_{ces} | Chip Enable Active Prior to Rising Edge—Write | 140 | ns |
| T_{ces} | Chip Enable Active Prior to Rising Edge—Read | 160 | ns |
| T_{ceh} | Chip Enable Hold to Rising Edge of Read/Write Signal | 0 | ns |
| T_w | Write Active Time | 100 | ns |
| T_{wd} | Data Valid Prior to Rising Edge of Write Signal | 50 | ns |
| T_{dh} | Data Write Time | 20 | ns |
| T_r | Chip Enable Active Prior to Valid Data | 160 | ns |
| T_{td} | Read Active Prior to Valid Data | 95 | ns |
| T_{df} | Read Data Float Delay | 10 | ns |
| T_{rc} | Reset Active Time | 300 | ns |

Write Cycle Timing Diagram



Read Cycle Timing Diagram



Character Set

| ASCII CODE | | D0 | L | H | L | H | L | H | L | H | L | H | L | H | L | H | L | H | | |
|------------|----|----|----|-----|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|
| D1 | D2 | L | L | L | H | H | L | L | H | H | L | L | H | H | L | L | H | H | | |
| D3 | D4 | L | L | L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | | |
| D7 | D6 | D5 | D4 | HEX | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| L | L | L | L | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| L | L | L | H | 1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| L | L | H | L | 2 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| L | L | H | H | 3 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| L | H | L | L | 4 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| L | H | L | H | 5 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| L | H | H | L | 6 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| L | H | H | H | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| H | X | X | X | 8 | UDC 0 | UDC 1 | UDC 2 | UDC 3 | UDC 4 | UDC 5 | UDC 6 | UDC 7 | UDC 8 | UDC 9 | UDC 10 | UDC 11 | UDC 12 | UDC 13 | UDC 14 | UDC 15 |

IDCS5086

Notes:

1. Upon power up, the device will initialize in a random state.
2. X=don't care.

DC Electrical Characteristics at 25°C

| Parameters | Limits | | | | Conditions |
|---|-------------|-------|------------------|-------|--|
| | Min. | Typ. | Max. | Units | |
| V_{CC} | 4.5 | 5.0 | 5.5 | V | — |
| I_{CC} Blank | — | 0.65 | 1.0 | mA | $V_{CC}=5.0\text{ V}$, $V_{IN}=5.0\text{ V}$ |
| I_{CC} 12 dots/digit on ^{1) 2)} | — | 200 | 255 | mA | $V_{CC}=5.0\text{ V}$, "V" in all 8 digits |
| I_{CC} 20 dots/digit on ^{1) 2)} | — | 300 | 370 | mA | $V_{CC}=5.0\text{ V}$, "#" in all 8 digits |
| I_{ILP} (with pull-up) Input Leakage | -18 | -11 | -5.0 | μA | $V_{CC}=5.0\text{ V}$, $V_{IN}=0\text{ V}$ to V_{CC} (WR, CE, FL, RST, RD, CLKSEL) |
| I_{IL} (no pull-up) Input Leakage | -1.0 | — | +1.0 | μA | $V_{CC}=5.0\text{ V}$, $V_{IN}=5.0\text{ V}$ (CLK, A0–A3, D0–D7) |
| V_{IH} Input Voltage High | 2.0 | — | V_{CC} +0.3 | V | $V_{CC}=4.5\text{ V}$ to 5.5 V |
| V_{IL} Input Voltage Low | GND -0.3 | — | — | V | $V_{CC}=4.5\text{ V}$ to 5.5 V |
| V_{OL} (D0–D7), Output Voltage Low | — | — | 0.4 | V | $V_{CC}=4.5\text{ V}$, $I_{OL}=1.6\text{ mA}$ |
| V_{OL} (CLK), Output Voltage Low | — | — | 0.4 | V | $V_{CC}=4.5\text{ V}$, $I_{OL}=40\text{ μA}$ |
| V_{OH} Output Voltage High | 2.4 | — | — | V | $V_{CC}=4.5\text{ V}$, $I_{OH}=40\text{ μA}$ |
| θ_{JC} Thermal Resistance, Junction to Case | — | 25 | — | °C/W | — |
| Clock I/O Frequency | 28 | 57.34 | 81.14 | kHz | $V_{CC}=4.5$ to 5.5 V |
| FM, Digit Multiplex Frequency | 125 | 256 | 362.5 | Hz | $V_{CC}=4.5$ to 5.5 V |
| Blinking Rate | 0.98 | 2.0 | 2.83 | Hz | — |
| Clock I/O Buss Loading | — | — | 2.40 | pF | — |
| Clock Out Rise Time | — | — | 500 | nsec | $V_{CC}=4.5\text{ V}$, $V_{OH}=2.4\text{ V}$ |
| Clock Out Fall Time | — | — | 500 | nsec | $V_{CC}=4.5\text{ V}$, $V_{OH}=0.4\text{ V}$ |

Notes:

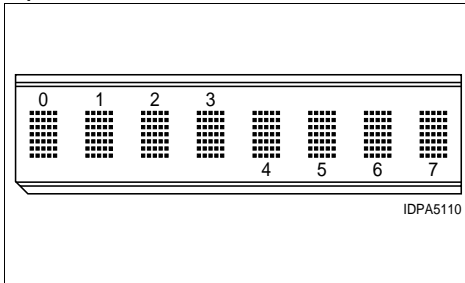
¹⁾ I_{CC} is an average value.

²⁾ I_{CC} is measured with the display at full brightness. Peak $I_{CC}=^{28}I_{15}$ I_{CC} average (#displayed).

Recommended Operating Conditions ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Min. | Max. | Units |
|---------------------|----------|------|------|-------|
| Supply Voltage | V_{CC} | 4.5 | 5.5 | V |
| Input Voltage Low | V_{IL} | — | 0.8 | V |
| Input Voltage High | V_{IH} | 2.0 | — | V |
| Output Voltage Low | V_{OL} | — | 0.4 | V |
| Output Voltage High | V_{OH} | 2.4 | — | V |

Top View



Pin Assignments

| Pin # | Name | Symbol | Definition |
|-------|----------------|--------------------|---|
| 16 | Supply ground | GND _{sup} | Analog ground for LED drivers |
| 17 | — | NC | No connection |
| 18 | Logic ground | GND _{log} | Logic ground for digital circuitry |
| 19 | Read | \overline{RD} | Reads data from display when $\overline{RD}=0$. Also $\overline{CE}=0$. |
| 20 | Data bit zero | D0 | Least significant data bit. |
| 21 | Data bit one | D1 | Second data bit. |
| 22–24 | No pins | — | No connections |
| 25 | Data bit two | D2 | Third data bit. |
| 26 | Data bit three | D3 | Fourth data bit. |
| 27 | Data bit four | D4 | Fifth data bit. |
| 28 | Data bit five | D5 | Sixth data bit. |
| 29 | Data bit six | D6 | Seventh data bit. |
| 30 | Data bit seven | D7 | Most significant data bit. |

Pin Assignments

| Pin # | Name | Symbol | Definition |
|-------|-----------------|------------------|--|
| 1 | Reset | \overline{RST} | Initializes display; clears Character RAM (20H), Flash RAM (00H), control word (00H), and resets internal counters. UDC Address Register and UDC RAM unaffected. |
| 2 | Flash | \overline{FL} | Accesses Flash RAM. Address inputs A0–A2 select digit address while data bit D0 sets (D0=1) or resets (D0=0) Flash bit, A3 and A4 ignored. |
| 3 | Address input | A0 | A0–A2 select specific digits. See Table „Memory Selection“ (page 9). |
| 4 | | A1 | Same as A0 |
| 5 | | A2 | Same as A0 |
| 6 | Address input | A3 | A3 and A4 access parts of memory together with Flash pin. See Table 1. |
| 7–9 | No pins | — | No connections |
| 10 | Address input | A4 | Same as A3 |
| 11 | Clock Select | CLS | Selects internal or external clock source. CLS=1 selects internal clock (master), CLS=0 selects external clock (slave operation). |
| 12 | Clock In/Out | CLK | Inputs or outputs clock as determined by CLS. |
| 13 | Write | \overline{WR} | Writes data into display when $\overline{WR}=0$. Note $\overline{CE}=0$ to enable write cycle. |
| 14 | Chip Enable | \overline{CE} | Enables display's write and read cycles when $\overline{CE}=0$. |
| 15 | Positive supply | V _{CC} | Positive power supply input. |

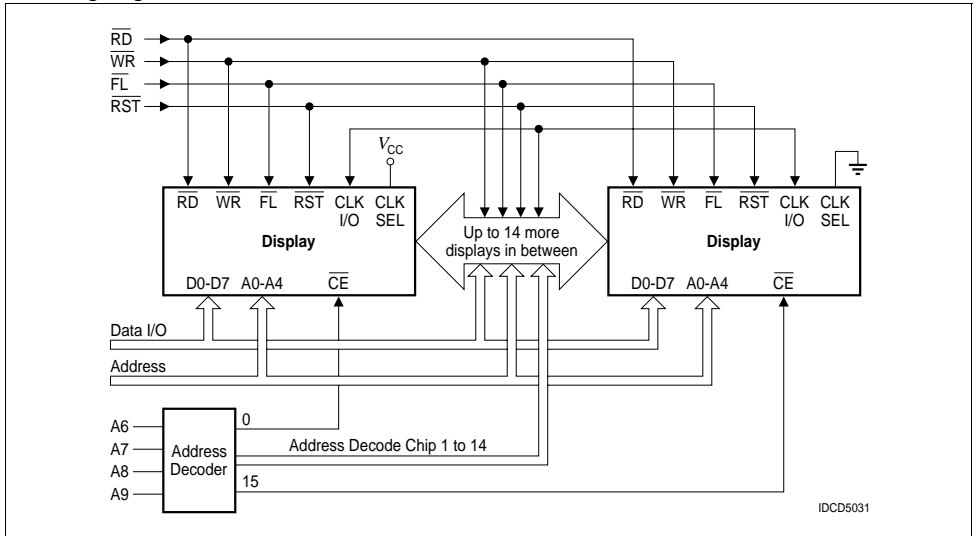
Cascading Displays

The PDSP188X is designed to drive up to 16 other PDSP188Xs with input loading of 15 pF each.

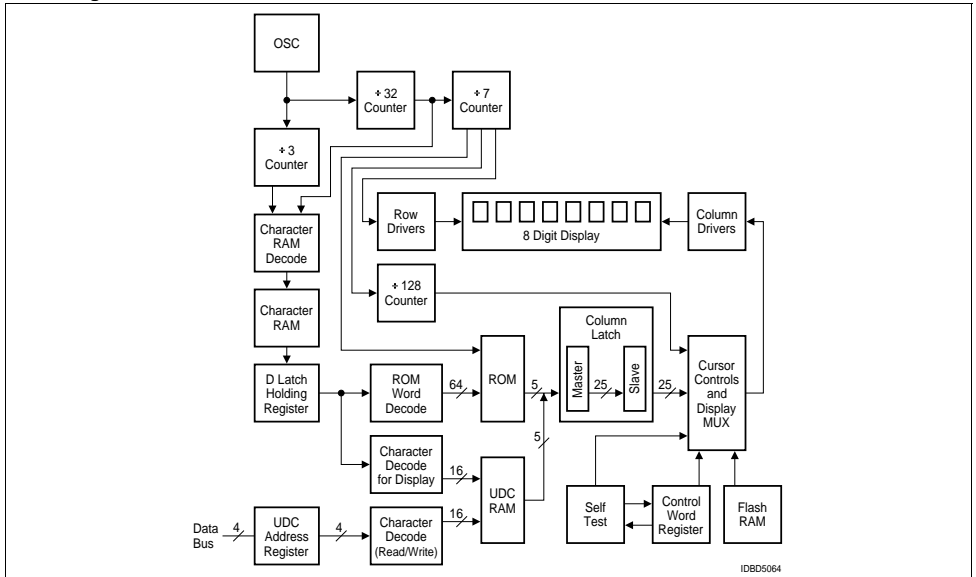
General requirements for cascading 16 displays together:

- Determine the correct address for each display.
- Use \overline{CE} from an address decoder to select the correct display.
- Use \overline{CE} from an address decoder to select the correct display.
- Select one of the Displays to provide the Clock for the other displays. Connect CLKSEL to V_{CC} for this display.
- Tie \overline{CLKSEL} to ground on other displays.
- Use \overline{RST} to synchronize the blinking between the displays.

Cascading Diagram



Block Diagram



Functional Description

The display's user interface is organized into five memory areas. They are accessed using the Flash Input, \overline{FL} , and address lines, A3 and A4. All the listed RAMs and Registers may be read or written through the data bus. See Table „Memory Selection“ (page 9). Each input pin is described in Pin Definitions.

Five Basic Memory Areas

| | |
|--|---|
| Character RAM | Stores either ASCII (Katakana) character data or an UDC RAM address |
| Flash RAM | 1 x 8 RAM which stores Flash data |
| User-Defined Character RAM (UDC RAM) | Stores dot pattern for custom characters |
| User-Defined Address Register (UDC Address Register) | Provides address to UDC RAM when user is writing or reading custom character |
| Control Word Register | Enables adjustment of display brightness, flash individual characters, blink, self test or clearing the display |

\overline{RST} can be used to initialize display operation upon power up or during normal operation. When activated, \overline{RST} will clear the Flash RAM and Control Word Register (00H) and reset the internal counter. All eight display memory locations will be set to 20H to show blanks in all digits.

\overline{FL} pin enables access to the **Flash RAM**. The **Flash RAM** will set (D0=1) or reset (D0=0) flashing of the character addressed by A0–A2.

The 1 x 8 bit **Control Word Register** is loaded with attribute data if A3=0.

The **Control Word Logic** decodes attribute data for proper implementation.

Character ROM is designed for 128 ASCII characters. The ROM is Mask Programmable for custom fonts.

The **Clock Source** could either be the internal oscillator ($\overline{CLKSEL}=1$) of the device or an external clock ($\overline{CLKSEL}=0$) could be an input from another HDSP211X display for synchronizing blinking for multiple displays.

The **Display Multiplexer** controls the Row Drivers so no additional logic is required for a display system.

The **Display** has eight digits. Each digit has 35 LEDs.

Theory of Operation

The PDSP188X Display is designed to work with all major microprocessors. Data entry is via an eight bit parallel bus. Three bits of address route the data to the proper digit location in the RAM. Standard control signals like \overline{WR} and \overline{CE} allow the data to be written into the display.

D0–D7 data bits are used for both Character RAM and control word data input. A3 acts as the mode selector. If A3=1, character RAM is selected. Then input data bit D7 will determine whether input data bits D0–D6 is ASCII coded data (D7=0) or UDC data (D7=1). See section on „UDC Address Register and UDC RAM“ (page 10).

For normal operation \overline{FL} pin should be held high. When \overline{FL} is held low, Flash RAM is accessed to set character blinking.

The seven bit ASCII code is decoded by the Character ROM to generate Column data. Twenty columns worth of data is sent out each display cycle, and it takes fourteen display cycles to write into eight digits.

The rows are multiplexed in two sets of seven rows each. The internal timing and control logic synchronizes the turning on of rows and presentation of column data to assure proper display operation.

Power Up Sequence

Upon power up the display will come on at random. Thus the display should be reset on power-up. Reset will clear the Flash RAM, Control Word Register and reset the internal counter. All the digits will show blanks and display brightness level will be 100%.

The display must not be accessed until three clock pulses (110 μ s minimum using the internal clock) after the rising edge of the reset line.

Microprocessor Interface

The interface to a microprocessor is through the 8-bit data bus (D0–D7), the 4-bit address bus (A0–A3) and control lines \overline{FL} , \overline{CE} and \overline{WR} .

To write data (ASCII/Control Word) into the display \overline{CE} should be held low, address and data signals stable and \overline{WR} should be brought low. The data is written on the low to high transition of \overline{WR} .

The Control Word is decoded by the Control Word Decode Logic. Each code has a different function. The code for display brightness changes the duty cycle for the column drivers. The peak LED current stays the same but the average LED current diminishes depending on the intensity level.

The character Flash Enable causes 2.0 Hz coming out of the counter to be ANDED with the column drive signal to make the column driver cycle at 2.0 Hz. Thus the character flashes at 2.0 Hz.

Memory Selection

| \overline{FL} | A4 | A3 | Section of Memory | A2–A0 | Data Bits Used |
|-----------------|----|----|-----------------------|-------------------|----------------|
| 0 | X | X | Flash RAM | Character Address | D0 |
| 1 | 0 | 0 | UDC Address Register | Don't Care | D3–D0 |
| 1 | 0 | 1 | UDC RAM | Row Address | D4–D0 |
| 1 | 1 | 1 | Character RAM | Character Address | D7–D0 |
| 1 | 1 | 0 | Control Word Register | Don't Care | D7–D0 |

The display Blink works the same way as the Flash Enable but causes all twenty column drivers to cycle at 2.0 Hz thereby making all eight digits blink at 2.0 Hz.

The Self Test function of the IC consists of two internal routines which exercise major portions of the IC and illuminates all the LEDs.

Clear bit clears the character RAM and writes a blank into the display memory. It however does not clear the control word.

ASCII Data or Control Word Data can be written into the display at this point. For multiple display operation, CLK I/O must be properly selected. CLK I/O will output the internal clock if CLKSEL=1, or will allow input from an external clock if CLKSEL=0.

Character RAM

The Character RAM is selected when \overline{FL} , A4 and A3 are set to 1,1,1 during a read or write cycle. The Character RAM is a 8 by 8 bit RAM with each of the eight locations corresponding to a digit on the display. Digit 0 is on the left side of the display and digit 7 is on the right side of the display. Address lines, A2–A0 select the digit address with A2 being the most significant bit and A0 being the least significant bit. The two types of data stored in the Character RAM are the ASCII coded data and the UDC Address Data. The type of data stored in the Character RAM is determined by data bit, D7. If D7 is low, then ASCII coded data is stored in data bits D6–D0. If D7 is high, then UDC Address Data is stored in data bit D3–D0.

The ASCII coded data is a 7 bit code used to select one of 128 ASCII characters permanently stored in the ASCII ROM.

The UDC Address data is a 4 bit code used to select one of the UDC characters in the UDC RAM. There are up to 16 characters available. See Table „Character RAM Access Logic“ (page 10).

UDC Address Register and UDC RAM

The UDC Address Register and UDC RAM allows the user to generate and store up to 16 custom characters. Each custom character is defined in 5 x 7 dot matrix pattern. It takes 8 write cycles to define a custom character, one cycle to load the UDC Address Register and 7 cycles to define the character. The contents of the UDC Address Register will store the 4 bit address for one of the 16 UDC RAM locations. The UDC RAM is used to store the custom character.

UDC Address Register

The UDC Address Register is selected by setting \overline{FL} =1, A4=0, A3=0. It is a 4 bit register and uses data bits, D3–D0 to store the 4 bit address code (D7–D4 are ignored). The address code selects one of 16 UDC RAM locations for custom character generation.

UDC RAM

The UDC RAM is selected by setting \overline{FL} =1, A4=0, A3=1. The RAM is comprised of a 7 x 5 bit RAM. As shown in Table „UDC Character Map“ (page 11), address lines, A2-A0 select one of the 7 rows of the custom character. Data bits, D4-D0 determine the 5 bits of column data in each row. Each data bit corresponds to a LED. If the data bit is high, then the LED is on. If the data bit is low, the LED is off. To create a character, each of the 7 rows of column data need to be defined. See Table „UDC Address Register and UDC RAM“ (page 10) for logic.

Character RAM Access Logic

| RST | CE | WR | RD | FL | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|----|----|----|----|----|----|----------------------------------|----|----|---|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | Character Address for Digits 0–7 | | | 0 7 bit ASCII code for a Write Cycle | | | | | | | |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | Character Address for Digits 0–7 | | | 0 7 bit ASCII code read during a Read Cycle | | | | | | | |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | Character Address for Digits 0–7 | | | 1 D3–D0=UDC address for a Write Cycle | | | | | | | |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | Character Address for Digits 0–7 | | | 1 D3–D0=UDC address for Read Data | | | | | | | |

UDC Address Register and UDC Character RAM

| RST | CE | WR | RD | FL | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|-----|----|----|----|----|----|----|-----------------------------------|----|----|--|----|----|----|----|----|----|----|----------------------|
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | Not used for UDC Address Register | | | D3–D0=UDC RAM Address Code for Write Cycle | | | | | | | | UDC Address Register |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | Not used for UDC Address Register | | | D3–D0=UDC RAM Address Code for Read Cycle | | | | | | | | |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | A2–A0=Character Row Address | | | D4–D0=Character Column Data for Write Cycle | | | | | | | | UDC RAM |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | A2–A0=Character Row Address | | | D4–D0=Character Column Data read during a Read Cycle | | | | | | | | |

Flash RAM

The Flash RAM allows the display to flash one or more of the characters being displayed. The Flash Ram is accessed by setting FL low. A4 and A3 are ignored. The Flash RAM is a 8 x 1 bit RAM with each bit corresponding to a digit address. Digit 0 is on the left side of the display and digit 7 is on the right side of the display. Address lines, A2–A0 select the digit address with A2 being the most significant digit and A0 being the least significant digit. Data bit, D0, sets and resets the flash bit for each digit. When D0 is high, the flash bit is set; and when D0 is low, it is reset. See Table „Flash RAM Access Logic“ (page 11).

Control Word

The Control Word is used to set up the attributes required by the user. It is addressed by setting FL=1, A4=1, A3=0. The Control Word is an 8 bit register and is accessed using data bits, D7–D0. See Table „Control Word Access Logic“ (page 11) and Figure „Control Word Data Definition“ (page 12) for the logic and attributed control. The Control Word has 5 functions. They are brightness control, flashing character enable, blinking character enable, self test, and clear (Flash and Character RAMS only).

Brightness Control

Control Word bits, D2–D0, control the brightness of the display with a binary code of 000 being 100% brightness and 111 being display blank. See Figure „Control Word Data Definition“ (page 12) for brightness level versus binary code. The average I_{CC} can be calculated by multiplying the 100% brightness level I_{CC} value by the display's brightness level. For example, a display set to 80% brightness with a 100% average I_{CC} value of 200 mA will have an average I_{CC} value of 200 mA x 80%=160 mA.

Flash Function

Control Word bit, D3, enables or disables the Flash Function. When D3 is 1, the Flash Function is enabled and any digit with its corresponding bit set in the Flash RAM will flash at approximately 2.0 Hz. When using an external clock, the flash rate can be determined by dividing the clock rate by 28,672. When D3 is 0, the Flash Function is disabled and the contents of the Flash RAM is ignored. For synchronized flashing on multiple displays, see the Reset Section (page 12).

Flash RAM Access Logic

| RST | CE | WR | RD | FL | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|----|----|----|----|----|----|----------------------------------|----|----|---|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 1 | 0 | X | X | Flash RAM Address for Digits 0–7 | | | D0=Flash Data, 0=Flash Off and 1=Flash On (Write Cycle) | | | | | | | |
| 1 | 0 | 1 | 0 | 0 | X | X | Flash RAM Address for Digits 0–7 | | | D0=Flash Data, 0=Flash Off and 1=Flash On (Read Cycle) | | | | | | | |

Control Word Access Logic

| RST | CE | WR | RD | FL | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|----|----|----|----|----|----|---------------------------|----|----|--|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | Not used for Control Word | | | Control Word data for a Write Cycle, see Figure „Control Word Data Definition“ (page 12) | | | | | | | |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | Not used for Control Word | | | Control Word data for a Read during a Read Cycle | | | | | | | |

Blink Function

Control Word bit, D4, enables or disables the Blink Function. When D4 is 1, the Blink Function is enabled and all characters on the display will blink at approximately 2.0 Hz. The Blink Function will override the Flash Function if both functions are enabled. When D4 is 0, the Blink Function is disabled. When using an external clock, the blink rate can be determined by dividing the clock rate by 28,672. For synchronized blinking on multiple displays, see the Reset Section (page 12).

UDC Character Map

| Row Data | | | | Column Data | | | | |
|----------|----|----|-------|--------------------------------|----|----|----|----|
| A2 | A1 | A0 | Row # | C1 | C2 | C3 | C4 | C5 |
| | | | | D4 | D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | 1 | 5 x 7 Dot Matrix Pattern | | | | |
| 0 | 0 | 1 | 2 | | | | | |
| 0 | 1 | 0 | 3 | | | | | |
| 0 | 1 | 1 | 4 | | | | | |
| 1 | 0 | 0 | 5 | | | | | |
| 1 | 0 | 1 | 6 | | | | | |
| 1 | 1 | 0 | 7 | | | | | |

Self Test

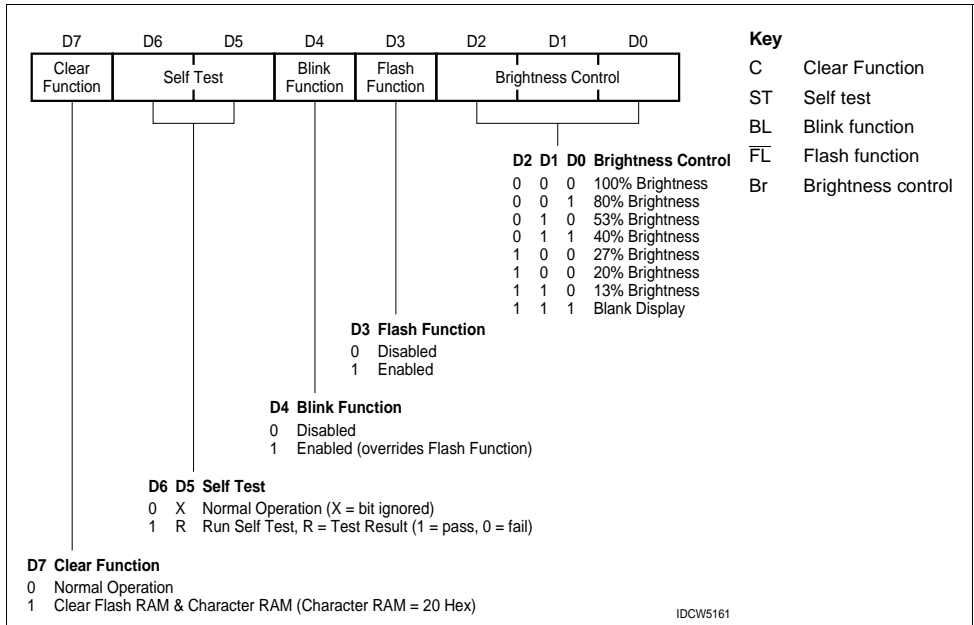
Control Word bits, D6 and D5, are used for the Self Test Function. When D6 is 1, the Self Test is initiated. Results of the Self Test are stored in bit D5. Control Word bit, D5, is a read only bit. When D5 is 1, Self Test has passed. When D5 is 0, Self Test failed is indicated. The Self Test function of the IC consists of two internal routines which exercise major portions of the IC and illuminates all of the LEDs. The first routine cycles the ASCII decoder ROM through all states and performs a check sum on the out-put. If the check sum is correct, D5 is set to a 1 (Pass).

The second routine provides a visual test of the LEDs. This is accomplished by writing checkered and inversed checkered patterns to the display. Each pattern is displayed for approximately 2.0 sec. During the self test function the display must not be accessed. The time needed to execute the self test function is calculated by multiplying the clock time by 262,144 (typical time ≈ 4.6 s). At the end of the self test, the Character RAM is loaded with blanks; the Control Word Register is set to zeroes except D5; the Flash RAM is cleared and the UDC Address Register is set to all 1.0 sec.

Clear Function (see Figure „Control Word Data Definition“ (page 12) and Table „Clear Function“ (page 12))

Control Word bit, D7 clears the character RAM to 20 hex and the flash RAM to all zeroes. The RAMs are cleared within three clock cycles (110 μs minimum, using the internal clock) when D7 is set to 1. During the clear time the display must not be accessed. When the clear function is finished, bit 7 of the Control Word RAM will be reset to a "0".

Control Word Data Definition



Clear Function

| CE | WR | FL | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|
| 0 | 0 | 1 | 0 | X | X | X | 0 | X | X | X | X | X | X | X | Clear disabled Clear user RAM, flash RAM and display |
| 0 | 0 | 1 | 0 | X | X | X | 1 | X | X | X | X | X | X | X | |

X=don't care

PDSP1880, PDSP1881, PDSP1882, PDSP1883, PDSP1884

Display Cycle Using Built-in ROM Example

Display message "Showtime." Digit 0 is leftmost—closest to pin 1.

Logic levels: 0=Low, 1=High, X=Don't care.

| RST | CE | WR | RD | FL | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation | Display |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|-----------|
| 0 | X | 1 | 1 | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X | Reset. No Read/Write Within 3 Clock Cycles | All Blank |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | X | X | X | 0 | 0 | X | 0 | 0 | 0 | 1 | 1 | 53% Brightness Selected | All Blank |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | Write "S" to Digit 0 | S |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | Write "H" to Digit 1 | SH |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | Write "O" to Digit 2 | SHO |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | Write "W" to Digit 3 | SHOW |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | Write "T" to Digit 4 | SHOWT |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | Write "I" to Digit 5 | SHOWTI |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | Write "M" to Digit 6 | SHOWTIM |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | Write "E" to Digit 7 | SHOWTIME |

Displaying User Defined Character Example

Load character "A" into UDC-5 and then display it in digit 2.

Logic levels: 0=Low, 1=High, X=Don't care

| RST | CE | WR | RD | FL | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation | Display |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|-------------|
| 0 | X | 1 | 1 | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X | Reset. No Read/Write Within 3 Clock Cycles | All Blank |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | X | X | X | X | X | X | X | 0 | 1 | 0 | 1 | Select UDC-5 | All Blank |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | X | X | X | 0 | 1 | 1 | 1 | 0 | Write into Row 1 of UDC-5 | All Blank |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | X | X | X | 1 | 0 | 0 | 0 | 1 | Write into Row 2 of UDC-5 | All Blank |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | X | X | X | 1 | 0 | 0 | 0 | 1 | Write into Row 3 of UDC-5 | All Blank |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | X | X | X | 1 | 1 | 1 | 1 | 1 | Write into Row 4 of UDC-5 | All Blank |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | X | X | X | 1 | 0 | 0 | 0 | 1 | Write into Row 5 of UDC-5 | All Blank |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | X | X | X | 1 | 0 | 0 | 0 | 1 | Write into Row 6 of UDC-5 | All Blank |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | X | X | X | 1 | 0 | 0 | 0 | 1 | Write into Row 7 of UDC-5 | All Blank |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | X | X | X | 0 | 1 | 0 | 1 | Write UDC-5 into Digit 2 | (Digit 2) A |

Electrical and Mechanical Considerations

Voltage Transient Suppression

For best results power the display and the components that interface with the display to avoid logic inputs higher than V_{CC} . Additionally, the LEDs may cause transients in the power supply line while they change display states. The common practice is to place a parallel combination of a 0.01 μF and a 22 μF capacitor between V_{CC} and GND for all display packages.

ESD Protection

The input protection structure of the PDSP188X provides significant protection against ESD damage. It is capable of withstanding discharges greater than 4.0 kV. Take all the standard precautions normal for CMOS components. These include properly grounding personnel, tools, tables, and transport carriers that come in contact with unshielded parts. If these conditions are not, or cannot be met, keep the leads of the device shorted together or the parts in anti-static packaging.

Soldering Considerations

The PDSP188X can be hand soldered with SN63 solder using a grounded iron set to 260 °C.

Wave soldering is also possible. Use water soluble organic acid flux or resin based RMA flux.

A wave temperature of 245 °C \pm 5 °C with a dwell between 1.5 sec to 3.0 sec can be used. Exposure to the wave should not exceed temperatures above 260 °C for five seconds at 1.59 mm (0.063") below the seating plane. The packages should not be immersed in the wave.

Post Solder Cleaning Procedures

The least offensive cleaning solution is hot D.I. water (60 °C) for less than 15 minutes. Addition of mild saponifiers is acceptable. Do not use commercial dishwasher detergents.

For faster cleaning, solvents may be used. Exercise care in choosing solvents as some may chemically attack the polycarbonate package. Maximum exposure should not exceed two minutes at elevated temperatures. Acceptable solvents are TF (trichlorotrifluoroethane), and IPA.

Some major solvent manufacturers are: Allied Chemical Corporation, Specialty Chemical Division, Morristown, NJ; Baron-Blakeslee, Chicago, IL; Dow Chemical, Midland, MI; E.I. DuPont de Nemours & Co., Wilmington, DE.

For further information refer to Appnote 19 at www.osram-os.com

An alternative to soldering and cleaning the display modules is to use sockets. Naturally, 28 pin DIP sockets 7.62 mm (0.300") wide with 2.54 mm (0.100") centers work well for single displays. Multiple display assemblies are best handled by longer SIP sockets or DIP sockets when available for uniform package alignment. Socket manufacturers are Aries Electronics, Inc., Frenchtown, NJ; Garry Manufacturing, New Brunswick, NJ; Robinson-Nugent, New Albany, IN; and Samtec Electronic Hardware, New Albany, IN.

Optical Considerations

The 4.70 mm (0.180") high character of the PDSP188X gives readability up to eight feet. Proper filter selection enhances readability over this distance.

Using filters emphasizes the contrast ratio between a lit LED and the character background. This will increase the discrimination of different characters. The only limitation is cost. Take into consideration the ambient lighting environment for the best cost/benefit ratio for filters.

Incandescent (with almost no green) or fluorescent (with almost no red) lights do not have the flat spectral response of sunlight. Plastic band-pass filters are an inexpensive and effective way to strengthen contrast ratios. The PDSP1880 / PDSP1882 are red / high efficiency red displays and should be matched with a long wavelength pass filter in the 570 nm to 590 nm range. The PDSP1883 should be matched with a yellow-green band-pass filter that peaks at 565 nm. For displays of multiple colors, neutral density grey filters offer the best compromise.

Additional contrast enhancement is gained by shading the displays. Plastic band-pass filters with built-in louvers offer the next step up in contrast improvement. Plastic filters can be improved further with anti-reflective coatings to reduce glare. The trade-off is fuzzy characters. Mounting the filters close to the display reduces this effect. Take care not to overheat the plastic filter by allowing for proper air flow.

Optimal filter enhancements are gained by using circular polarized, anti-reflective, band-pass filters. The circular polarizing further enhances contrast by reducing the light that travels through the filter and reflects back off the display to less than 1%.

Several filter manufacturers supply quality filter materials. Some of them are: Panelgraphic Corporation, W. Caldwell, NJ; SGL Homa-lite, Wilmington, DE; 3M Company, Visual Products Division, St. Paul, MN; Polaroid Corporation, Polarizer Division, Cambridge, MA; Marks Polarized Corporation, Deer Park, NY; Hoya Optics, Inc., Fremont, CA.

One last note on mounting filters: recessing displays and bezel assemblies is an inexpensive way to provide a shading effect in overhead lighting situations. Several bezel manufacturers are: R.M.F. Products, Batavia, IL; Nobex Components, Griffith Plastic Corp., Burlingame, CA; Photo Chemical Products of California, Santa Monica, CA; I.E.E.-Atlas, Van Nuys, CA.

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| Page | Subjects (major changes since last revision) | Date of change |
|-------------|---|-----------------------|
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