LX1672

Multiple Output LoadSHARE™ PWM

PRODUCTION DATA SHEET

DESCRIPTION

The LX1672 is a highly integrated power supply controller IC featuring two PWM switching regulator stages with an additional onboard linear regulator driver.

The two constant frequency voltage-mode PWM phases can be easily configured as a single Bi-Phase high current output, two independently regulated outputs, or as a DDR memory I/O supply with a tracking DDR termination voltage supply. Power loss and noise, due to the ESR of the input capacitors, are minimized by operating each PWM output 180° out of phase. This architecture also minimizes capacitor requirements while maximizing regulator response.

In bi-phase operation, the high current output utilizes a patented current sharing architecture, called Forced Current Sharing†, to allow accurate current sharing without the use of expensive current sense resistors.

This patented approach also gives system designers maximum flexibility with respect to MOSFET supply. Each phase can utilize different supply voltages, for efficient use of available supplies, while programming the ratio of current pulled from each using one of three methods (see application section).

The LX1672 incorporates fully programmable soft-start sequencing capabilities. Each output can be configured to come up in any order necessary as required by the application.

The LX1672 features an additional Linear Regulator Driver output, which when coupled with an inexpensive MOSFET is capable of supplying up to 5A for I/O, memory, and other supplies surrounding today's micro-processor designs.

Each regulator voltage output is programmed via a simple voltage-divider network. The LX1672, utilizing MOSFET RDS(ON) impedance, monitors maximum current limit conditions, in each PWM phase without the use of expensive current sense resistors.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

† U.S Patents: 6,285,571,6,292,378

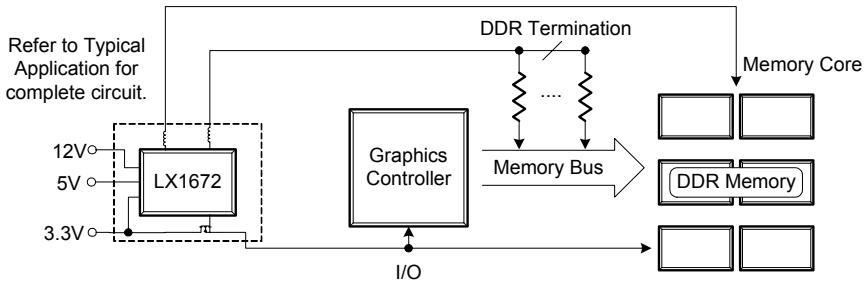
KEY FEATURES

- Up to Three Independently Regulated Outputs
- DDR Termination Compliant
- Bi-phase Current Sharing
- Outputs As Low As 0.8V Generated From An Internal 1% Reference
- Multiphase High Current Output Reduces Required Capacitance
- Integrated High Current MOSFET Drivers
- 300KHz, 500KHz and 600KHz High Frequency Operation Minimizes External Component Requirements
- Independent Phase Programmable Soft-Start and Power Sequencing
- Adjustable Linear Regulator Driver Output
- No current-sense resistors

APPLICATIONS/BENEFITS

- Multi-Output Power Supplies
- Video Card Power Supplies
- DDR, VDDQ and Termination Supply
- PC Peripherals
- Portable PC Processor and I/O Supply

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_A (°C)	Switching Frequency (kHz)	PW Plastic TSSOP 28-Pin RoHS Compliant / Pb-free Transition DC: 0518	LQ Plastic MLPQ 38-Pin RoHS Compliant / Pb-free Transition DC: 0512
0 to 70	300	**LX1672-03CPW**	**LX1672-03CLQ**
0 to 70	500	**LX1672-05CPW**	
0 to 70	600		**LX1672-06CLQ**

NOTE: Available in Tape & Reel. Append the letters "TR" to the part number (i.e. LX1672-06CLQ-TR)

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) DC .....-0.3V to 5.5V
Driver Supply Voltage (V_{Cx}, V_{CCL}) DC .....-0.3V to 12V
Current Sense Inputs (V_{SX}, C_{SX}) ..... -0.3V to 12V
Error Amplifier Inputs (FB_X, RF_2, LDFB).....-0.3V to 5.5V
Input Voltage (SS / Enable, LDDIS) .....-0.3V to5.5V
Output Drive Peak Current Source (HO*x*, LO*x*).....1A (500ns)
Output Drive Peak Current Sink (HO*x*, LO*x*) 1A (500ns)
Operating Junction Temperature..... 150°C
Storage Temperature Range.....-65°C to 150°C
Peak Package Solder Reflow Temp.(40 second max. exposure) .... 260°C (+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

x= Denote Phases 1 & 2

THERMAL DATA

PW **Plastic TSSOP 28-Pin**

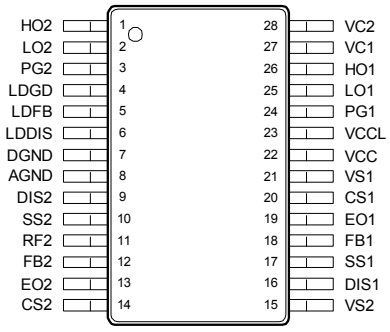
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	85°C/W

LQ **Plastic MLPQ 38-Pin**

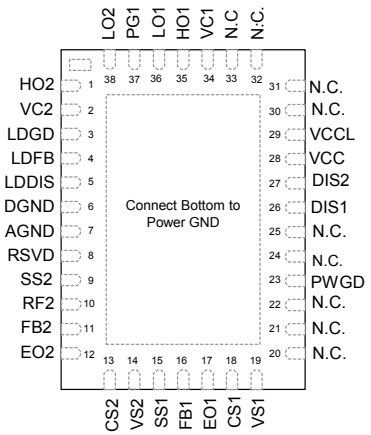
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	35°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JC})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

PACKAGE PIN OUT



PW PACKAGE
(Top View)



(N.C. – No Internal Connection
N/U – Not Used)

RoHS / Pb-free 100% Matte Tin Lead Finish

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FUNCTIONAL PIN DESCRIPTION

NAME	DESCRIPTION
FB1	**Bi-Phase Operation:** Phase 1 and 2 Voltage Feedback **Single Phase Operation:** Phase 1 Voltage Feedback – connected to the output through a resistor network to set desired output voltage of Phase 1
EO*X*	Error Amplifier Output – Sets external compensation for the corresponding phase denoted by "X".
FB2	**Bi-phase Operation:** Load Sharing Voltage Sense Feedback – Connect filtered phase 2 switching output (pre-inductor) to FB_2 to ensure proper current sharing between phase 1 and phase 2. **Single Phase Operation:** Phase 2 Voltage Feedback – connected to the output through a resistor network (post inductor) to set desired output voltage of Phase 2.
RF2	**Bi-Phase Operation:** Load Sharing Voltage Sense Feedback Reference – Sets reference for current sharing control loop. Connecting filtered phase 1 switching output (pre-inductor) to REF_2 forces average current in phase 2 to be equal to phase 1. **Single Phase Operation:** Phase 2 Voltage Reference – connected to SS2 pin as reference.
VCC	IC supply voltage (nominal 5V).
VCCL	Power supply pin for all Low side drivers.
LDFB	Low Dropout Regulator Voltage Feedback – Sets output voltage of external MOSFET via resistor network.
CS*X*	Over-Current Limit Set – Connecting a resistor between CS pin and the source of the high-side MOSFET sets the current-limit threshold for the corresponding phase denoted by "X". Exceeding the current-limit threshold forces the corresponding phase into hiccup mode protection. A minimum of 1KΩ must be in series with this input.
SS*X*	Soft-start/Hiccup Capacitor Pin – During start-up, the voltage on this pin controls the output voltage of its respective regulator. An internal 20kΩ resistor and the external capacitor set the time constant for soft-start function. The Soft-start function does not initialize until the supply voltage exceeds the UVLO threshold. When an over-current condition occurs, this capacitor is used for the timing of hiccup mode protection.
AGND	Analog ground reference.
DGND	Digital ground reference.
LDGD	Low Dropout Regulator Gate Drive – Connects to gate of external N-Channel MOSFET for linear regulator function.
PG*X*	Driver Power Ground. Connects to the source of the bottom N-channel MOSFETS of phase 1 where X=1, and phase 2 where X=2 for the TSSOP. The MLPQ package has a common PG output .
HO*X*	High Side MOSFET Gate Driver – "X" denotes corresponding phase.
LO*X*	Low Side MOSFET Gate Driver – "X" denotes corresponding phase.
VC*X*	Phase High-Side MOSFET Gate Driver Supply – Connect to separate supply or boot strap supply to ensure proper high-side gate driver supply voltage. "X" denotes corresponding phase. If the phase is not used connect to VCC.
LDDIS	LDO Disable input. High disables the LDO output. This pin has a 100KΩ nominal pull down resistor
VS*X*	Voltage reference for Current sense. This is also the supply pin for the Current Sense Comparator. "X" denotes corresponding phase. This pin cannot be left floating, if the phase is not used connect to VCC
DIS*X*	PWM Disable Input – High disables the PWM output. This pin has a nominal 80KΩ pull down resistor. "X" denotes corresponding phase.
PWGD	Open drain output , high at end of Soft Start and no Fault. Pulls low if any Fault condition occurs. This output is present on the MLP package only.

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature $0°C \leq T_A \leq 70°C$ except where otherwise noted and the following test conditions: V_{CC} = 5V, V_{CCL} = 5V, V_{CX} = 12V, HOX = LOX = 3000pF Load.

Parameter	Symbol	Test Conditions	LX1672 Min	LX1672 Typ	LX1672 Max	Units
SWITCHING REGULATORS						
Input Voltage	V_{CC}		4.5		5.5	V
Input Voltage	V_{CCL}, V_{CX}				12	V
Operation Current	I_{CC}	Static and Dynamic		10		mA
Reference Voltage	V_{SS}	T_A = 25°C	0.792	0.8	0.808	V
		0°C ≤ T_A ≤ 70°C	0.784		0.816	
Line Regulation (Note 2)			-1		1	%
Load Regulation (Note 2)			-1		1	%
Minimum Pulse Width		TSSOP Package			250	nS
Minimum Pulse Width		MLPQ Package			150	nS
Maximum Duty Cycle		LX1672-03 Load = 3000pF	85			%
Maximum Duty Cycle		LX1672-05 Load = 3000pF	75			%
Maximum Duty Cycle		LX1672-06 Load = 3000pF	70			%
ERROR AMPLIFIERS						
Input Offset Voltage	Vos	Common Mode Input Voltage = 1V	-6.0		6.0	mV
DC Open Loop Gain				70		dB
Unity Gain Bandwidth	UGBW			16		MHz
High Output Voltage	V_{OH}	I Source = 2mA	3.5	3.8		V
Low Output Voltage	V_{OL}	I Sink = 10µA		200	400	mV
Input Common Mode Range		Input Offset Voltage ≤ 20mV	.1		3.5	V
Input Bias Current	I_{IN}	0 and 3.5 V Common Mode Input Voltage		100		nA
CURRENT SENSE						
Current Sense Bias Current	I_{SET}	V_{CSX} = V_{VSX} – 0.3V , V_{VSX} = 5V	45	50	55	µA
Trip Threshold	V_{TRIP}	Referenced to VSX , V_{VSX} = 5V	260	300	340	mV
Current Sense Delay	T_{CSD}			350		nS
Current Sense Comparator Operating Current	I_{CSX}	Current into VS*X* pins		2	5	mA
OUTPUT DRIVERS – N-CHANNEL MOSFETS						
Low Side Driver Operating Current	I_{VCCL}	Static		2.5		mA
High Side Driver Operating Current	I_{VCX}	Static		3		mA
Drive Rise Time, Fall Time	T_{RF}	C_L = 3000pF		50		nS
High Level Output Voltage	V_{DH}	I_{SOURCE} = 20mA, V_{CCL} = 12V	10	11		V
Low Level Output Voltage	V_{DL}	I_{SINK} = 20mA, V_{CCL} = 12V		0.15	0.25	V
OSCILLATOR						
PWM Switching Frequency	F_{SW}	LX1672-03	255	300	345	KHz
PWM Switching Frequency		LX1672-05	425	500	575	KHz
PWM Switching Frequency		LX1672-06	510	600	690	KHz
Ramp Amplitude	V_{RAMP}			1.25		V_{PP}

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C ≤ T_A ≤ 70°C except where otherwise noted and the following test conditions: V_{CC} = 5V, V_{CCL} = 5V, V_{CX} = 12V, HOX = LOX = 3000pF Load

Parameter	Symbol	Test Conditions	LX1672			Units
			Min	Typ	Max	
UVLO AND SOFT-START (SS)						
Start-Up Threshold (V_{CX}), (V_{CCL})			3.5	4.0	4.5	V
Start-Up Threshold (V_{CC})			4.0	4.25	4.5	V
Hysteresis Vcc				0.1		V
SS Input Resistance	R_{SS}			20		KΩ
SS Shutdown Threshold	V_{SHDN}			0.15		V
Hiccup Mode Duty Cycle		C_{SS} = 0.1µF		10		%
LINEAR REGULATOR CONTROLLER						
Voltage Reference Tolerance		V_{LDFB} = 0.8V, C_{OUT} = 330µF		2		%
Source Current	I_{HDRV}	V_{OUT} = 9V	6			mA
Sink Current	I_{LDRV}	V_{OUT} = 0.4V		0.2		mA
DISABLE INPUT						
PWM Disable	DISX			1.0		V
		Pull down Resistance		80		KΩ
LDO Disable	LDDIS			2.5		V
		Pull down Resistance		100		KΩ

Note 1 – X = Phase 1,2
Note 2 – System Specification

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BLOCK DIAGRAM

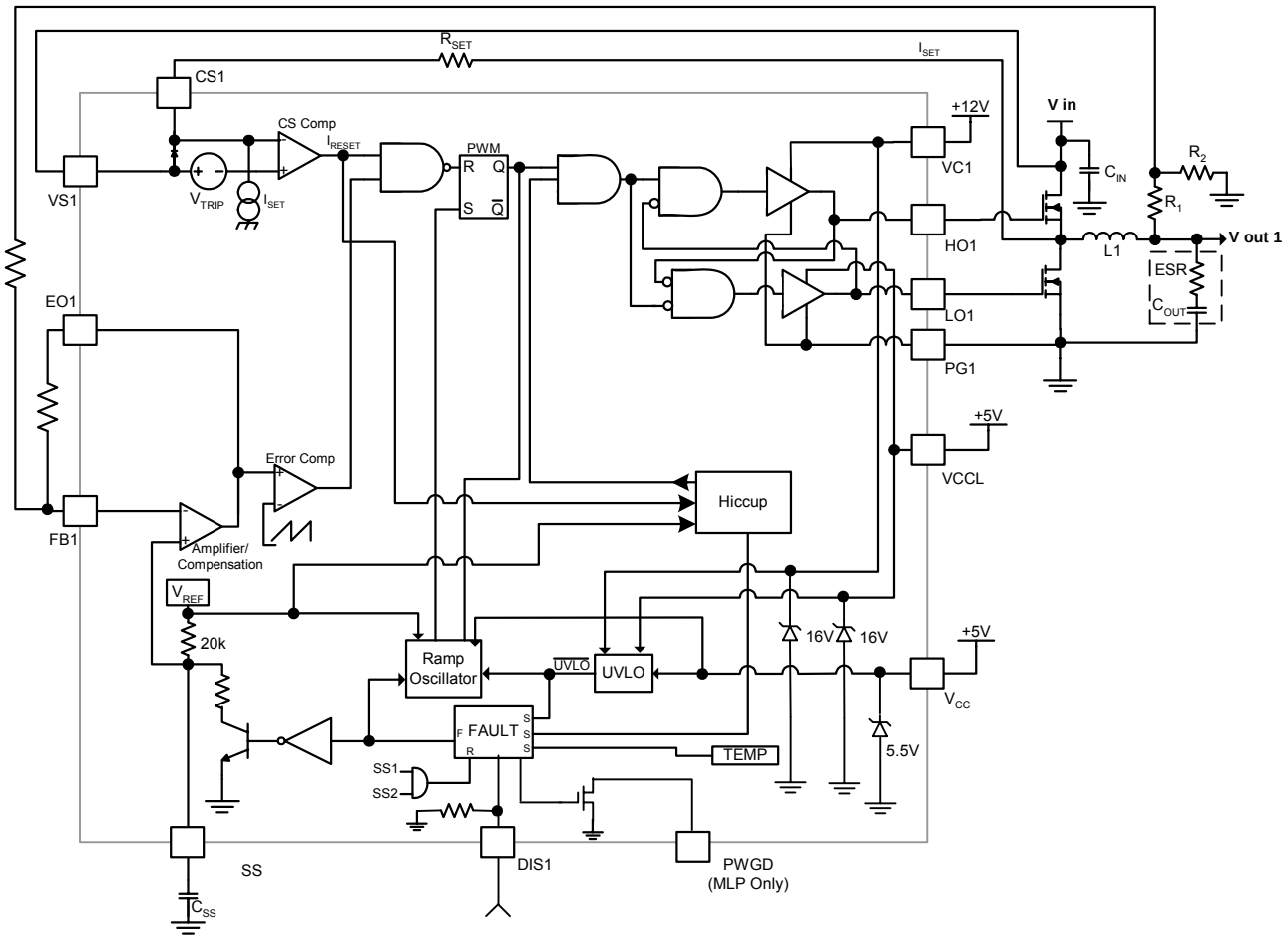

Figure 1 – Block Diagram of PWM Phase 1

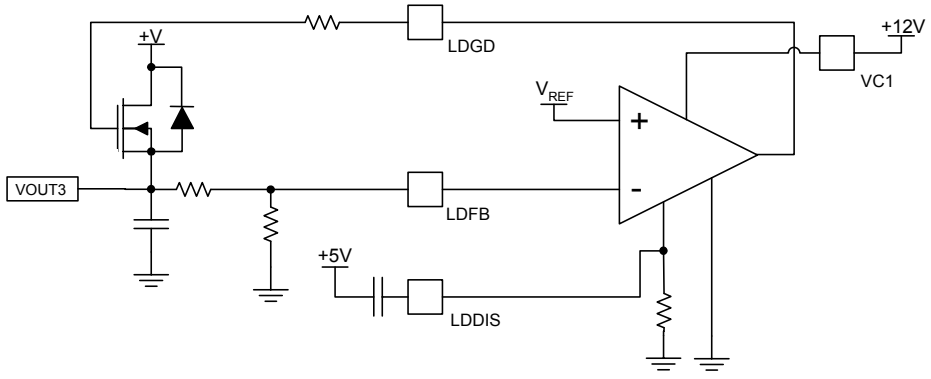

Figure 2 – LDO Controller Block Diagram

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BLOCK DIAGRAM

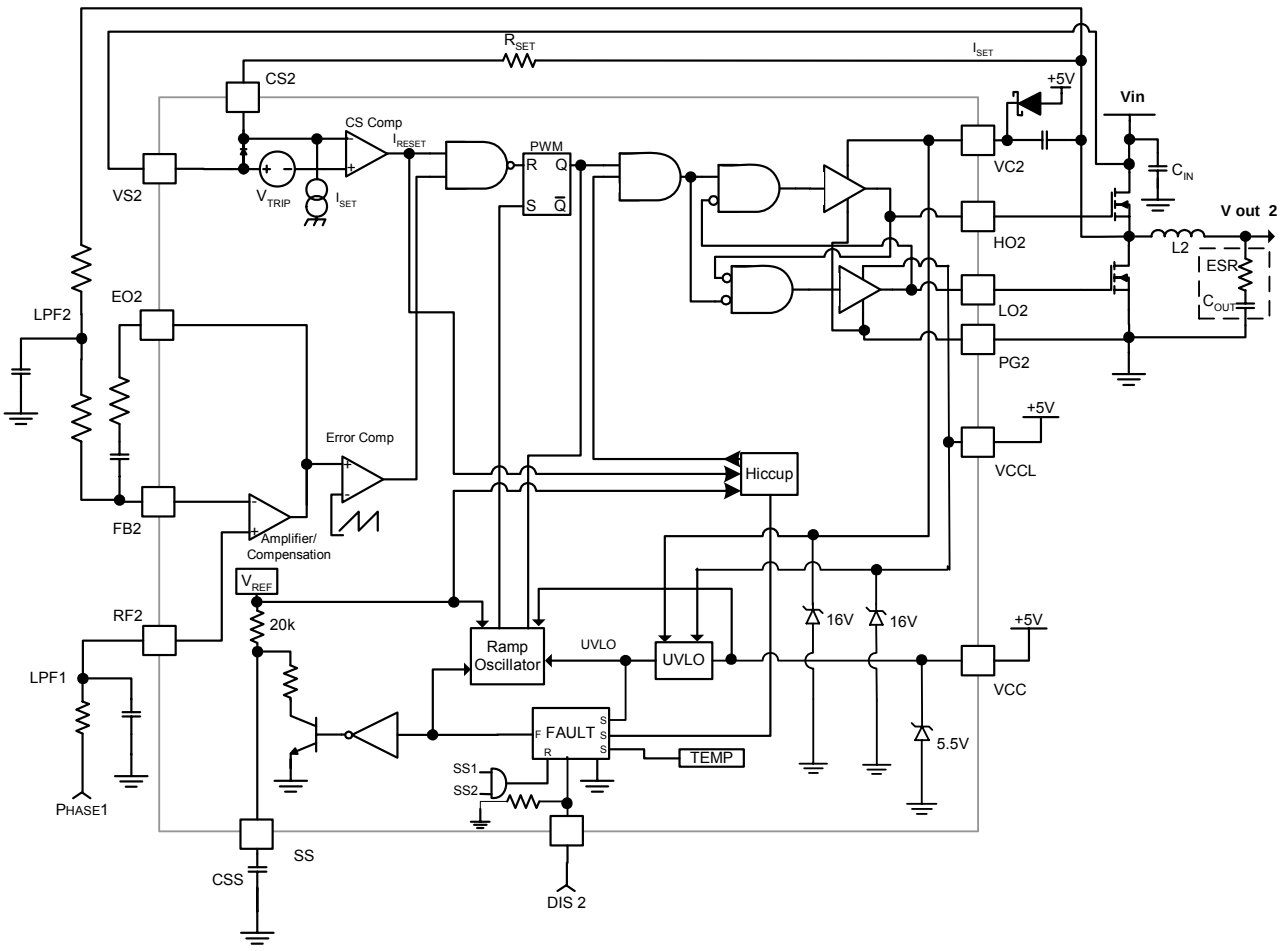

Figure 3– Block Diagram of Phase 2 Connected in LoadSHARE Mode

Note: With the MLPQ package there is only one PG*X* output (PG1 and PG2 are common)

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APPLICATION CIRCUIT

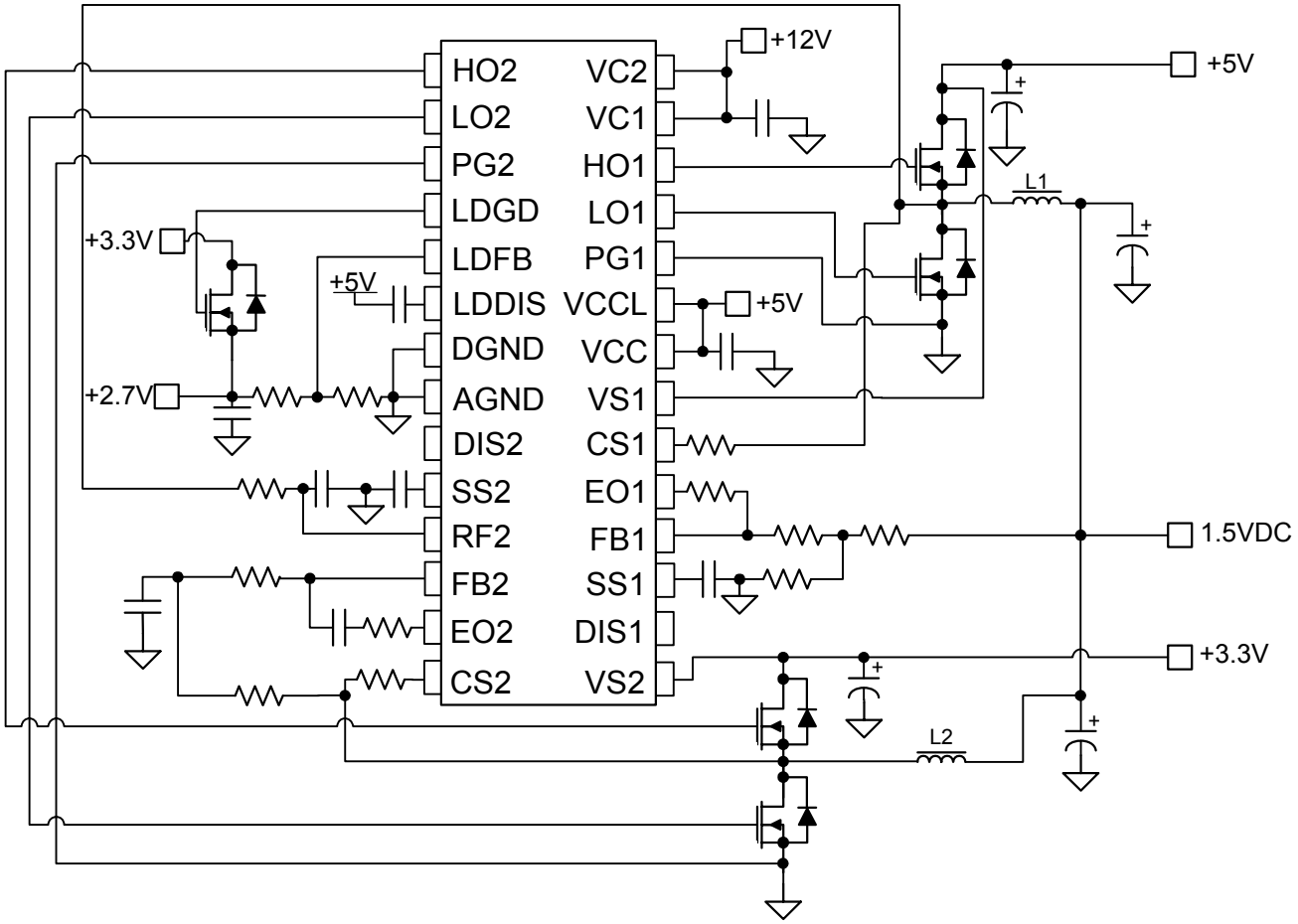

Figure 4 – Bi-Phase Operation With Phase 1 & 2 LoadSHARING™ From 5V & 3.3V

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APPLICATION CIRCUIT

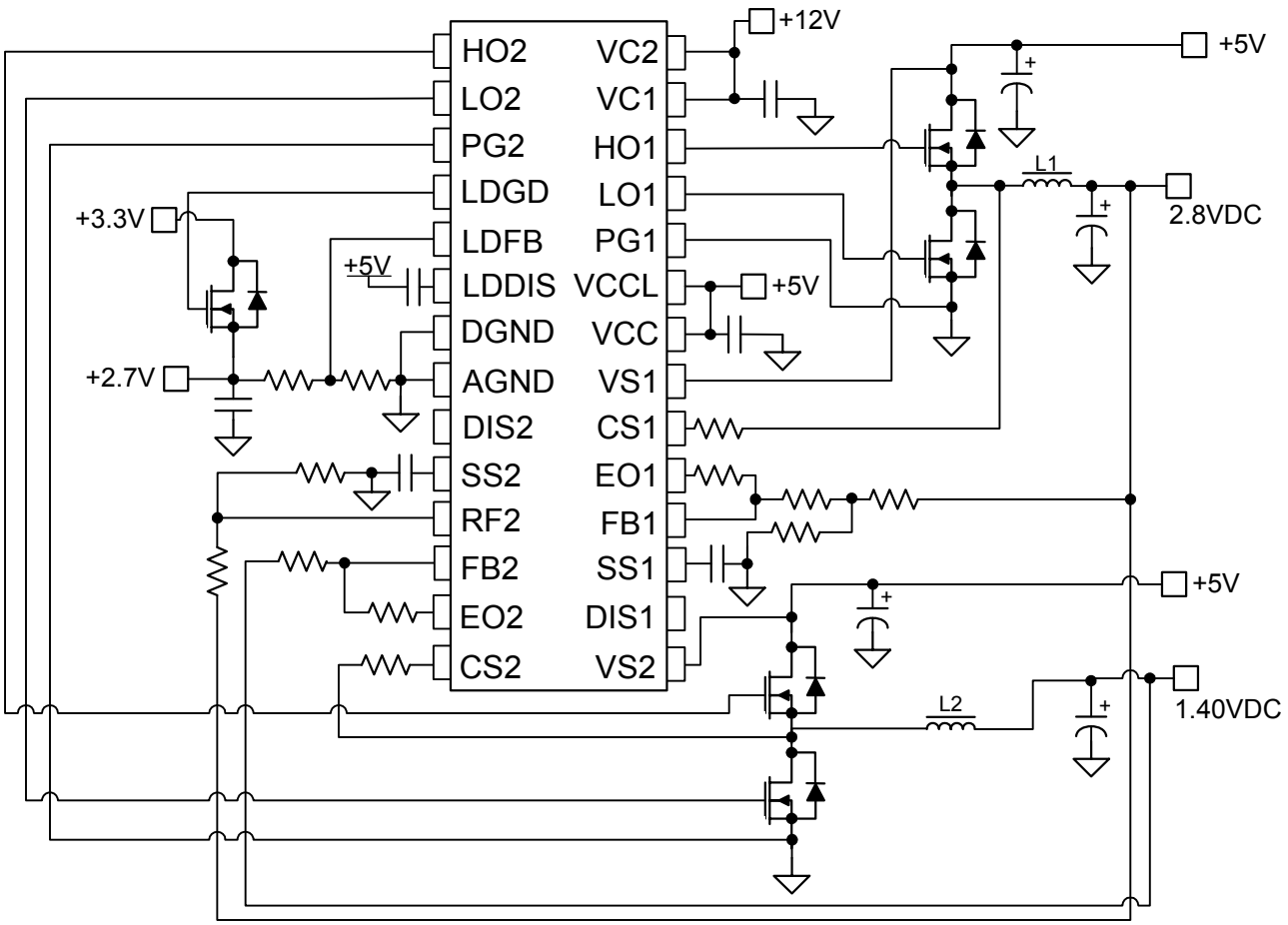

Figure 5 – Bi-Phase Operation with Phase 2 Output Tracking The Output of Phase 1.

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THEORY OF OPERATION

GENERAL DESCRIPTION

The LX1672 is a voltage-mode pulse-width modulation controller integrated circuit. The internal ramp generator frequency is fixed to 300kHz. The device has external compensation, for more flexibility of output current magnitude.

UNDER VOLTAGE LOCKOUT (UVLO)

At power up, the LX1672 monitors the supply voltage for VCC, VCCL, and VC*X* (there is no requirement for sequencing the supplies). Before all supplies reach their under-voltage lock-out (UVLO) thresholds, the soft-start (SS) pin is held low to prevent soft-start from beginning, the oscillator is disabled and all MOSFETs are held off. There is an internal delay that will filter out transients less that 1.5µSec.

SOFT-START

Once the supplies are above the UVLO threshold, the soft-start capacitor begins to be charged by the reference through a 20kΩ internal resistor. The capacitor voltage at the SS pin rises as a simple RC circuit. The SS pin is connected to the error amplifier's non-inverting input that controls the output voltage. The output voltage will follow the SS pin voltage if sufficient charging current is provided to the output capacitor.

The simple RC soft-start allows the output to rise faster at the beginning and slower at the end of the soft-start interval. Thus, the required charging current into the output capacitor is less at the end of the soft-start interval. A comparator monitors the SS pin voltage and indicates the end of soft-start when SS pin voltage reaches 95% of V_{REF}.

OVER-CURRENT PROTECTION (OCP) AND HICCUP

The LX1672 uses the $R_{DS(ON)}$ of the upper MOSFET, together with a resistor (R_{SET}) to set the actual current limit point. The current sense comparator senses the MOSFET current 350nS after the top MOSFET is switched on in order to reduce inaccuracies due to ringing. A current source supplies a current (I_{SET}), whose magnitude is 50µA. The set resistor R_{SET} is selected to set the current limit for the application. R_{SET} and VS*X* should be connected directly at the upper MOSFET drain and source to get an accurate measurement across the low resistance $R_{DS(ON)}$.

When the sensed voltage across $R_{DS(ON)}$ plus the set resistor exceeds the 300mV, V_{TRIP} threshold, the OCP comparator outputs a signal to reset the PWM latch and to start hiccup mode. The soft-start capacitor (C_{SS}) is discharged slowly (10 times slower than when being charged up by R_{SS}). When the voltage on the SS pin reaches a 0.1V threshold, hiccup finishes and the circuit soft-starts again. During hiccup both MOSFETs for that phase are held off.

Hiccup is disabled during the soft-start interval, allowing start up with maximum current. If the rate of rise of the output voltage is too fast, the required charging current to the output capacitor may be higher than the limit-current. In this case, the peak MOSFET current is regulated to the limit-current by the current-sense comparator. If the MOSFET current still reaches its limit after the soft-start finishes, the hiccup is triggered again. When the output has a short circuit the hiccup circuit ensures that the average heat generation in both MOSFETs and the average current is much less than in normal operation.

Over-current protection can also be implemented using a sense resistor, instead of using the $R_{DS(ON)}$ of the upper MOSFET, for greater set-point accuracy.

OSCILLATOR FREQUENCY

An internal oscillator sets the PWM switching frequency at 300KHz, 500KHz, or 600KHz.

THEORY OF OPERATION FOR A BI-PHASE, LOADSHARE CONFIGURATION

The basic principle used in LoadSHARING™, in a multiple phase buck converter topology, is that if multiple, identical, inductors have the same identical voltage impressed across their leads, they must then have the same identical current passing through them. The current that we would like to balance between inductors is mainly the DC component along with as much as possible the transient current. All inductors in a multiphase buck converter topology have their output side tied together at the output filter capacitors. Therefore, this side of all the inductors have the same identical voltage.

If the input side of the inductors can be forced to have the same equivalent DC potential on this lead, then they will have the same DC current flowing. To achieve this requirement, phase 1 will be the control phase that sets the output operating voltage, under normal PWM operation. To force the current of phase 2 to be equal to the current of phase 1, a second feedback loop is used. Phase 2 has a low pass filter connected from the input side of each inductor. This side of the inductors has a square wave signal that is proportional to its duty cycle. The output of each LPF is a DC (+ some AC) signal that is proportional to the magnitude and duty cycle of its respective inductor signal. The second feedback loop will use the output of the phase 1 LPF as a reference signal for an error amplifier that will compare this reference to the output of the phase 2 LPF. This error signal will be amplified and used to control the PWM circuit of phase 2. Therefore, the duty cycle of phase 2 will be set so that the equivalent voltage potential will be forced across the phase 2 inductor as compared to the phase 1 inductor. This will force the current in the phase 2 inductor to follow and be equal to the current in the phase 1 inductor.

There are four methods that can be used to implement the LoadSHARE feature of the LX1672 in the Bi-Phase mode of operation.

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THEORY OF OPERATION (CONTINUED)

BI-PHASE, LOADSHARE (ESR METHOD)

The first method is to change the ratio of the inductors equivalent series resistance, (ESR). As can be seen in the previous example, if the offset error is zero and the ESR of the two inductors are identical; then the two inductor currents will be identical. To change the ratio of current between the two inductors, the value of the inductor's ESR can be changed to allow more current to flow through one inductor than the other. The inductor with the lower ESR value will have the larger current. The inductor currents are directly proportional to the ratio of the inductor's ESR value.

The following circuit description shows how to select the inductor ESR for each phase where a different amount of power is taken from two different input power supplies. A typical setup will have a +5V power supply connected to the phase 1 half bridge driver and a +3.3V power supply connected to the phase 2 half bridge driver. The combined power output for this core voltage is 18W (+1.5V @ 12A). For this example the +5V power supply will supply 7W and the +3.3V power supply will supply the other 11W. 7W @ 1.5V is a 4.67A current through the phase 1 inductor. 11W @ 1.5V is a 7.33A current through the phase 2 inductor. The ratio of inductor ESR is inversely proportional to the power level split. $\frac{ESR1}{ESR2} = \frac{I2}{I1}$

The higher current inductor will have the lower ESR value. If the ESR of the phase 1 inductor is selected as 10mΩ, then the ESR value of the phase 2 inductor is calculated as:

$$\left(\frac{4.67A}{7.33A}\right) \times 10\,\text{m}\Omega = 6.4\,\text{m}\Omega$$

Depending on the required accuracy of this power sharing; inductors can be chosen from standard vendor tables with an ESR ratio close to the required values. Inductors can also be designed for a given application so that there is the least amount of compromise in the inductor's performance.

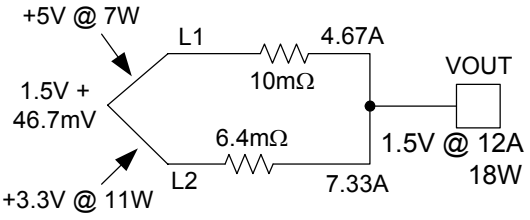

Figure 7 – Ratio LoadSHARE™ Using Inductor ESR

BI-PHASE, LOADSHARE (FEEDBACK DIVIDER METHOD)

Sometimes it is desirable to use the same inductor in both phases while having a much larger current in one phase versus the other. A simple resistor divider can be used on the input side of the Low Pass Filter that is taken off of the switching side of the inductors. If the Phase 2 current is to be larger than the current in Phase 1; the resistor divider is placed in the feedback path before the Low Pass Filter that is connected to the Phase 2 inductor. If the Phase 2 current needs to be less than the current in Phase 1; the resistor divider is then placed in the feedback path before the Low Pass Filter that is connected to the Phase 1 inductor.

As in Figure 7, the millivolts of DC offset created by the resistor divider network in the feedback path, appears as a voltage generator between the ESR of the two inductors.

A divider in the feedback path from Phase 2 will cause the voltage generator to be positive at Phase 2. With a divider in the feedback path of Phase 1 the voltage generator becomes positive at Phase 1. The Phase with the positive side of the voltage generator will have the larger current. Systems that operate continuously above a 30% power level can use this method, a down side is that that the current difference between the two inductors still flows during a no load condition.

This produces a low efficiency condition during a no load or light load-state, this method should not be used if a wide range of output power is required.

The following description and Figure 8 show how to determine the value of the resistor divider network required to generate the offset voltage necessary to produce the different current ratio in the two output inductors. The power sharing ratio is the same as that of Figure 7. The Offset Voltage Generator is symbolic for the DC voltage offset between Phase 1 & 2. This voltage is generated by small changes in the duty cycle of Phase 2. The output of the LPF is a DC voltage proportional to the duty cycle on its input. A small amount of attenuation by a resistor divider before the LPF of Phase 2 will cause the duty cycle of Phase 2 to increase to produce the added offset at V2. The high DC gain of the error amplifier will force LPF2 to always be equal to LPF1. The following calculations determine the value of the resistor divider necessary to satisfy this example.

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THEORY OF OPERATION (CONTINUED)

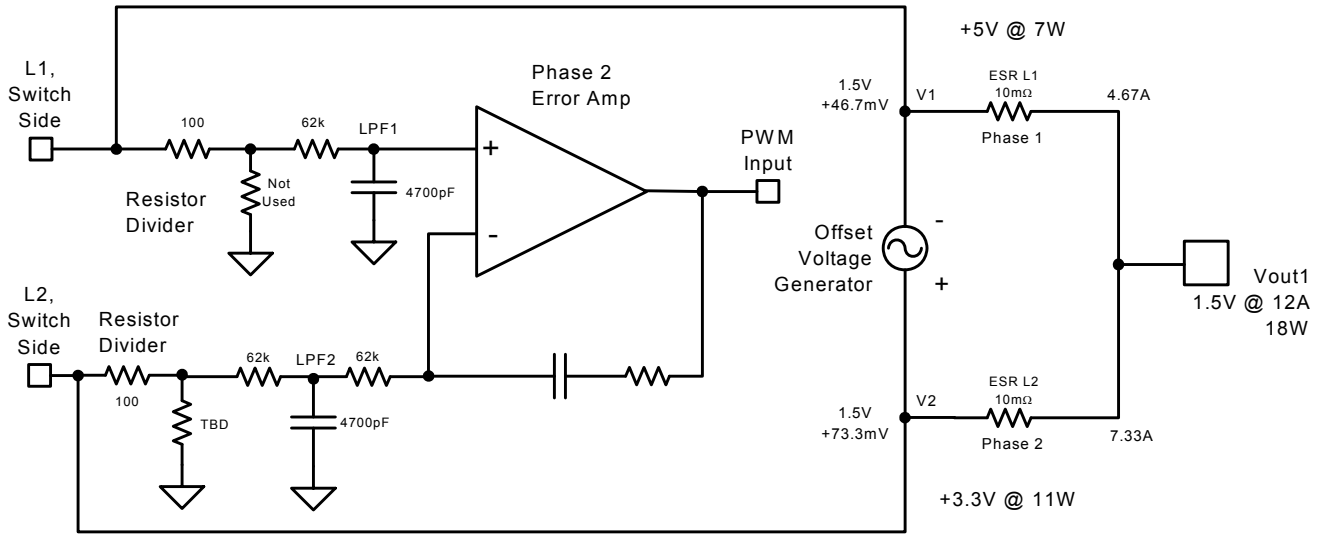

Figure 8 – LoadSHARE™ Using Feedback Divider Offset

Where V1 = 1.5467 ; V2 = 1.5733 and $K = \frac{V1}{V2}$ then $TBD = \frac{K \times 100}{1 - K} = 5.814\,K$

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THEORY OF OPERATION (CONTINUED)

BI-PHASE, LOADSHARE™ (PROPORTIONAL METHOD)

The best topology for generating a current ratio at full load and proportional between full load and no load is shown in figure 9. The DC voltage difference between LPF1 and VOUT is a voltage that is proportional to the current flowing in the Phase 1 inductor. This voltage can be amplified and used to offset the voltage at LPF2 through a large impedance that will not significantly alter the characteristics of the low pass filter. At no load there will be no offset voltage and no offset current between the two phases. This will give the highest efficiency at no load.

Also a speed up capacitor can be used between the offset amplifier output and the negative input of the Phase 2 error amplifier. This will improve the transient response of the Phase 2 output current, so that it will share more equally with phase 1 current during a transient condition.

The use of a MOSFET input amplifier is required for the buffer to prevent loading the low pass filter. The gain of the offset amplifier, and the value of Ra and Rb, will determine the ratio of currents between the phases at full load. Two external amplifiers are required or this method.

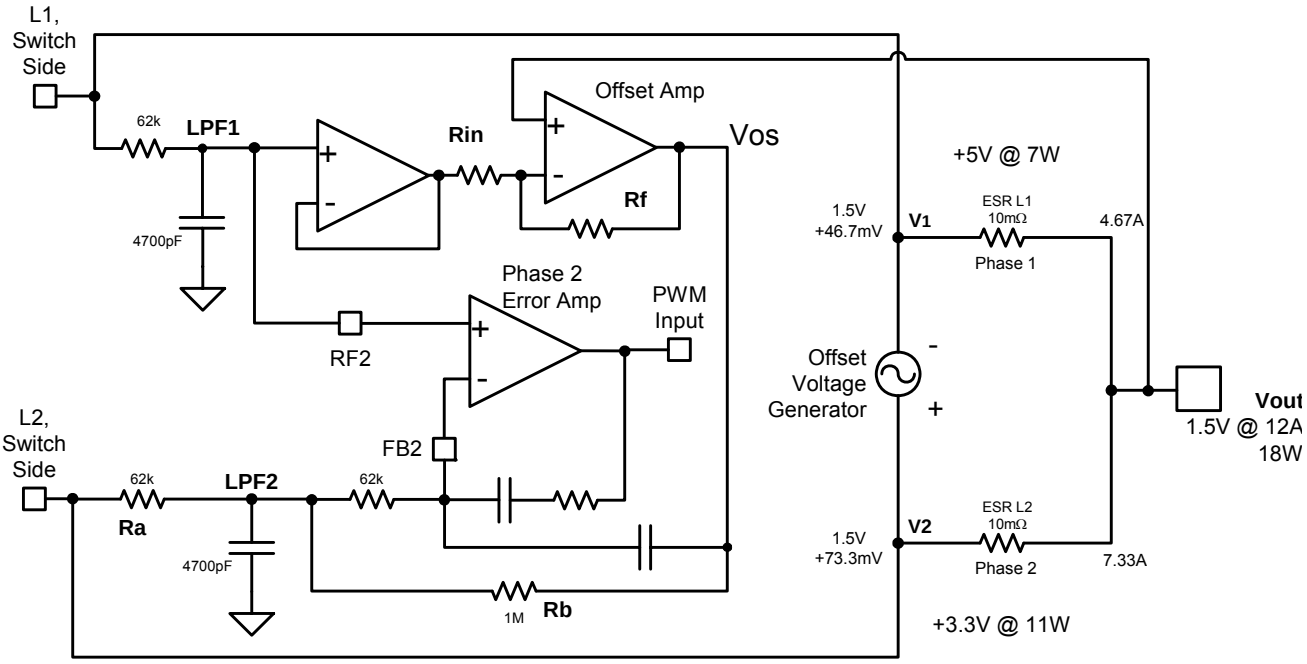

Figure 9 –LoadSHARE™ Using Proportional Control

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THEORY OF OPERATION (CONTINUED)

The circuit in Figure 9 sums a current through a 1MΩ resistor (Rb) offsetting the phase 2 error amplifier to create an imbalance in the L1 and L2 currents. Although there are many ways to calculate component values the approach taken here is to pick Ra, Rb, R_{IN}, V_{OUT}, and inductor ESR. A value for the remaining resistor Rf can then be calculated.

The first decision to be made is the current sharing ratio, follow the previous examples to understand the basics of LoadSHARE™. The most common reason to imbalance the current in the two phases is because of limitations on the available power from the input rails for each phase. Use the available input power and total required output power to determine the inductor currents for each phase.

All references are to Figure 9

1) Calculate the voltages V1 and V2.

$$V1 = L1\,Current \times L1\,ESR + Vout$$

$$V2 = L2\,Current \times L2\,ESR + Vout$$

2) Select values for Ra and Rb (Ra is typically 62KΩ ; Rb is typically 1MΩ)

3) Calculate the offset voltage Vos at the output of the offset amplifier

$$Vos = V2 - \left(\frac{V2 - V1}{Ra}\right) \times (Ra + Rb)$$

4) Calculate the value for Rf

(select a value for R_{IN} typically 5KΩ)

$$Rf = R_{IN}\left(\frac{Vos - V_{OUT}}{V_{OUT} - V1}\right)$$

Due to the high impedances in this circuit layout can affect the actual current ratio by allowing some of the switching waveforms to couple into the current summing path. It may be necessary to make some adjustment in Rf after the final layout is evaluated. Also, the equation for Rf requires very accurate numbers for the voltages to insure an accurate result.

BI-PHASE, LOADSHARE™ (SERIES RESISTOR METHOD)

A fourth but less desirable way to produce the ratio current between the two phases is to add a resistor in series with one of the inductors. This will reduce the current in the inductor that has the resistor and increase the current in the inductor of the opposite phase. The example of Figure 7 can be used to determine the current ratio by adding the value of the series resistor to the ESR value of the inductor. The added resistance will lower the overall efficiency

LoadSHARE ERROR SOURCES

With the high DC feedback gain of this second loop, all phase timing errors, $R_{DS(On)}$ mismatch, and voltage differences across the half bridge drivers are removed from the current sharing accuracy. The errors in the current sharing accuracy are derived from the tolerance on the inductor's ESR and the input offset voltage specification of the error amplifier. The equivalent circuit is shown next for an absolute worst case difference of phase currents between the two inductors.

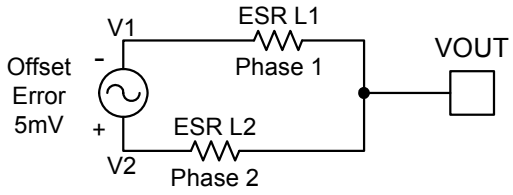

Figure 6 – Error Amplitude

Nominal ESR of 6mΩ. ESR ±5%

Max offset Error = 6mV

+5% ESR L1 = 6.3 mΩ

-5% ESR L2 = 5.7 mΩ

$$\text{If phase 1 current} = 12\,A = \frac{V1 - V_{OUT}}{ESR\,L1}$$

$$V1 - V_{OUT} = 12 \times 6.3 \times 10^{-3} = 75.6\,mV$$

$$V2 = V1 + 6\,mV = 81.6\,mV$$

$$\text{Phase 2 current} = \frac{V2 - V_{OUT}}{ESR\,L2} = \frac{81.6 \times 10^{-3}}{5.7 \times 10^{-3}} = 14.32\,A$$

Phase 2 current is 2.32A greater than Phase 1.

Input bias current also contributes to imbalance.

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APPLICATION NOTE

OUTPUT INDUCTOR

The output inductor should be selected to meet the requirements of the output voltage ripple in steady-state operation and the inductor current slew-rate during transient. The peak-to-peak output voltage ripple is:

$$V_{RIPPLE} = ESR \times I_{RIPPLE}$$

where

$$\Delta I = \frac{V_{IN} - V_{OUT}}{L} \times \frac{D}{f_s}$$

ΔI is the inductor ripple current, L is the output inductor value and ESR is the Effective Series Resistance of the output capacitor.

ΔI should typically be in the range of 20% to 40% of the maximum output current. Higher inductance results in lower output voltage ripple, allowing slightly higher ESR to satisfy the transient specification. Higher inductance also slows the inductor current slew rate in response to the load-current step change, ΔI, resulting in more output-capacitor voltage droop. When using electrolytic capacitors, the capacitor voltage droop is usually negligible, due to the large capacitance

The inductor-current rise and fall times are:

$$T_{RISE} = L \times \frac{\Delta I}{(V_{IN} - V_{OUT})}$$

and

$$T_{FALL} = L \times \frac{\Delta I}{V_{OUT}}$$

The inductance value can be calculated by

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \times \frac{D}{f_s}$$

OUTPUT CAPACITOR

The output capacitor is sized to meet ripple and transient performance specifications. Effective Series Resistance (ESR) is a critical parameter. When a step load current occurs, the output voltage will have a step that equals the product of the ESR and the current step, ΔI. In an advanced microprocessor power supply, the output capacitor is usually selected for ESR instead of capacitance or RMS current capability. A capacitor that satisfies the ESR requirements usually has a larger capacitance and current capability than strictly needed. The allowed ESR can be found by:

$$ESR \times (I_{RIPPLE} + \Delta I) < V_{EX}$$

Where I_{RIPPLE} is the inductor ripple current, ΔI is the maximum load current step change, and V_{EX} is the allowed output voltage excursion in the transient.

Electrolytic capacitors can be used for the output capacitor, but are less stable with age than tantalum capacitors. As they age, their ESR degrades, reducing the system performance and increasing the risk of failure. It is recommended that multiple parallel capacitors be used, so that, as ESR increase with age, overall performance will still meet the processor's requirements.

There is frequently strong pressure to use the least expensive components possible; however, this could lead to degraded long-term reliability, especially in the case of filter capacitors. Microsemi's demonstration boards use the CDE Polymer AL-EL (ESRE) filter capacitors, which are aluminum electrolytic, and have demonstrated reliability. The OS-CON series from Sanyo generally provides the very best performance in terms of long term ESR stability and general reliability, but at a substantial cost penalty. The CDE Polymer AL-EL (ESRE) filter series provides excellent ESR performance at a reasonable cost. Beware of off-brand, very low-cost filter capacitors, which have been shown to degrade in both ESR and general electrolytic characteristics over time.

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APPLICATION NOTE (CONTINUED)

INPUT CAPACITOR

The input capacitor and the input inductor, if used, are to filter the pulsating current generated by the buck converter to reduce interference to other circuits connected to the same 5V rail. In addition, the input capacitor provides local de-coupling for the buck converter. The capacitor should be rated to handle the RMS current requirements. The RMS current is:

$$I_{RMS} = I_L \sqrt{d(1-d)}$$

Where I_L is the inductor current and d is the duty cycle. The maximum value occurs when d = 50%, then $I_{RMS} = 0.5I_L$. For 5V input and output in the range of 2 to 3V, the required RMS current is very close to $0.5I_L$.

SOFT-START CAPACITOR

The value of the soft-start capacitor determines how fast the output voltage rises and how large the inductor current is required to charge the output capacitor. The output voltage will follow the voltage at the SS pin if the required inductor current does not exceed the maximum allowable current for the inductor. The SS pin voltage can be expressed as:

$$V_{SS} = V\,ref\left(1 - e^{-t/R_{SS}C_{SS}}\right)$$

Where R_{SS} and C_{SS} are the soft-start resistor and capacitor.

The current required to charge the output capacitor during the soft start interval is.

$$Iout = Cout\frac{dVss}{dt}$$

Taking the derivative with respect to time results in

$$Iout = \frac{VrefCout}{RssCss} e^{-t/R_{SS}C_{SS}}$$

and at t=0

$$Imax = \frac{VrefCout}{RssCss}$$

The required inductor current for the output capacitor to follow the soft start voltage equals the required capacitor current plus the load current. The soft-start capacitor should be selected to provide the desired power on sequencing and insure that the overall inductor current does not exceed its maximum allowable rating.

Values of Css equal to .1µF or greater are unlikely to result in saturation of the output inductor unless very large output capacitors are used..

OVER-CURRENT PROTECTION

Current limiting occurs at current level I_{CL} when the voltage detected by the current sense comparator is greater than the current sense comparator threshold, V_{TRIP} (300mV).

$$I_{CL} \times R_{DS(ON)} + I_{SET} \times R_{SET} = V_{TRIP}$$

So,

$$R_{SET} = \frac{V_{TRIP} - I_{CL} \times R_{DS(ON)}}{I_{SET}} = \frac{300\,mV - I_{CL} \times R_{DS(ON)}}{50\,\mu A}$$

Example:

For 10A current limit, using FDS6670A MOSFET (10mΩ $R_{DS(ON)}$):

$$R_{SET} = \frac{0.3 - 10 \times 0.010}{50 \times 10^{-6}} = 4K\,\Omega$$

Note: Maximum R_{SET} is 6KΩ. Any resistor 6KΩ or greater will not allow startup since I_{CL} will equal zero (50µA x 6KΩ = 300mV).

At higher PWM frequencies or low duty cycles, where the upper gate drive is less than 350nS wide, the 350nS delay for current limit enable may result in current pulses exceeding the desired current limit set point. If the upper MOSFET on time is less than 350nS and a short circuit condition occurs the duty cycle will increase, since V_{OUT} will be low. The current limit circuit will be enabled when the upper gate drive exceeds 350nS although the actual peak current limit value will be higher than calculated with the above equation.

Short circuit protection still exists due to the narrow pulse width even though the magnitude of the current pulses will be higher than the calculated value.

If OCP is not desired connect both VS*X* and VC*X* to VCC. Do not leave them floating.

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APPLICATION NOTE (CONTINUED)

OUTPUT DISABLE

The LX1672 PWM MOSFET driver outputs are shut off by pulling the disable (DIS*X*) pins above 1.2V.

The LDO voltage regulator has its own Disable pin (LDDIS) for control of this output voltage. Pulling this pin above 3V disables the LDO.

PROGRAMMING THE OUTPUT VOLTAGE

The output Voltage is sensed by the feedback pin (FB_X) which is compared to a 0.8V reference. The output voltage can be set to any voltage above 0.8V (and lower than the input voltage) by means of a resistor divider R1 - R2 (see Figure 1).

$$V_{OUT} = V_{REF}(1 + R_1/R_2)$$

Note: Keep R_1 and R_2 close to 1kΩ (order of magnitude)

DDR V_{TT} TERMINATION VOLTAGE

Double Data Rate (DDR) SDRAM requires a termination voltage (V_{TT}) in addition to the line driver supply voltage (VDDQ) and receiver supply voltage (VDD). Although it is not a requirement VDD is generally equal to VDDQ; so that only V_{TT} and VDDQ are required..

The LX1672 can supply both voltages by using two of the three PWM phases. Since the currents for V_{TT} and (VDD plus VDDQ) are quite often several amps, (2A to 6A is common) a switching regulator is a logical choice

V_{TT} for DDR memory can be generated with the LX1672 by using the positive input of the phase 2 error amplifier RF2 as a reference input from an external reference voltage V_{REF} which is defined as one half of VDDQ. Using V_{REF} as the reference input will insure that all voltages are correct and track each other as specified in the JEDEC (EIA/JESD8-9A) specification. The phase 2 output will then be equal to V_{REF} and track the VDDQ supply as required.

When an external reference is used the Soft Start will not be functional for that phase.

See Microsemi Application Note 17 for more details.

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APPLICATION

APPLICATION NOTE CONSIDERATIONS

1. The power N-MOSFET transistor's total gate charge spec, (Qg) should not exceed 40Nc when VCx = +12V. This condition will guarantee operation over the specified ambient temperature range. The Qg value of the N-MOSFET is directly related to the amount of power dissipation inside the IC package, from the two sets of MOSFET drivers. The equation relating Qg to the power dissipation of a MOSFET driver is: Pd = f * Qg * Vd . f = 300KHs and Vd is the supply voltage for the MOSFET driver. The two bottom MOSFET drivers are powered by the VCCL pin that is connected to +5V. The upper MOSFET drivers can be connected to the +12V supply or to a bootstrap supply generated by its output bridge. The bootstrap supply will be at +17V. Depending on the thermal environment of the application circuit, the Qg value of the N-MOSFETs will have to be less than the 40nC value. A typical configuration of the input voltage rails to generate the output voltages required is having the 5volt supply on phase 1 and the 3.3 volt supply on phase 2. At the max Qg value, the two bottom MOSFET drivers will dissipate 60mw each. The upper MOSFET drivers for phases 1 and 2 operate off of +12volts. Their dissipation is 144mw each. The total power dissipation for gate drive is 408 mw. Icc x Vcc =15ma x 5 V= 75mW. Total package power dissipation = 483mW. Using the thermal equation of: $T_J = T_A + Pd * Oja$, the Junction temperature for this IC package is = 23 + .483 * 85 which = 64°C. This means that the ambient temperature rise has to be less than 86°C.
2. The Soft-Start reference input has a 300mv threshold, above which the PWM starts to operate. The internal operating reference level is set at 800mV. This means that the output voltage is 37.5% low when the PWM becomes active. This starts each phase up in the current limit mode without Hiccup operation. If more than one phase is using the 5volt rail for conversion, then their soft-start capacitor values should be changed so that the two phases do not start up together. This will help reduce the amount of 5 volt input capacitance required. Also the VCC pin and the VCCL pin should be kept separated and should be decoupled separately. This will prevent the VCC pin from drooping back below the UVLO set point during start up.
3. If a phase is not used connect VS*X* and VC*X* pins to VCC. Do not leave them floating. A floating VS*X* pin will result in operation resembling a hiccup condition.
4. When phases 1 and 2 are used in the Bi-phase mode to current share into the same output load, the phase 2 current is forced to follow the phase 1 current. It is important to use a larger soft-start capacitor on phase 2 than phase 1 so that the phase 1 current becomes active before phase 2 becomes active. This will minimize any start up transient. It is also important to disable phase 1 and 2 at the same time. Disabling phase 1 without disabling phase 2, in the Bi-phase mode, allows phase 2 to turn on and off randomly because it has lost its reference.
5. The minimum R_{SET} resistor value is 1k ohm for the current limit sensing. If this resistor becomes shorted, it will do permanent damage to the IC.
6. A resistor has been put in series with the gate of the LDO pass transistor to reduce the output noise level. The resistor value can be changed to optimize the output transient response versus output noise.
7. The LDO controller inside the IC uses the voltage at VC1 as the drive voltage. Due to noise considerations ideally the voltage on the VC1 pin would be a fixed +12volt supply. When VC1 is connected to a bootstrap supply the LDO output will reflect significant switching noise without filtering.
8. To delay the turn on of the LDO controller output, a capacitor should be connected between the LDDIS pin and the +5volts. The LDDIS input has a 100K pull down resistor, which keeps the LDO active until this pin is pulled high. During the power up sequence the capacitor connected to the LDDIS pin will keep the LDO off until this capacitor, being charge by the 100K pull down resistor, goes through the low input threshold level.

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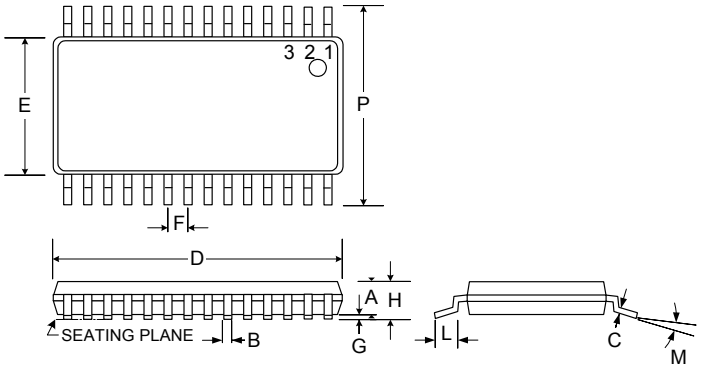
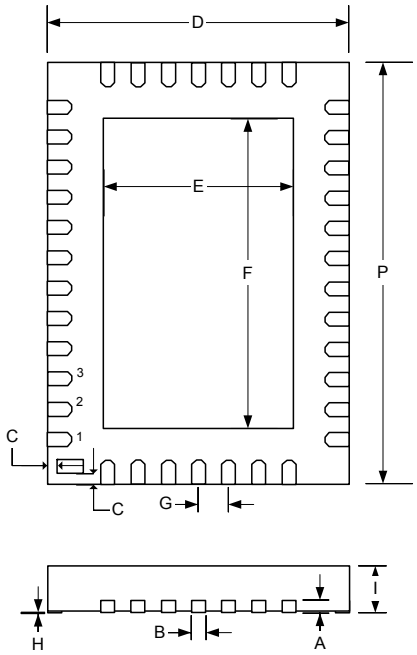
PACKAGE DIMENSIONS

PW 28-Pin Thin Small Shrink Outline (TSSOP)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.85	0.95	0.033	0.037
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.003	0.008
D	9.60	9.80	0.378	0.390
E	4.30	4.50	0.169	.176
F	0.65 BSC		0.025 BSC	
G	0.05	0.15	0.002	0.005
H	–	1.10	–	0.043
L	0.50	0.75	0.020	0.030
M	0°	8°	0°	8°
P	6.25	6.50	0.246	0.256
*LC	–	0.10	–	0.004

LQ 38-Pin Thin Micro Lead Quad Package (MLPQ)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.20 REF		0.0078 REF	
B	0.18	0.30	0.007	0.011
C	0.18	0.18	0.007	0.007
D	5.00 BSC		.196 BSC	
E	3.00	3.25	0.118	0.127
F	5.00	5.25	0.196	0.206
G	0.50 BSC		0.019 BSC	
H	0	0.05	0	0.19
I	0.70	0.80	0.027	0.031
P	7.00 BSC		0.275 BSC	

Note: Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(0.006”) on any side. Lead dimension shall not include solder coverage.

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