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Evaluation Board for the 7.5 GHz PLL Frequency Synthesizer

FEATURES

On-board regulators for 3 V, 5 V, 12 V power supplies
Includes OP27 for active filter applications
Designed for simple hook-up to an external VCO board

GENERAL DESCRIPTION

This board is designed to allow the user to evaluate the performance of the ADF4007 frequency synthesizer for PLLs (phase locked loops). The block diagram of the board is shown in Figure 1. It contains the ADF4007 synthesizer, links for choosing the divide ratio (8, 16, 32, and 64), an SMA connector for the reference input, and an RF input and output.

EVALUATION BOARD CONNECTION DIAGRAM

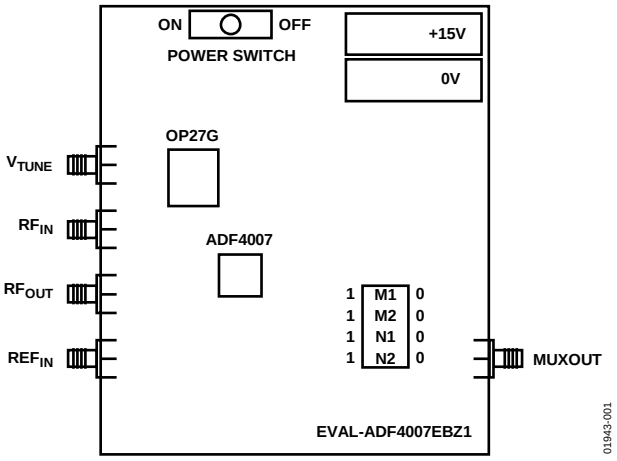

Figure 1.

TABLE OF CONTENTS

REVISION HISTORY

12/10—Revision 0: Initial Version

HARDWARE DESCRIPTION

The evaluation board is designed to work with an external VCO. The layout accommodates loop filter components and also has an op amp (OP27) for an active filter, if needed. The silk screen for the evaluation board is shown in Figure 2. The board schematic is shown in Figure 3 and Figure 4.

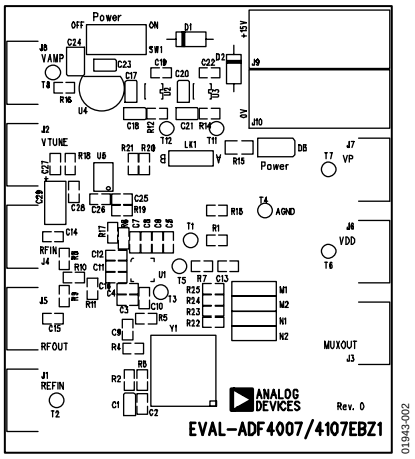

Figure 2. Evaluation Board Silkscreen

The board is powered from a single external 15 V supply. The power supply circuitry allows the user to choose either 3 V or 5 V for the ADF4007 V_P. The ADF4007 V_{DD} is 3.0 V, and the OP27 V_{CC} is 12 V. It is very important to note that the ADF4007 V_{DD} should never exceed 3.3 V or the ADF4007 V_P, whichever is less. Doing so can damage the device.

VTUNE is available at an output SMA connector. This should be connected to an external VCO board. The output of this board should then be connected back into the EVAL-ADF4007EBZ1 at RFIN. This is split into two equal power levels with one going to RFOUT and the other going to the RFIN of the ADF4007 to close the loop in the PLL. The RFOUT can be fed to a spectrum analyzer to test the output signal. It should have an amplitude of 6 dB down from the VCO specified output level.

TEST PROCEDURE FOR EVAL-ADF4007EBZ1

EQUIPMENT LIST

- EVAL-ADF4007EBZ1 evaluation board
- +15 V power supply
- Signal generator
- Oscilloscope
- Frequency counter
- Multimeter
- 50 Ω terminator
- Two BNC to SMA cables

TEST PROCEDURE

Step 1: Set Link/Switch Positions

1. Ensure that the link/switch positions are as follows:
   - LK1: Position A, Vp is 5 V
   - M2: 0 (GND)
   - M1: 1 (DV_{DD})
   - N2: 1 (DV_{DD})
   - N1: 1 (DV_{DD})
2. Connect a 50 Ω terminator to J5.

Step 2: Power Up the Evaluation Board

Turn the on switch (SW 1) to the on position. The power LED should come on.

Step 3: Measure the Following Voltages

- J6: +3.0 V
- J7: +5.0 V
- J8: +12.0 V

Step 4: Check the R Counter

1. Apply a 40 MHz, −5 dBm signal to J1 using one BNC to SMA cable from the signal generator.
2. Measure the output frequency at J3 using an oscilloscope or a frequency counter. The output frequency should be 10 MHz.
3. Disconnect the signal generator.

Step 5: Check the N Counter

1. Change M2 to 1 and M1 to 0.
2. Apply a 640 MHz, −4 dBm signal to J1 using one BNC to SMA cable from the signal generator.
3. Measure the output frequency at J3 using an oscilloscope or a frequency counter. The output frequency should be 10 MHz.

EVALUATION BOARD SCHEMATICS

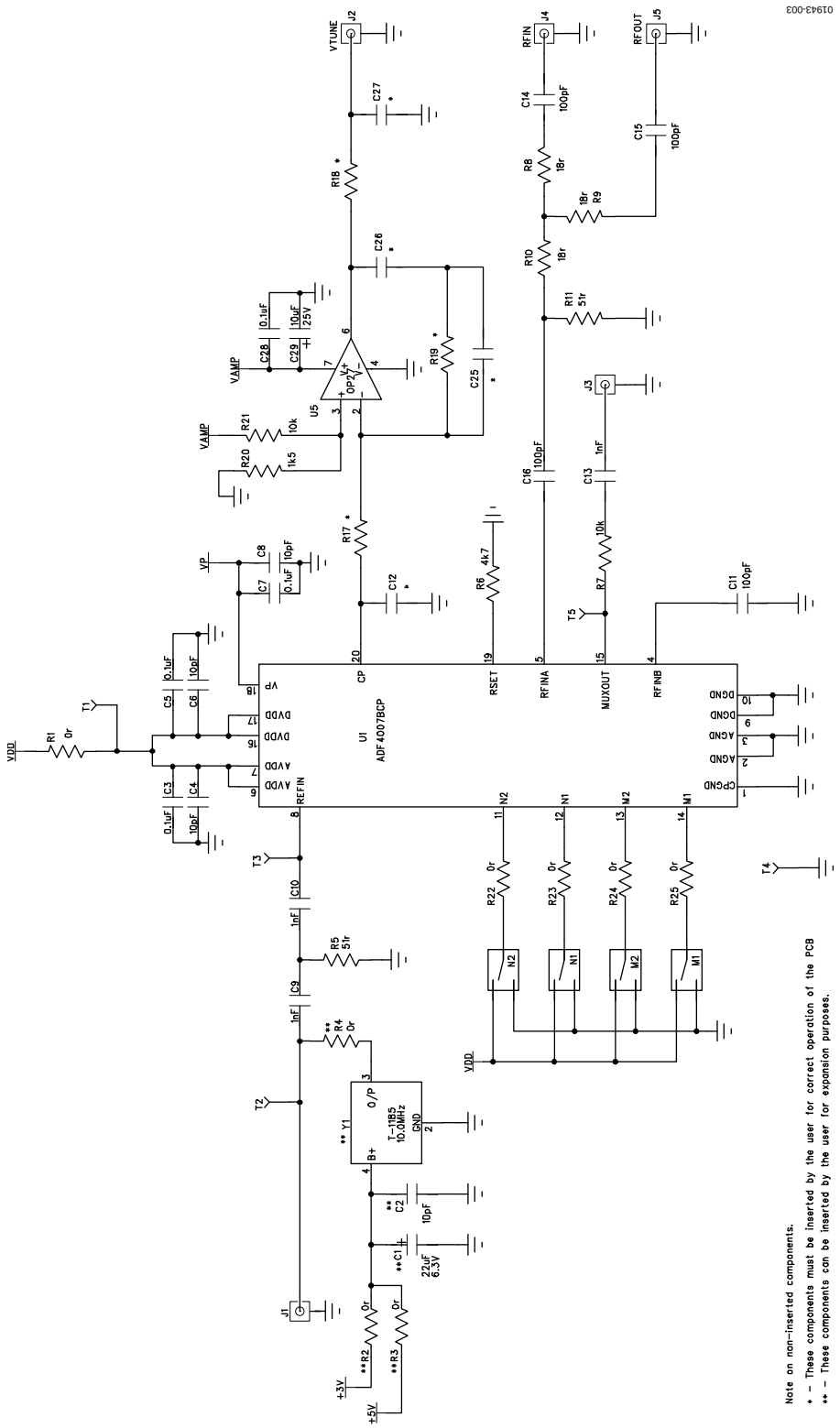

Figure 3. EVAL-ADF4007EBZ1 Schematic

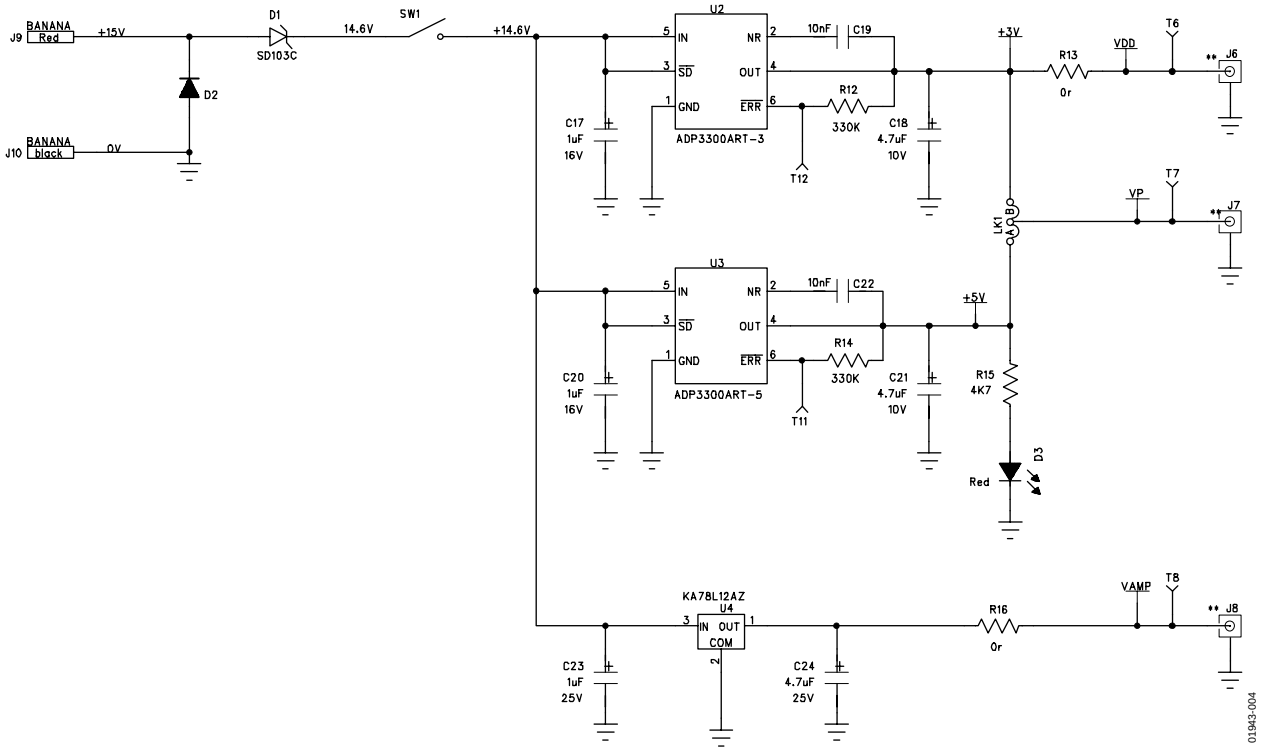

Figure 4. EVAL-ADF4007EBZ1 Schematic (Continued)

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Reference Designator	Part Description	Manufacturer/Part No.
C1	Capacitor+, 22 µF, 6.3 V, CAP\TAJ_A	FEC 197-038
C2, C4, C6, C8	Capacitor, 10 pF, 0603	FEC 499-110
C3, C5, C7, C28	Capacitor, 0.1 µF, 0603	FEC 499-675
C9, C10, C13 to C16	Capacitor, 1 nF, 0603	FEC 317-202
C12	Capacitor, 0603	
C17, C20, C23	Capacitor+, 1 µF, 25 V, CAP\TAJ_A	FEC 197-476
C18, C21	Capacitor+, 4.7 µF,10 V, CAP\TAJ_A	FEC 498-658
C19, C22	Capacitor, 10 nF, 0603	FEC 499-146
C24	Capacitor+, 4.7 µF, 25 V, CAP\TAJ_B	FEC 197-506
C25 to C27	Capacitor, 0603	
C29	Capacitor+, 10 µF, 25 V, CAP\TAJ_C	FEC 197-518
D1	SD103C, 6.2 V, DO35	SD103C
D2	DIODE, IN4001, DO35	FEC 365-117
D3	LED_SMT	FEC 515-620
J1 to J8	SMA_CARD_EDGE	Pasternack PE4542
J9	Banana, red	FEC 150-039
J10	Banana, black	FEC 150-040
LK1	JUMPER2\SIP3, LINK-3P	Futura JSC-16-GO
M1, M2, N1, N2	JUM_CHANGE_1, LINK-3P-NOTEXT	Futura JSC-16-GO
R1 to R4, R13, R16, R22 to R25	Resistor, 0 Ω, 0603	FEC 772-227
R5, R11	Resistor, 51 Ω, 0603	Digikey 311-51.0HCT-ND
R6	Resistor, 4.7 kΩ, 0603	FEC 911-318
R7	Resistor, 10 kΩ, 0603	FEC 911-355
R8 to R10	Resistor, 18 Ω, 0603	FEC 911-021
R12, R14	Resistor, 330 kΩ, 0603	FEC 911-537
R15	Resistor, 4.7 kΩ, 0805	FEC 911-938
R17 to R19	Resistor, 0603	
R20	Resistor, 1 kΩ, 0603	FEC 911-XXX
R21	Resistor, 10 kΩ, 0603	FEC 911-355
SW1	SW_POWER, SW_SIP-3P	FEC 150-559
T1 to T8, T11, T12	Test point	
U1	ADF4007, CSP-20	ADF4007BCP
U2	ADP3300, SOT23-6	ADP3300ART-3
U3	ADP3300, SOT23-6	ADP3300ART-5
U4	7812, TO-92	FEC 563-766
U5	OP27GS, SO8NB	OP27GS
Y1	OSC_TCXO, 10.0 MHz	

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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