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August 2015

FDMS8095AC

Dual N & P-Channel PowerTrench® MOSFET

N-Channel: 150 V, 27 A, 30 mΩ P-Channel: -150 V, -2.2 A, 1200 mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 30 mΩ at V_{GS} = 10 V, I_D = 6.2 A

- Max $r_{DS(on)}$ = 41 mΩ at V_{GS} = 6 V, I_D = 5.2 A
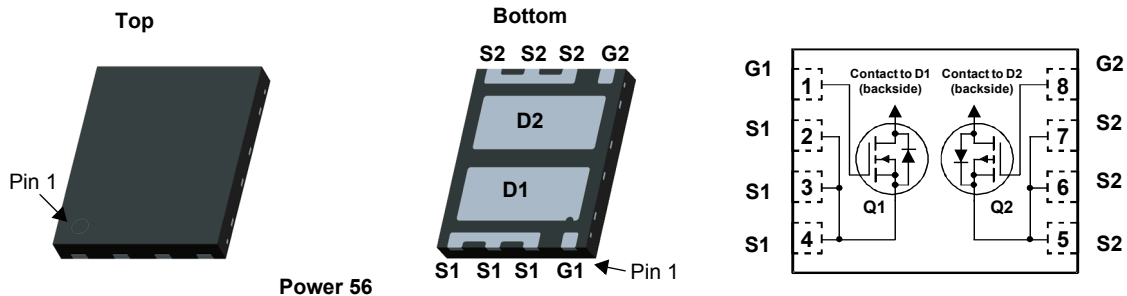
Q2: P-Channel

- Max $r_{DS(on)}$ = 1200 mΩ at V_{GS} = -10 V, I_D = -1 A

- Max $r_{DS(on)}$ = 1400 mΩ at V_{GS} = -6 V, I_D = -0.9 A

- Optimised for active clamp forward converters

- RoHS Compliant

General Description

These dual N and P-Channel enhancement mode Power MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance. Shrinking the area needed for implementation of active clamp topology; enabling best in class power density.

Applications

- DC-DC Converter

- Active Clamp

Top

Bottom

Pin 1

Power 56

S2 S2 S2 G2

D2

D1

S1 S1 S1 G1 ← Pin 1

G1	1	Contact to D1 (backside)	Contact to D2 (backside)	8	G2
S1	2			7	S2
S1	3	Q1	Q2	6	S2
S1	4			5	S2

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Q1	Q2	Units
V_{DS}	Drain to Source Voltage			150	-150	V
V_{GS}	Gate to Source Voltage			±20	±25	V
I_D	Drain Current -Continuous	T_C = 25 °C	(Note 5)	27	-2.2	A
	Drain Current -Continuous	T_C = 100 °C	(Note 5)	17	-1.4	
	-Continuous	T_A = 25 °C		6.2 [1a]	-1 [1b]	
	-Pulsed		(Note 4)	143	-8.8	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	216	6	mJ
P_D	Power Dissipation for Single Operation	T_A = 25 °C		2.3 [1a]	2.3 [1b]	W
	Power Dissipation for Single Operation	T_A = 25 °C		0.9 [1c]	0.9 [1d]	
	Power Dissipation for Single Operation	T_C = 25 °C		50	12.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	55 [1a]	55 [1b]	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	138 [1c]	138 [1d]	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.5	10	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8095AC	FDMS8095AC	Power 56	13"	12 mm	3000 units

Electrical Characteristics T$_J$ = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV$_{DSS}$	Drain to Source Breakdown Voltage	I$_D$ = 250 μA, V$_{GS}$ = 0 V I$_D$ = -250 μA, V$_{GS}$ = 0 V	Q1 Q2	150 -150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I$_D$ = 250 μA, referenced to 25 °C I$_D$ = -250 μA, referenced to 25 °C	Q1 Q2		103 122		mV/°C
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$ = 120 V, V$_{GS}$ = 0 V V$_{DS}$ = -120 V, V$_{GS}$ = 0 V	Q1 Q2			1 -1	μA
I$_{GSS}$	Gate to Source Leakage Current	V$_{GS}$ = ±20 V, V$_{DS}$ = 0 V V$_{GS}$ = ±25 V, V$_{DS}$ = 0 V	Q1 Q2			±100 ±100	nA nA
On Characteristics							
V$_{GS(th)}$	Gate to Source Threshold Voltage	V$_{GS}$ = V$_{DS}$, I$_D$ = 250 μA V$_{GS}$ = V$_{DS}$, I$_D$ = -250 μA	Q1 Q2	2.0 -2.0	3.2 -3.2	4.0 -4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I$_D$ = 250 μA, referenced to 25 °C I$_D$ = -250 μA, referenced to 25 °C	Q1 Q2		-11 -6		mV/°C
r$_{DS(on)}$	Static Drain to Source On Resistance	V$_{GS}$ = 10 V, I$_D$ = 6.2 A V$_{GS}$ = 6 V, I$_D$ = 5.2 A V$_{GS}$ = 10 V, I$_D$ = 6.2 A, T$_J$ = 125 °C	Q1		25 33 48	30 41 58	mΩ
		V$_{GS}$ = -10 V, I$_D$ = -1 A V$_{GS}$ = -6 V, I$_D$ = -0.9 A V$_{GS}$ = -10 V, I$_D$ = -1 A, T$_J$ = 125 °C	Q2		840 940 1520	1200 1400 2171	
g$_{FS}$	Forward Transconductance	V$_{DD}$ = 10 V, I$_D$ = 6.2 A V$_{DD}$ = -10 V, I$_D$ = -1 A	Q1 Q2		19 0.75		S
Dynamic Characteristics							
C$_{iss}$	Input Capacitance	Q1 V$_{DS}$ = 75 V, V$_{GS}$ = 0 V, f = 1 MHZ	Q1 Q2		1441 162	2020 230	pF
C$_{oss}$	Output Capacitance	Q2	Q1 Q2		127 13	180 25	pF
C$_{rss}$	Reverse Transfer Capacitance	V$_{DS}$ = -75 V, V$_{GS}$ = 0 V, f = 1 MHZ	Q1 Q2		4.4 0.6	10 5	pF
R$_g$	Gate Resistance		Q1 Q2	0.1 0.1	1.3 3.3	3.3 8.3	Ω
Switching Characteristics							
t$_{d(on)}$	Turn-On Delay Time	Q1 V$_{DD}$ = 75 V, I$_D$ = 6.2 A, V$_{GS}$ = 10 V, R$_{GEN}$ = 6 Ω	Q1 Q2		12 5.2	22 11	ns
t$_r$	Rise Time		Q1 Q2		2.7 1.6	10 10	ns
t$_{d(off)}$	Turn-Off Delay Time	Q2 V$_{DD}$ = -75 V, I$_D$ = -1 A, V$_{GS}$ = -10 V, R$_{GEN}$ = 6 Ω	Q1 Q2		18 7.4	33 15	ns
t$_f$	Fall Time		Q1 Q2		4 6.3	10 13	ns
Q$_{g(TOT)}$	Total Gate Charge	V$_{GS}$ = 0 V to 10 V V$_{GS}$ = 0 V to -10 V	Q1 V$_{DD}$ = 75 V, I$_D$ = 6.2 A	Q1 Q2		21 2.8	30 4	nC
Q$_{g(TOT)}$	Total Gate Charge	V$_{GS}$ = 0 V to 6 V V$_{GS}$ = 0 V to -6 V		Q1 Q2		13 1.8	19 2.6	nC
Q$_{gs}$	Gate to Source Charge		Q2 V$_{DD}$ = -75 V I$_D$ = -1 A	Q1 Q2		6.7 0.8		nC
Q$_{gd}$	Gate to Drain "Miller" Charge			Q1 Q2		3.9 0.7		nC

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 6.2 A (Note 2) V_{GS} = 0 V, I_S = -1 A (Note 2)	Q1 Q2		0.8 -0.9	1.3 -1.3	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 6.2 A, di/dt = 100 A/s	Q1 Q2		69 44	111 71	ns
Q_{rr}	Reverse Recovery Charge	Q2 I_F = -1 A, di/dt = 100 A/s	Q1 Q2		106 68	170 109	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.
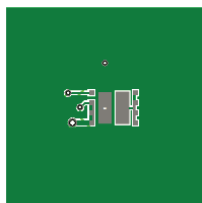
a. 55 °C/W when mounted on a 1 in² pad of 2 oz copper
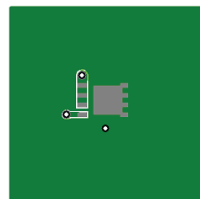
b. 55 °C/W when mounted on a 1 in² pad of 2 oz copper
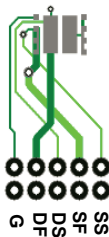
c. 138 °C/W when mounted on a minimum pad of 2 oz copper
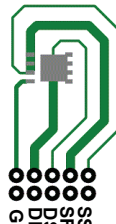
d. 138 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Q1: E_{AS} of 216 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 12 A, V_{DD} = 150 V, V_{GS} = 10 V. 100% test at L = 0.3 mH, I_{AS} = 28 A.

   Q2: E_{AS} of 6 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = -2 A, V_{DD} = -150 V, V_{GS} = -10 V. 100% test at L = 0.3 mH, I_{AS} = -6.9 A.

4. Pulsed Id please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted
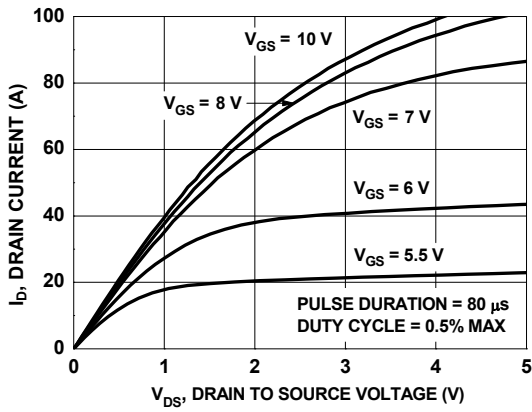
Figure 1. On Region Characteristics
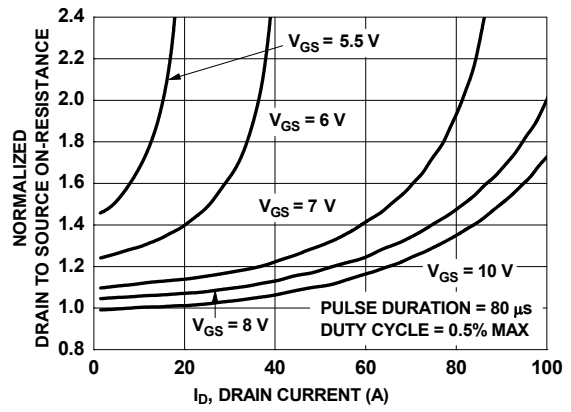
Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage
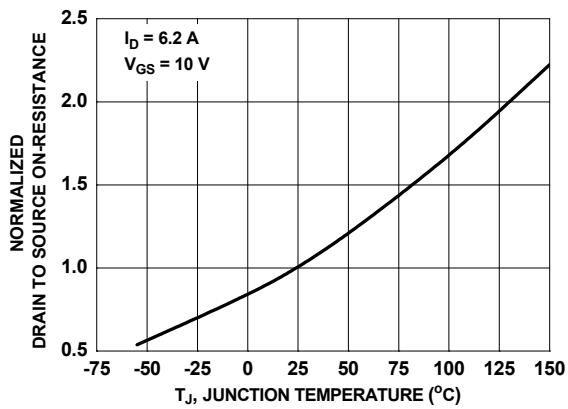
Figure 3. Normalized On Resistance vs Junction Temperature
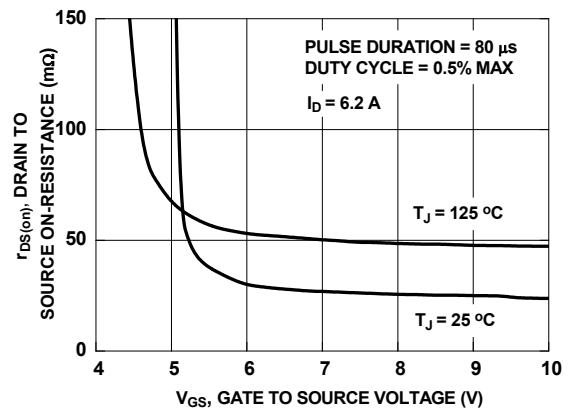
Figure 4. On-Resistance vs Gate to Source Voltage
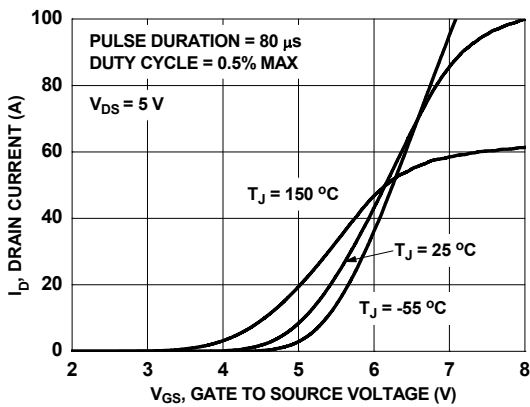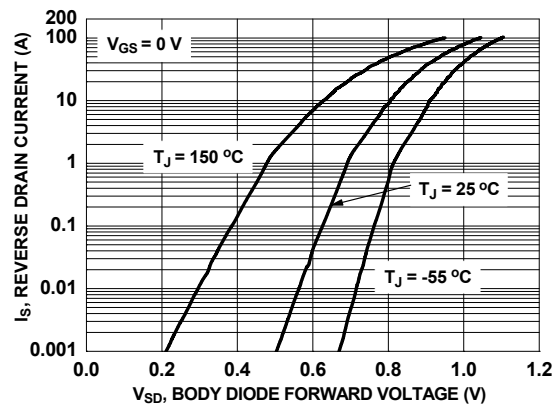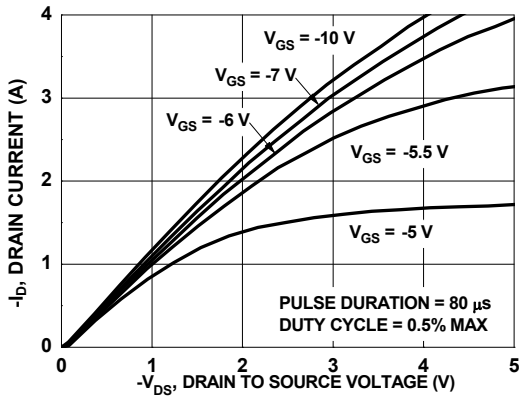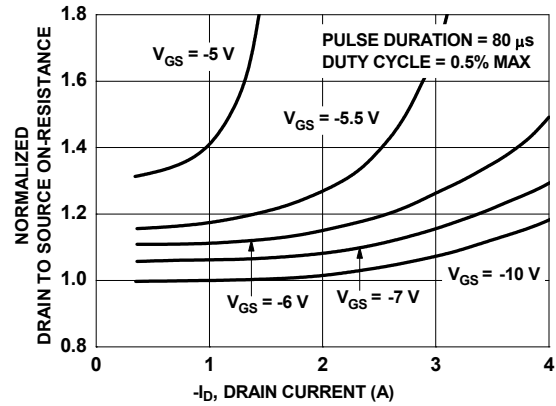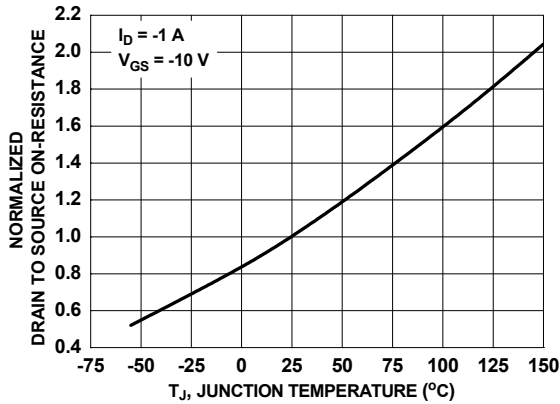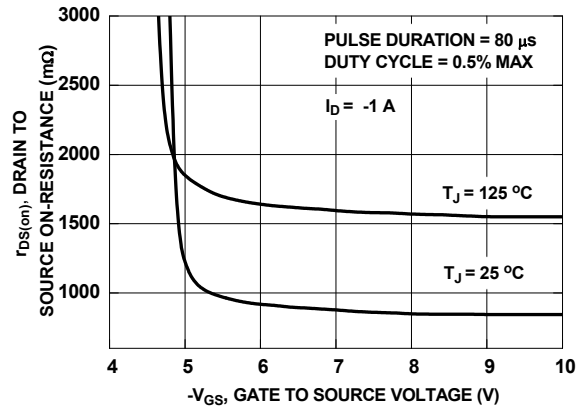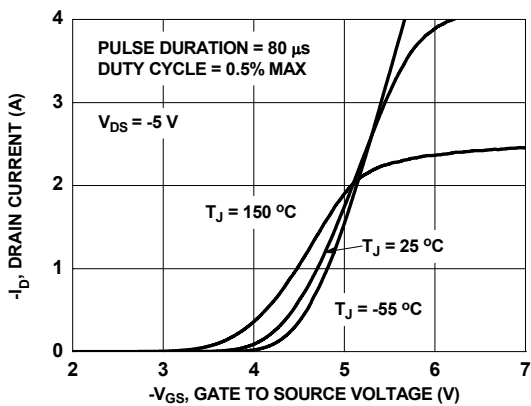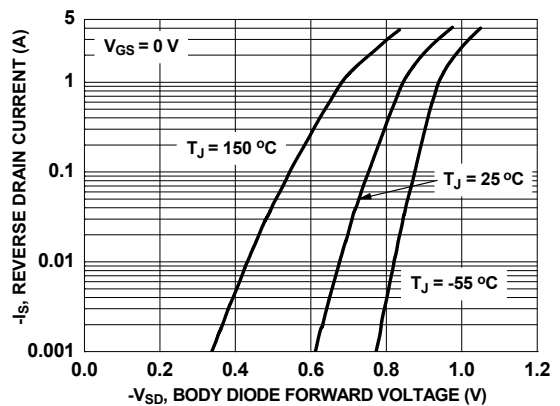
Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted
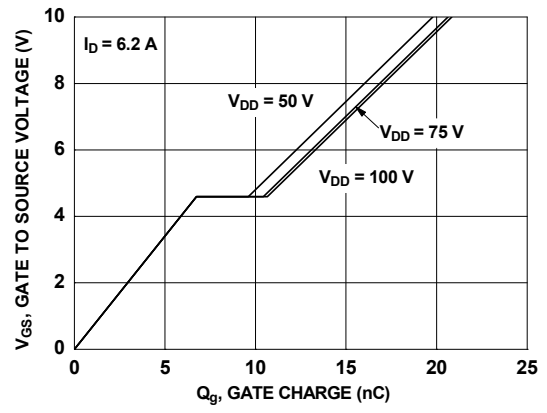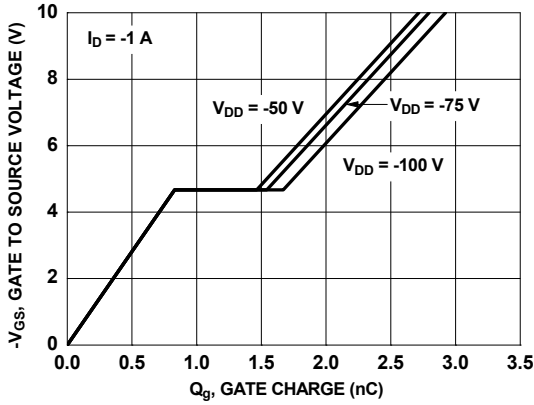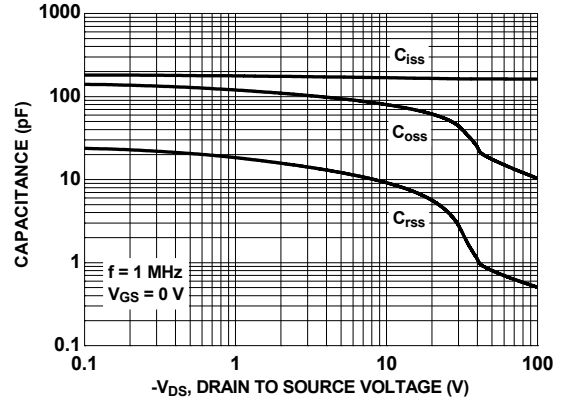
Figure 7. Gate Charge Characteristics
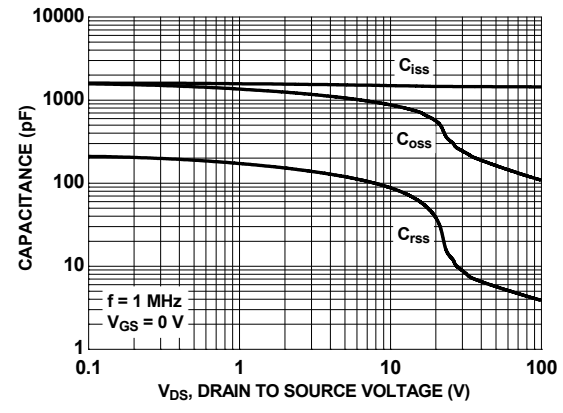
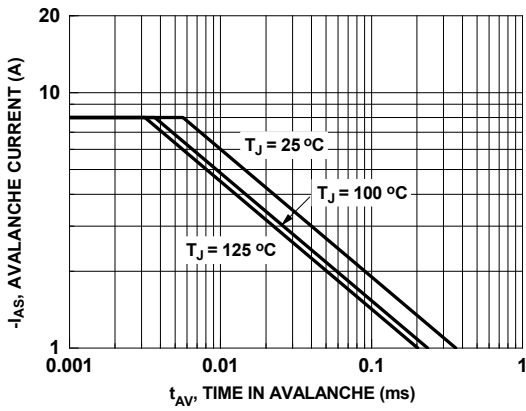**Figure 8. Capacitance vs Drain to Source Voltage**
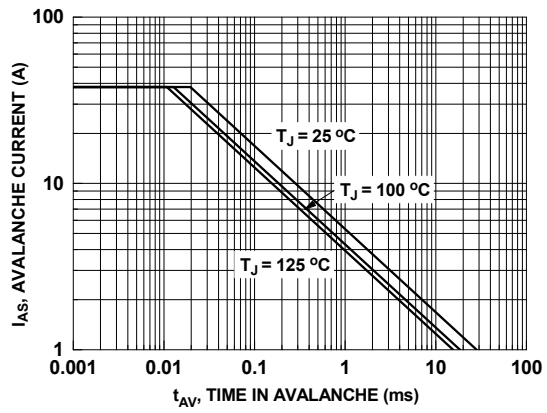
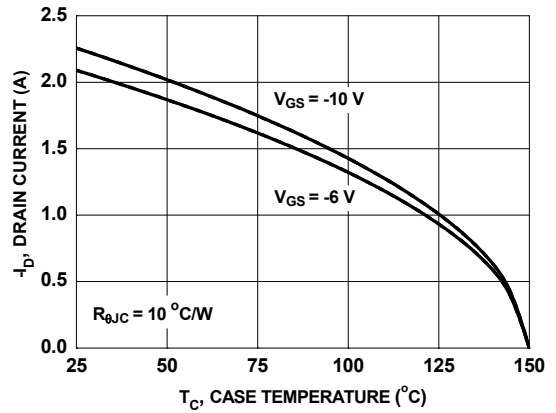**Figure 9. Unclamped Inductive Switching Capability**
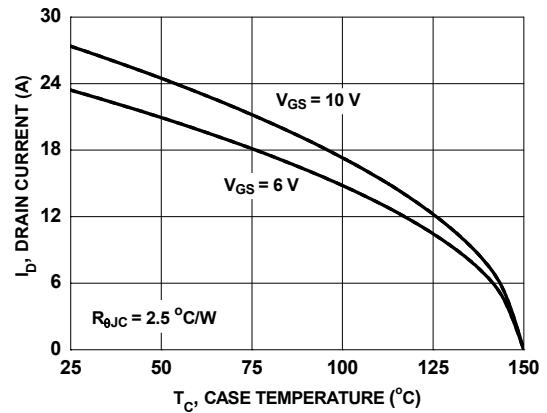
Figure 10. Maximum Continuous Drain Current vs Case Temperature
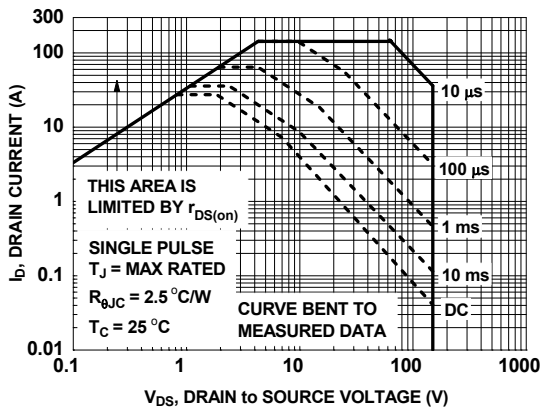
Figure 11. Forward Bias Safe Operating Area
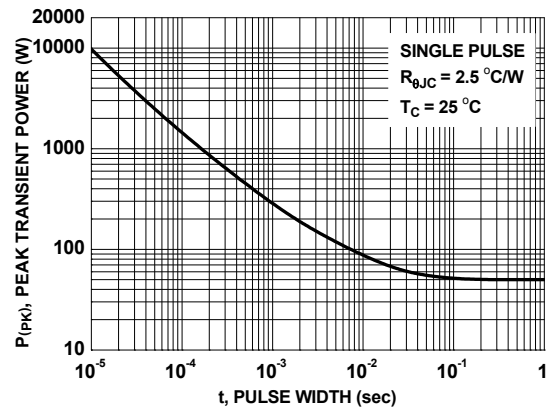
Figure 12. Single Pulse Maximum Power Dissipation

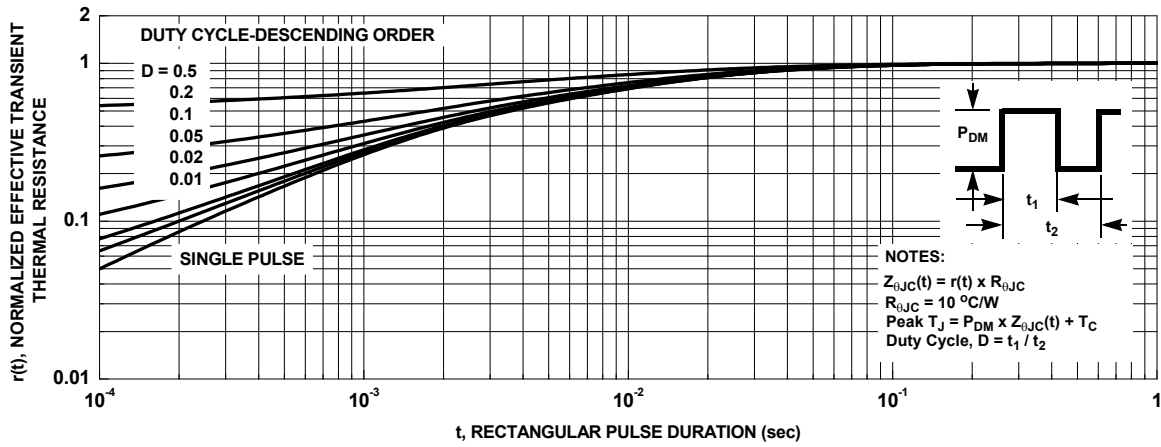## Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

DUTY CYCLE-DESCENDING ORDER

D = 0.5
0.2
0.1
0.05
0.02
0.01

SINGLE PULSE

r(t), NORMALIZED EFFECTIVE TRANSIENT THERMAL RESISTANCE

t, RECTANGULAR PULSE DURATION (sec)

NOTES:
$Z_{\theta JC}(t) = r(t) \times R_{\theta JC}$
$R_{\theta JC} = 2.5\ ^oC/W$
Peak $T_J = P_{DM} \times Z_{\theta JC}(t) + T_C$
Duty Cycle, $D = t_1 / t_2$
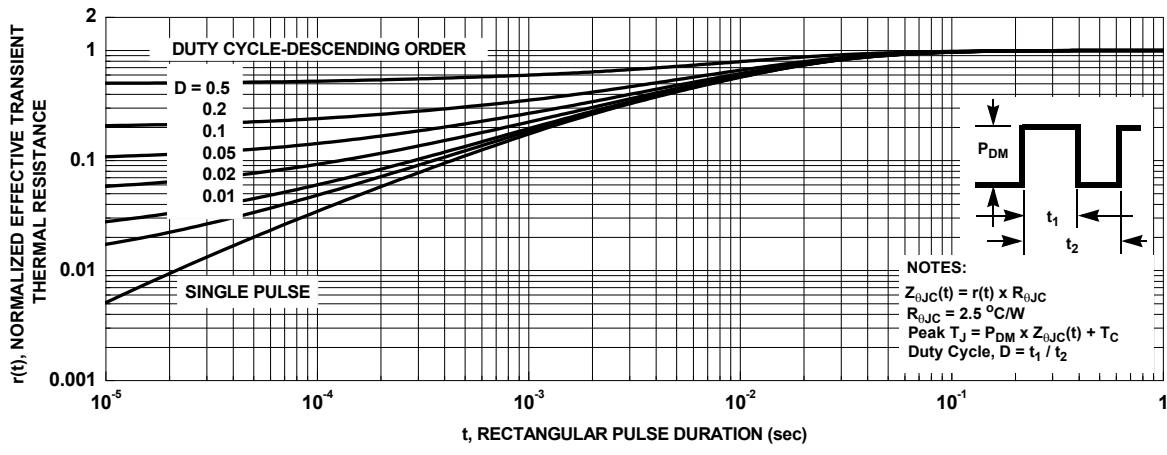
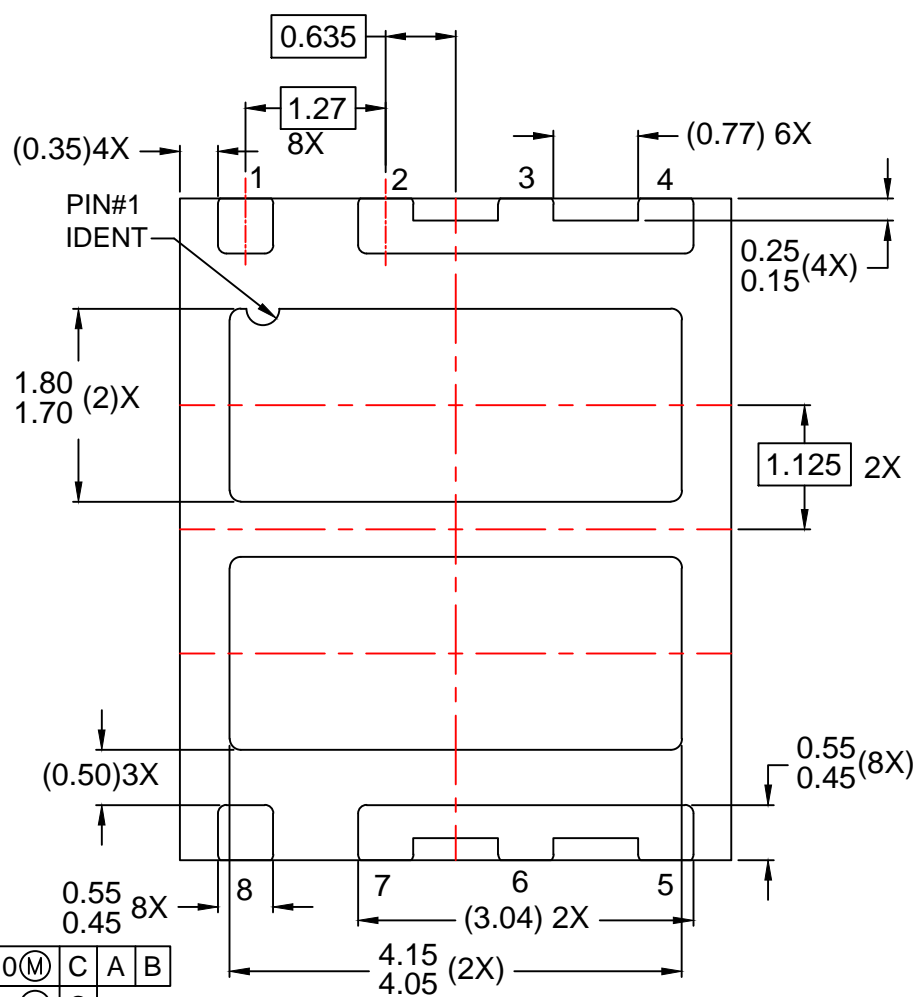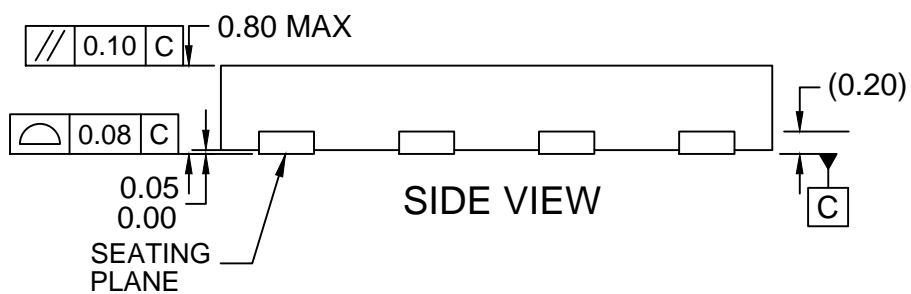**Figure 13. Junction-to-Case Transient Thermal Response Curve**

FDMS8095AC Rev.1.0

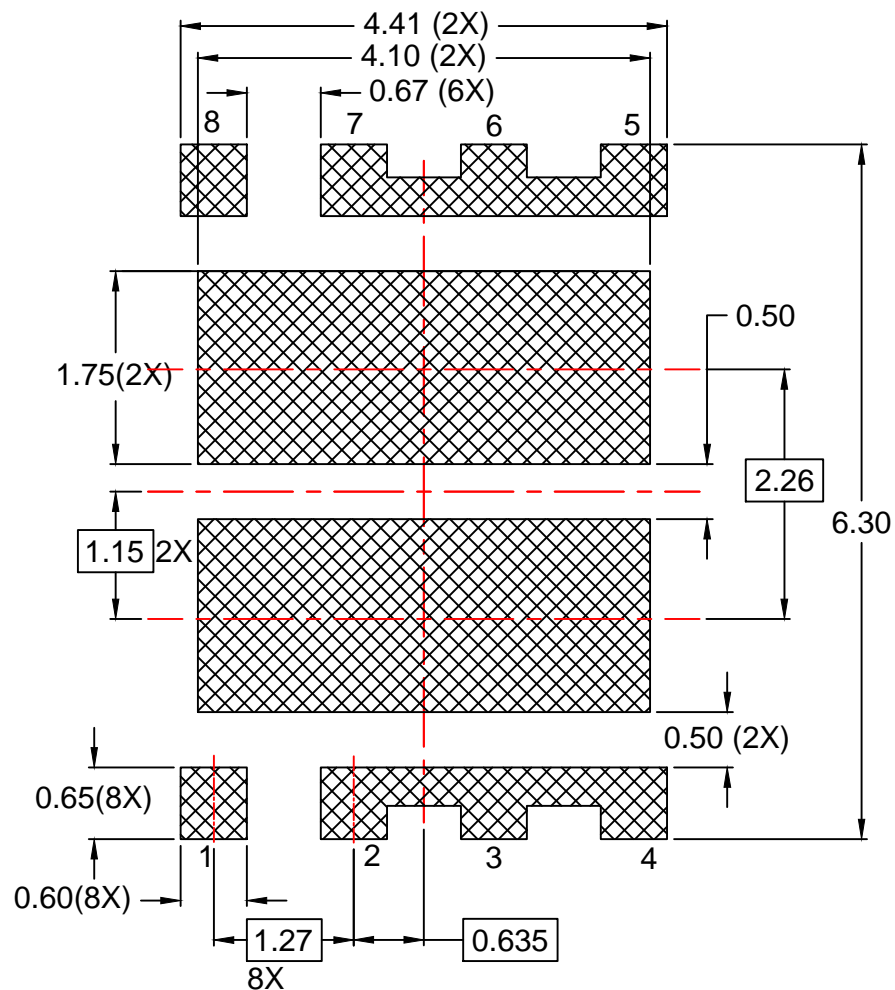## Typical Characteristics (Q2 P-Channel) T_J = 25 °C unless otherwise noted

Figure 14. On- Region Characteristics

Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

Figure 16. Normalized On-Resistance vs Junction Temperature

Figure 17. On-Resistance vs Gate to Source Voltage

Figure 18. Transfer Characteristics

Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 P-Channel) T_J = 25°C unless otherwise noted

Figure 20. Gate Charge Characteristics

Figure 21. Capacitance vs Drain to Source Voltage

Figure 22. Unclamped Inductive Switching Capability

Figure 23. Maximum Continuous Drain Current vs Case Temperature
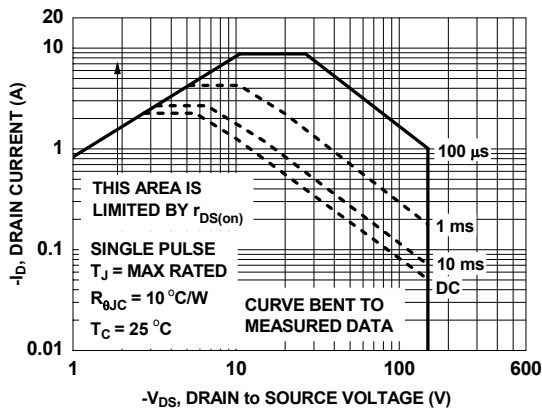
Figure 24. Forward Bias Safe Operating Area
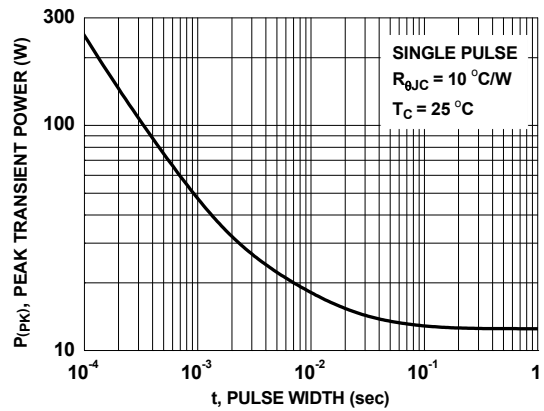
Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 P-Channel) T_J = 25 °C unless otherwise noted

Figure 26. Junction-to-Case Transient Thermal Response Curve

TOP VIEW

0.10 C 2X

5.00

A

B

6.00

PIN#1 IDENT

0.10 C 2X

SIDE VIEW

0.10 C

0.80 MAX

0.08 C

(0.20)

0.05
0.00

SEATING PLANE

C

BOTTOM VIEW

0.635

1.27
8X

(0.35)4X

PIN#1 IDENT

1 2 3 4

(0.77) 6X

0.25
0.15 (4X)

1.80
1.70 (2)X

1.125 2X

(0.50)3X

0.55
0.45 (8X)

0.55
0.45 8X

8 7 6 5

(3.04) 2X

4.15
4.05 (2X)

0.10 Ⓜ C A B
0.05 Ⓜ C

RECOMMENDED LAND PATTERN

4.41 (2X)
4.10 (2X)
0.67 (6X)

8 7 6 5

1.75(2X)

0.50

2.26

6.30

1.15 2X

0.50 (2X)

0.65(8X)

0.60(8X)

1 2 3 4

1.27
8X

0.635
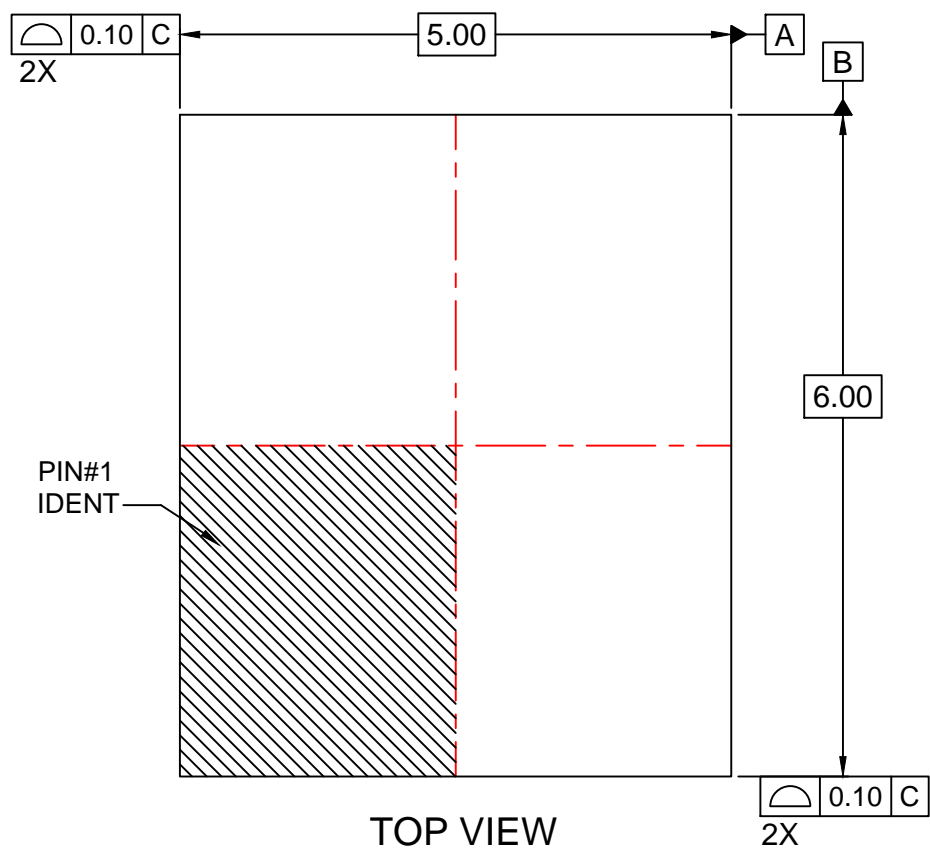
NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
E. DRAWING FILENAME: MKT-MLP08Zrev1.

PUBLICATION ORDERING INFORMATION