High Performance Regulators for PCs

Nch FET Ultra LDO for PC Chipsets

BD3506F,BD3506EFV

No.10030EAT30

●Description

The BD3506F/EFV is an ultra-low dropout linear regulator for chipset that can achieve ultra-low voltage input to ultra-low voltage output. By using N-MOS FET for built-in power transistor, the regulator can be used at ultra-low I/O voltage difference up to voltage difference generated by ON resistor (Ron = 120 mΩ/100 mΩ). Because by reducing the I/O voltage difference, large current (Iomax = 2.5A) output is achieved and conversion loss can be reduced, switching power supply can be replaced. BD3506F/EFV does not need any choke coil, diode for rectification and power transistors which are required for switching power supply, total cost of the set can be reduced and compact size can be achieved for the set. Using external resistors, optional output from 0.65V to 2.5V can be set. In addition, since voltage output start-up time can be adjusted by using the NRCS terminal, it is possible to meet the power supply sequence of the set.

●Features

1) Built-in high-accuracy reference voltage circuit (0.65V±1%)
2) Built-in VCC low input maloperation prevention circuit (Vcc = 4.15V)
3) Reduced rush current by NRCS
4) Built-in ultra-low on-resistor (120/100 mΩ typ) Nch Power MOSFET (BD3506F/BD3506EFV)
5) Built-in current limiting circuit (2.5A min)
6) Built-in thermal shutdown circuit
7) Output variable type (0.65-2.5V)
8) Adoption of SOP8 package (BD3506F): 5.0 x 6.2 x 1.5 (mm)
9) Adoption of high power HTSSOP-B20 package (BD3506EFV): 5.0 x 6.4 x 1.0 (mm)

●Applications

Mobile PC, desktop PC, LCD-TV, DVD, digital home appliances

●Line up

Parameter	BD3506F	BD3506EFV
Ron	120mΩ	100mΩ
Output Current	2.5A	2.5A
Package	SOP8	HTSSOP-B20

●Absolute Maximum Ratings(Ta=25℃)

Parameter	Symbol	Ratings		Unit
		BD3506F	BD3506EFV	
Input Voltage1	VCC	7 *1	7 *1	V
Input Voltage2	VIN	7 *1	7 *1	V
Enable Input Voltage	Ven	7	7	V
Power Dissipation1	Pd1	560 *2	-	mW
Power Dissipation2	Pd2	690 *3	1000 *4	mW
Operating Temperature Range	Topr	-10～+100	-10～+100	℃
Storage Temperature Range	Tstg	-55～+125	-55～+125	℃
Maximum Junction Temperature	Tjmax	+150	+150	℃

*1 However, not exceeding Pd.
*2 In the case of Ta≥25°C (no heat radiation board), derated at 4.48 mW/°C.
*3 In the case of Ta≥25°C (when mounting to 70mmx70mmx1.6mm glass epoxy substrate), derated at 5.52 mW/°C.
*4 In the case of Ta≥25°C (when mounting to 70mmx70mmx1.6mm glass epoxy substrate), derated at 8.00 mW/°C.

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●Recommended Operating Conditions(Ta=25℃)

Parameter	Symbol	Ratings		Unit
		MIN	MAX	
Input Voltage1	VCC	4.3	5.5	V
Input Voltage2	VIN	1.2	VCC-1 *5	V
Output Voltage	Vo	VFB	2.5	V
Enable Input Voltage	Ven	-0.3	5.5	V
Capacitor in NRCS pin	CNRCS	0.001	1	μF

*5 However, irrespective of charging order of VCC and VIN.

* No radiation-resistant design is adopted for the present product.

●Electrical Characteristics (unless otherwise noted, Ta=25 VCC=5V Ven=3V VIN=1.8V R1=3.9KΩ R2=3.3KΩ)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Bias Current	I_{CC}	-	0.7	1.4	mA	
Bias current	I_{ST}	-	0	10	μA	Ven=0V
Shut-Down Mode Current	V_{OUT}	-	1.200	-	V	Io=50mA
Output Voltage	Io	2.5	-	-	A	
Maximum Output Current	Iost	-	2.0	-	A	Vo=0V
Maximum Short Current	Tcvo	-	0.01	-	%/℃	
Temperature coefficient of Output Voltage	V_{FB1}	0.643	0.650	0.657	V	Io=50mA
Feed Back Voltage 1	V_{FB2}	0.630	0.650	0.670	V	Io=0 to 2A, Ta=-10 to 100℃*5
Feed Back Voltage 2	Reg.I1	-	0.1	0.5	%/V	VCC=4.3V to 5.5V
Line Regulation 1	Reg.I2	-	0.1	0.5	%/V	VIN=1.2V to 3.3V
Line Regulation 2	Reg.L	-	0.5	10	mV	Io=0 to 2A
Dropout Voltage (BD3506F)	dVo	-	120	200	mV	Io=1A,VIN=1.2V, Ta=-10 to 100℃*5
Dropout Voltage (BD3506EFV)	dVo	-	100	160	mV	Io=1A,VIN=1.2V, Ta=-10 to 100℃*5
Standby Discharge Current	Iden	150	-	-	mA	Ven=0V, Vo=1V
[Enable]						
High level Enable Input Voltage	Enhi	2	-	5.5	V	
Low level Enable Input Voltage	Enlow	-0.3	-	0.8	V	
Enable pin Input Current	Ien	-	7	10	μA	Ven=3V
[Voltage Feed Back]						
Feed Back terminal Bias Current	I_{FB}	-100	0	100	nA	
[NRCS]						
NRCS Charge Current	Inrcs	14	20	26	μA	Vnrcs=0.5V
NRCS Standby Voltage	V_{STB}	-	0	50	mV	Ven=0V
[UVLO]						
VCC UVLO	V_{CCUVLO}	4.00	4.15	4.30	V	Vcc:Sweep-up
VCC UVLO Hysteresis	Vcchys	100	160	220	mV	Vcc:Sweep-down

*5 Design Guarantee

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●Reference Data

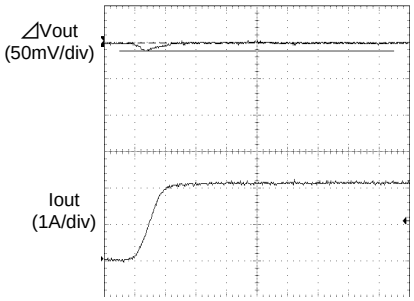

Fig.1 Transient Response

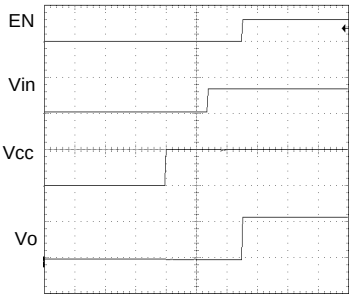

Fig.2 Input Voltage SequenceFinal Input Voltage EN

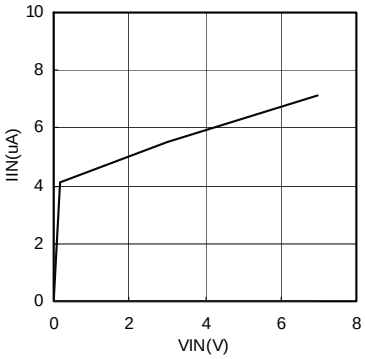

Fig.3 VIN-IIN(Ta=25℃)

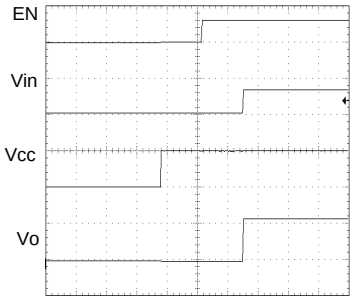

Fig.4 Input Voltage SequenceFinal Input Voltage VIN

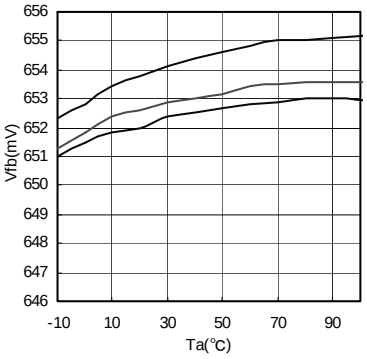

Fig.5 Ta-Vfb

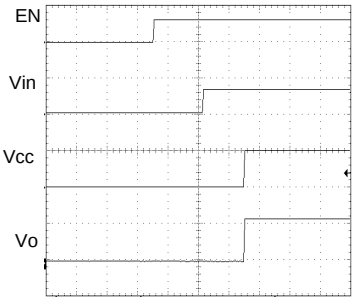

Fig.6 Input Voltage SequenceFinal Input Voltage VCC

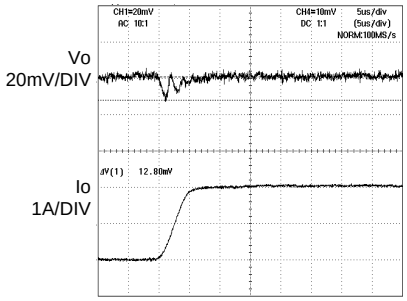

Fig.7 Transient Response (rise) Cout=100uF

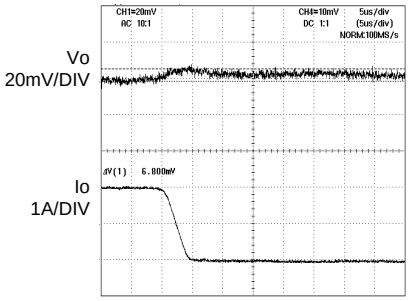

Fig.8 Transient Response (fall) Cout=100uF

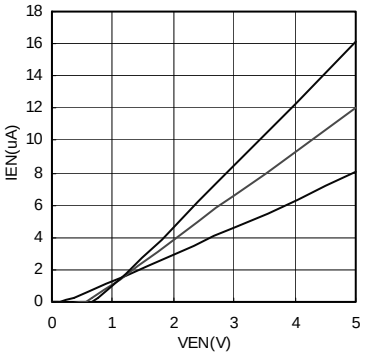

Fig.9 VEN-IEN

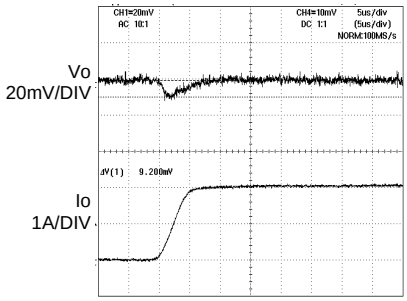

Fig.10 Transient Response (rise) Cout=220uF

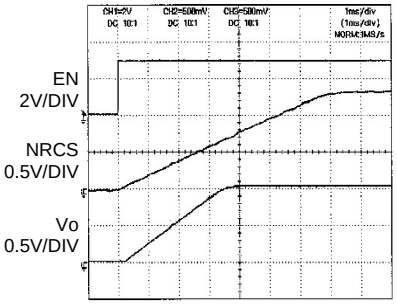

Fig.11 Start up Wave Form

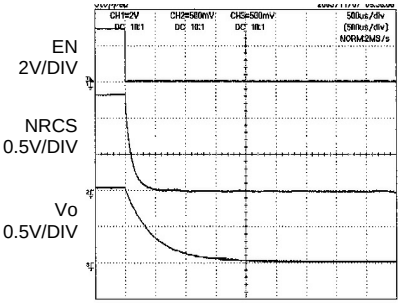

Fig.12 Shut down Wave Form

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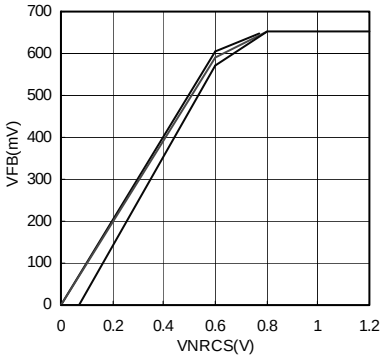

Fig.13 VNRCS-VFB

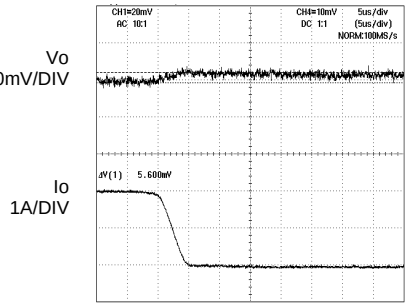

Fig.14 Transient Response (fall)
Cout=220uF

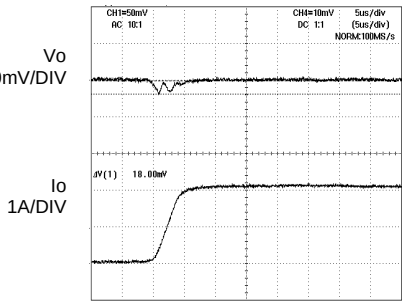

Fig.15 Transient Response (rise)
47u MLCC+30mΩ

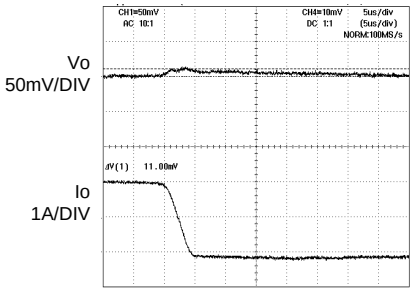

Fig.16 Transient Response (fall)
47u MLCC+30mΩ

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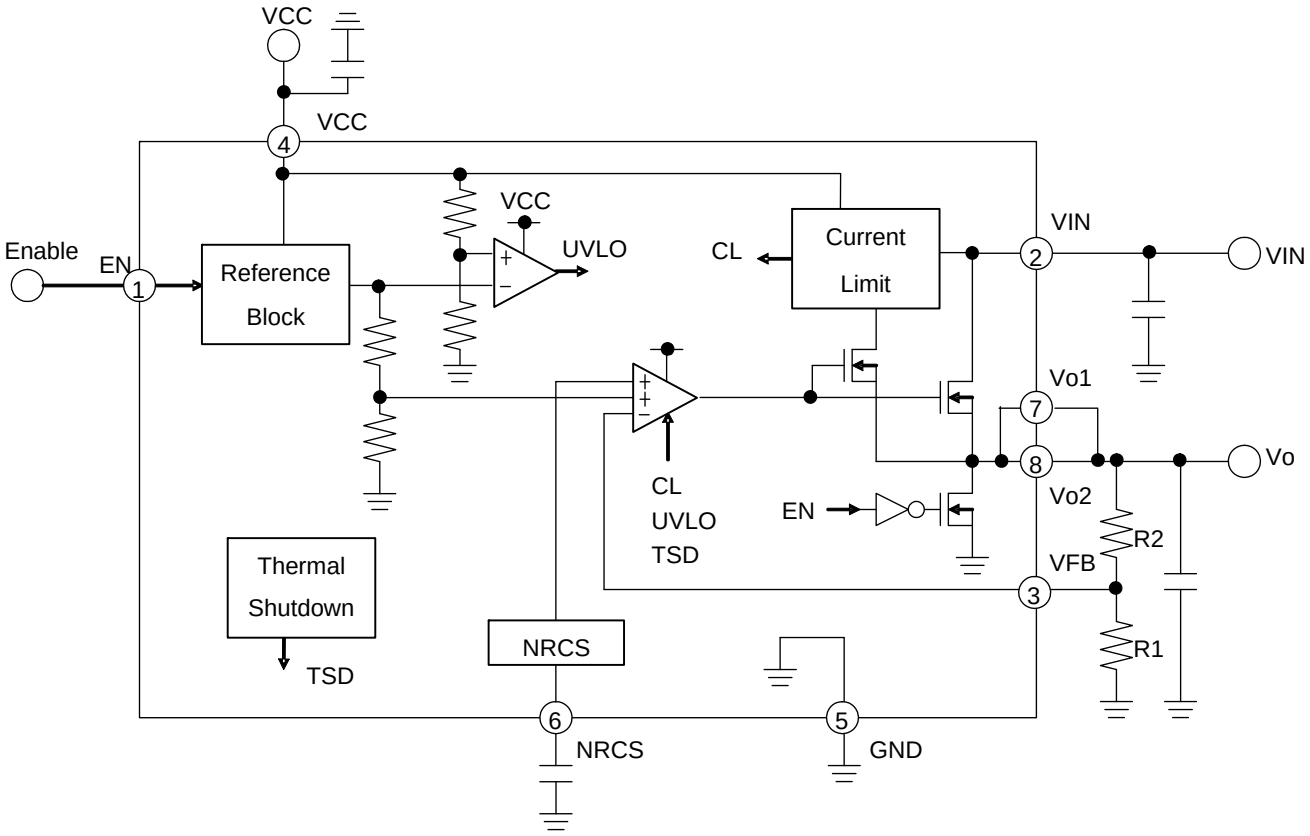
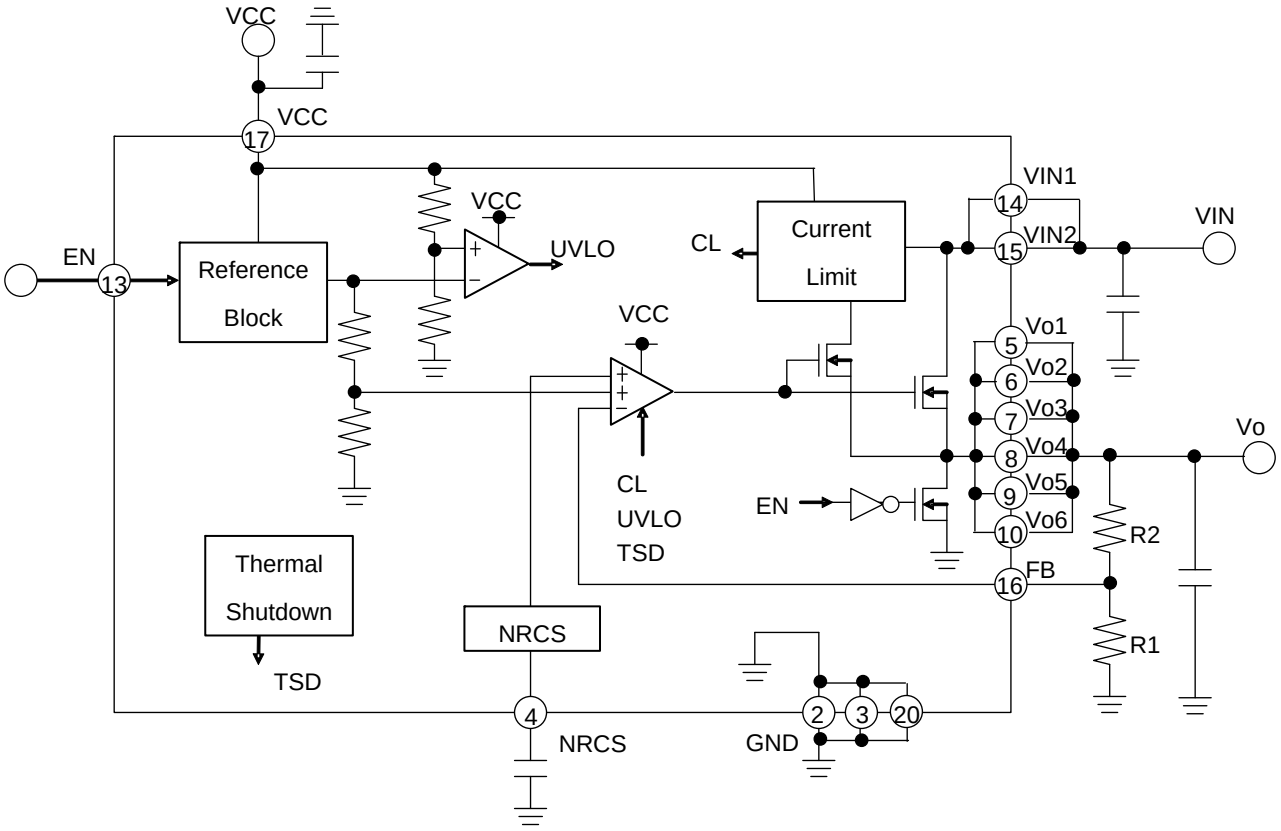
●Block Diagram

◎BD3506F



◎BD3506EFV



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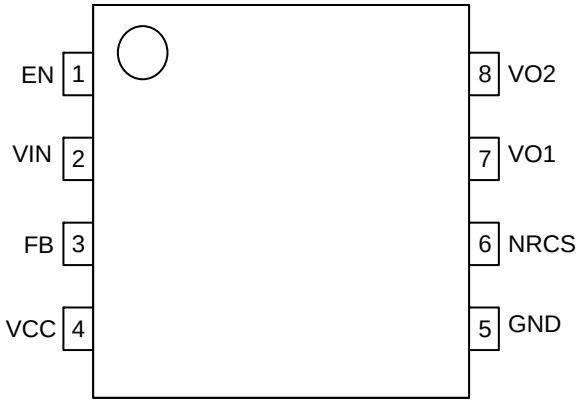
●Pin Configration and Pin Function

◎BD3506F

○Pin Configration

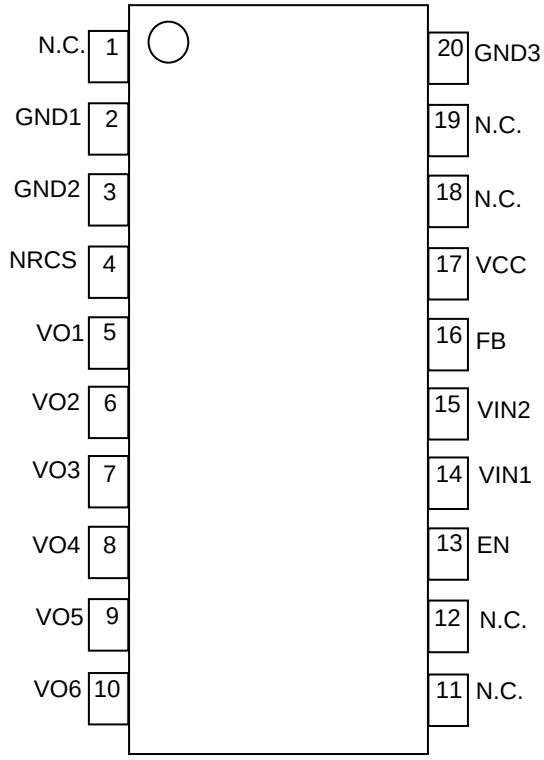


○Pin Function

Pin No.	Pin Name	PIN FUNCTION
1	EN	Enable Pin
2	VIN	Input Voltage Pin
3	FB	Output Voltage Feedback
4	VCC	Power Source
5	GND	Ground Pin
6	NRCS	NRCS(Non Rush Current on Start Up) time setup
7	VO1	VO1 Pin
8	VO2	VO2 Pin

◎BD3506EFV

○Pin Configration



○Pin Function

PIN No.	PIN Name	PIN FUNCTION
1	N.C.	Non connection
2	GND1	Ground1 Pin
3	GND2	Ground2 Pin
4	NRCS	NRCS(Non Rush Current on Start Up) time setup
5	VO1	VO1 Pin
6	VO2	VO2 Pin
7	VO3	VO3 Pin
8	VO4	VO4 Pin
9	VO5	VO5 Pin
10	VO6	VO6 Pin
11	N.C.	Non connection
12	N.C.	Non connection
13	EN	Enable Pin
14	VIN1	Input Voltage1 Pin
15	VIN2	Input Voltage2 Pin
16	FB	Output Voltage Feedback
17	VCC	Power Source
18	N.C.	Non connection
19	N.C.	Non connection
20	GND3	Ground3 Pin

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●Block Function

- AMP

  An error amplifier that compares reference voltage (VREF) to Vo and drives Nch FET (Ron = 120/100 mΩ) of output. The frequency characteristics are optimized so that low ESR functional polymer capacitor can be used for the output capacitor and high-speed transient response can be achieved. The input voltage range at the AMP section is GND-2.5V and the output voltage range of the AMP section is GND-VCC. At the time of EN OFF or UVLO, the output is brought to the LOW level and the output NchFET is turned OFF.

- EN

  By the logic input pin, regulator ON/OFF is controlled. At the time of OFF, the circuit current is controlled to be 0 μA to reduce the standby current consumption of the apparatus. In addition, EN turns ON FET that can discharge NRCS terminal Vo and removes excess electric charge to prevent maloperation of IC on the load side. Since there is no electrical connection with the Vcc terminal as is the case of Di for electrostatic measures, it does not depend on the input sequence.

- UVLO

  UVLO turned OFF output to prevent output voltage from making maloperation at the time of Vcc reduced voltage. Same as EN, UVLO discharges NRCS Vo. When voltage exceeds the threshold voltage (TYP 4.15V), UVLO starts output.

- CURRENT LIMIT

  In the event the output current that exceeds the current (2.5A or more) set inside the IC flows when output is turned ON, output voltage is attenuated to protect the IC on the load side. When current reduces, output voltage returns to the set voltage.

- NRCS

  Connecting an external capacitor to the counter-GND of NRCS pin can achieve soft start. The output voltage startup time is determined by the time when the NRCS terminal reaches VFB (0.65V). During start-up, the NRCS terminal serves as a constant current source of 20 μA (Typ.) output, and charges the capacitor externally connected.

- TSD (Thermal Shut down)

  In order to prevent thermal breakdown and thermal runaway of the IC, the output is turned OFF when chip temperature becomes high. In addition, when temperature returns to the specified temperature, the output is recovered. However, since the temperature protection circuit is originally built in to protect the IC itself, thermal design within Tj(max) is requested.

- VIN

  This is a large-current supply line. The VIN terminal is connected to the rain of output NchFET. Since there is no electrical connection with the Vcc terminal as is the case of Di for electrostatic measures, it does not depend on the input sequence. However, because there is body Di of output NchFET between VIN and Vo, there is electrical connection (Di-connection) between VIN and Vo. Consequently, when the output is turned ON/OFF by VIN, reverse current flows from Vo to VIN, to which care must be taken.

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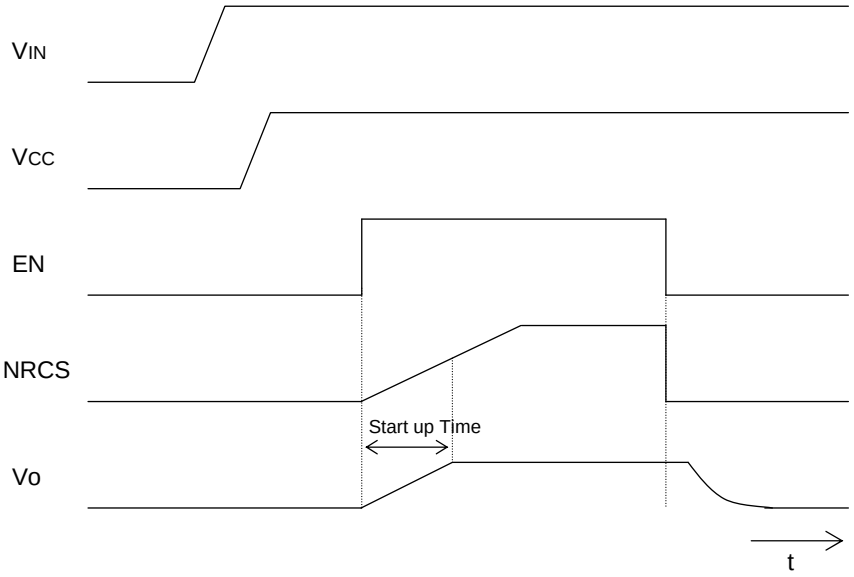
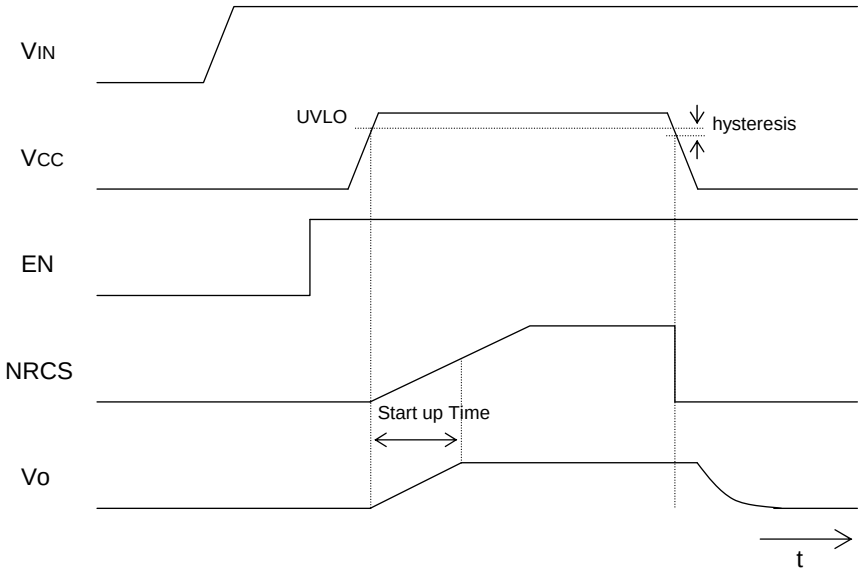
●**Timing Chart**

EN ON/OFF



V_{CC} ON/OFF



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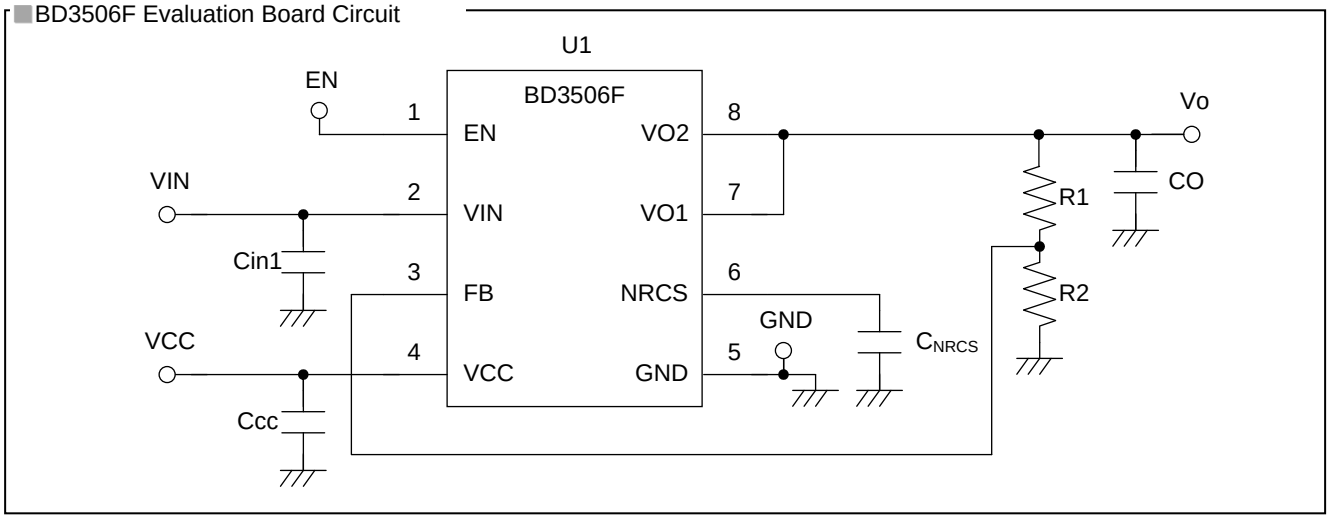
●Evaluation Board

■BD3506F Evaluation Board Circuit



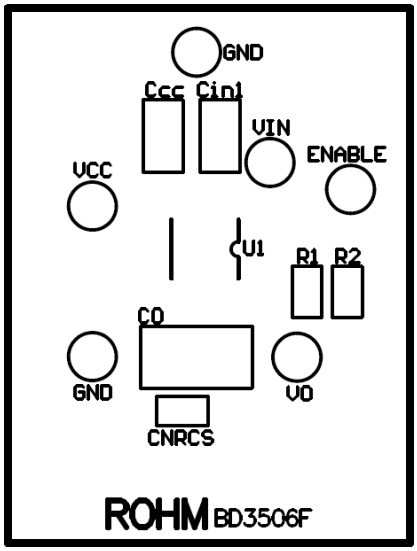
■BD3506F Evaluation Board Application Components

Part No	Value	Company	Parts Name
U1	-	ROHM	BD3506F
R1	3.3k	ROHM	MCR03Series
R2	3.9k	ROHM	MCR03Series

Part No	Value	Company	Parts Name
Ccc	1μF	MURATA	GRM18 Series
Cin1	10μF	MURATA	GRM21 Series
Co	220μF	SANYO,etc	2R5TPE220MF
C6	0.01μF	MURATA	GRM18 Series

■BD3506F Evaluation Board Layout

Silk Screen



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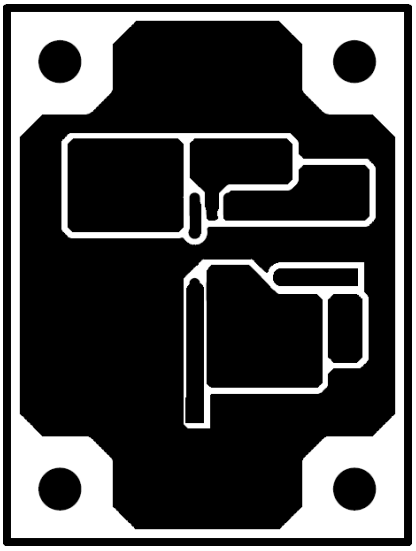

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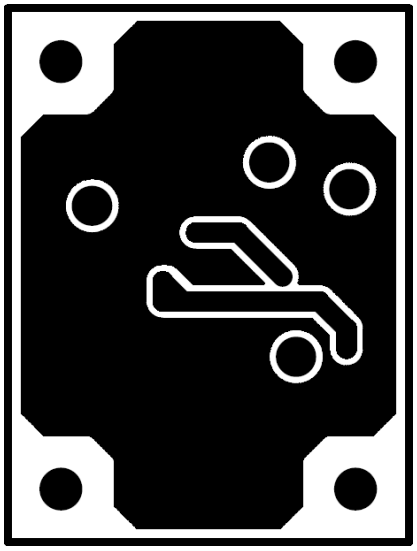

For Evaluation Board, BD3506EFV is available.

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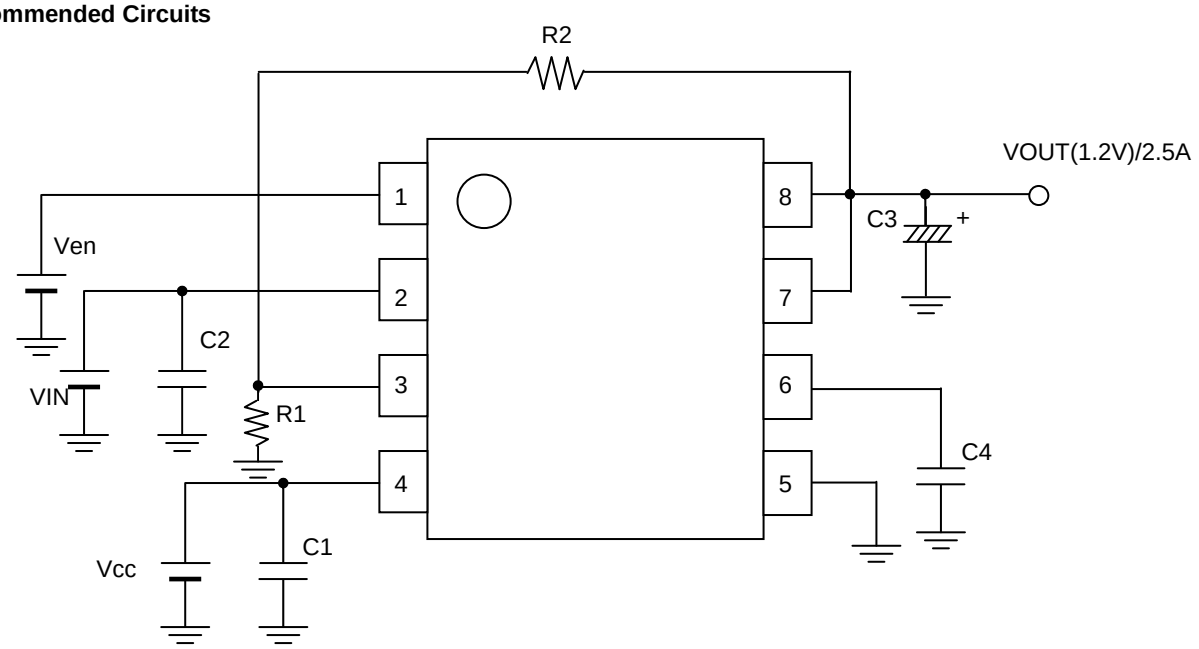
●**Recommended Circuits**



Part No	Value	Notes for use
R1/R2	6.5k/5.5k	The present IC can set output voltage by external reference voltage (VR) and value of output voltage setting resistors (R1, R2). Output voltage can be set by VRxR2/(R1+R2) but it is recommended to use at the resistance value (total: about 10 kΩ) which is not susceptible to VREF bias current (±100 nA).
C3	100µF	Connect the output capacitor between Vo1, Vo2 terminals and GND terminal without fail in order to stabilize output voltage. The output capacitor has a role to compensate for the phase of loop gain and to reduce output voltage fluctuation when load is rapidly changed. When there is an insufficient capacity value, there is a possibility to cause oscillation, and when the equivalent serial resistance (ESR) of the capacitors is large, output voltage fluctuation is increased when load is rapidly changed. About 100-µF high-performance electrolytic capacitors are recommended but output capacitor greatly depends on temperature and load conditions. In addition, when only ceramic capacitors with low ESR are used, or various capacitors are connected in series, the total phase allowance of loop gain becomes not sufficient, and oscillation may result. Thoroughgoing confirmation at application temperature and under load range conditions is requested.
C1	0.1µF	The input capacitor plays a part to lower output impedance of a power supply connected to input terminals (Vcc). When output impedance of this power supply increases, the input voltages (Vcc,) become unstable and there is a possibility of giving rise to oscillation and degraded ripple rejection characteristics. The use of capacitors of about 0.1 µF with low ESR, which provide less capacity value changes caused by temperature changes, is recommended, but since input capacitor greatly depends on characteristics of the power supply used for input, substrate wiring pattern, thoroughgoing confirmation under the application temperature and load range, is requested.
C2	10µF	The input capacitor plays a part to lower output impedance of a power supply connected to input terminals (VIN). When output impedance of this power supply increases, the input voltages (VIN) become unstable and there is a possibility of giving rise to oscillation and degraded ripple rejection characteristics. The use of capacitors of about 10 µF with low ESR, which provide less capacity value changes caused by temperature changes, is recommended, but since input capacitor greatly depends on characteristics of the power supply used for input, substrate wiring pattern, thoroughgoing confirmation under the application temperature and load range, is requested.
C4	1µF	To the present IC, there mounted is a function (Non Rush Current on Start-up: NRCS) to prevent rush current from VIN to load and output capacitor via Vo at the output voltage start-up. When the EN terminal is reset from High or UVLO, constant current is allowed to flow from the NRCS terminal. By this current, voltage generated at the NRCS terminal becomes the reference voltage and output voltage is started. In order to stabilize the NRCS set time, it is recommended to use a capacitor (B special) with less capacity value change caused by temperature change.

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●About heat loss

In designing heat, operate the apparatus within the following conditions.
(Because the following temperatures are warranted temperature, be sure to take margin, etc. into account.)

1. Ambient temperature Ta shall be not more than 100°C.
2. Chip junction temperature Tj shall be not more than 150°C.

Chip junction temperature Tj can be considered under the following two cases.

①Chip junction temperature Tj is found from IC surface temperature TC under actual application conditions:

$Tj=TC+\theta j\text{-}c\times W$

＜Reference value＞

θj-c:SOP8 41.0℃/W
HTSSOP-B20 45.0℃/W
Substrate size:70×70×1.6mm
(Substrate surface capper foil area:less3%)

θj-a:HTSSOP-B20 125.0℃/W
86.2℃/W
54.3℃/W
39.1℃/W

②Chip junction temperature Tj is found from ambient temperature Ta:

$Tj=Ta+\theta j\text{-}a\times W$

＜Reference value＞

θj-a:SOP8	222.0℃/W	(IC only)
	181.0℃/W	Single-layer substrate (substrate surface copper foil area: less 3%)
θj-a:HTSSOP-B20	125.0℃/W	Single-layer substrate (substrate surface copper foil area: less 3%))
	86.2℃/W	2nd-layer (substrate surface copper foil area:15×15mm^2)
	54.3℃/W	2nd-layer (substrate surface copper foil area: 70×70mm^2)
	39.1℃/W	4th-layer (substrate surface copper foil area: 70×70mm^2)

Substrate size 70×70×1.6mm^3 (thermal vias in the board.)

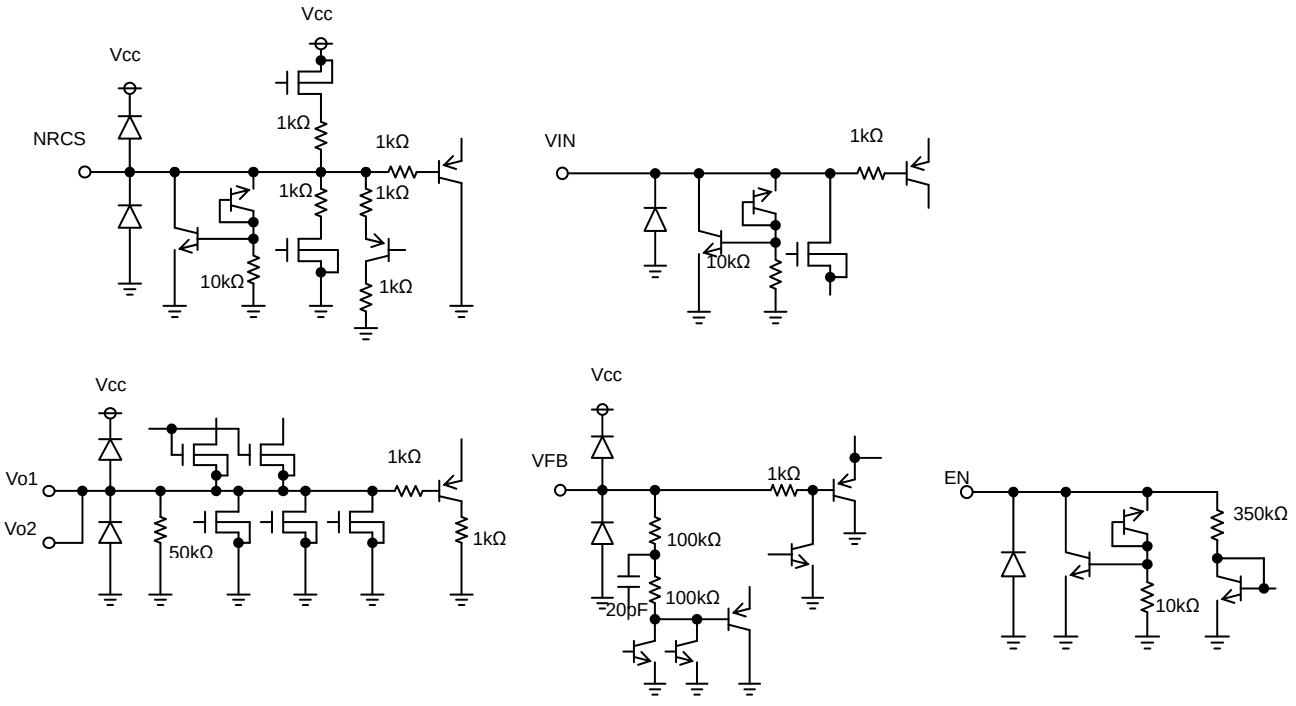
Most of heat loss in BD3506F/EFV occurs at the output Nch FET. The power lost is determined by multiplying the voltage between VIN and Vo by the output current. Confirm voltage and output current conditions of VIN and Vo used, and collate them with the thermal derating characteristics. Because BD3506EFV employs the power PKG, the thermal derating characteristics significantly vary in accord with the pc board conditions. When designing, care must be taken to the size of a pc board to be used.

Power dissipation (W) = {Input voltage (VIN) – Output voltage (V0≒VREF)}×Io (averaged)

Ex.) If VIN = 1.8 volts, V0=1.2 volts, and Io (averaged)=1.5 A, the power dissipation is given by the following:

Power dissipation (W) =(1.8 volts – 1.2 volts) × 1.5 (A)
= 0.9 W

●Equivalent Circuit



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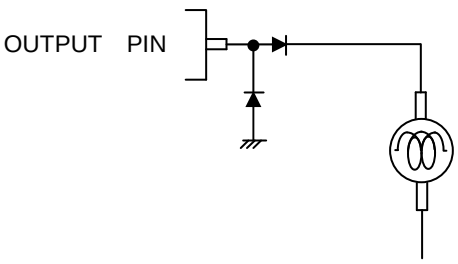
●Notes for use

1. Input terminals (VCC,VIN,EN)
   In the present IC, EN terminal, VIN terminal, and VCC terminal have an independent construction. In addition, in order to prevent malfunction at the time of low input, the UVLO function is equipped with the VCC terminal. They begin to start output voltage when all the terminals reach threshold voltage without depending on the input order of input terminals.
2. Operating range
   Within the operating range, the operation and function of the circuits are generally guaranteed at an ambient temperature within the range specified. The values specified for electrical characteristics may not be guaranteed, but drastic change may not occur to such characteristics within the operating range.
3. Permissible dissipation
   With respect to the permissible dissipation, the thermal derating characteristics are shown in the Exhibit, which we hope would be used as a good-rule-of-thumb. Should the IC be used in such a manner to exceed the permissible dissipation, reduction of current capacity due to chip temperature rise, and other degraded properties inherent to the IC would result. You are strongly urged to use the IC within the permissible dissipation.
4. Built-in thermal shutdown protection circuit
   The thermal shutdown circuit is first and foremost intended for interrupt IC from thermal runaway, and is not intended to protect and warrant the IC. Consequently, never attempt to continuously use the IC after this circuit is activated or to use the circuit with the activation of the circuit premised.
5. Inspection by set substrate
   In the event a capacitor is connected to a pin with low impedance at the time of inspection with a set substrate, there is a fear of applying stress to the IC. Therefore, be sure to discharge electricity for every process. As electrostatic measures, provide grounding in the assembly process, and take utmost care in transportation and storage. Furthermore, when the set substrate is connected to a jig in the inspection process, be sure to turn OFF power supply to connect the jig and be sure to turn OFF power supply to remove the jig.
6. For the present product, thoroughgoing quality control is carried out, but in the event that applied voltage, working temperature range, and other absolute maximum rating are exceeded, the present product may be destroyed. Because it is unable to identify the short mode, open mode, etc., if any special mode is assumed, which exceeds the absolute maximum rating, physical safety measures are requested to be taken, such as fuses, etc..
7. The use in the strong electromagnetic field may sometimes cause malfunction, to which care must be taken.
8. In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.

   (Example)



9. We are certain that examples of applied circuit diagrams are recommendable, but you are requested to thoroughly confirm the characteristics before using the IC. In addition, when the IC is used with the external circuit changed, decide the IC with sufficient margin provided while consideration is being given not only to static characteristics but also variations of external parts and our IC including transient characteristics.

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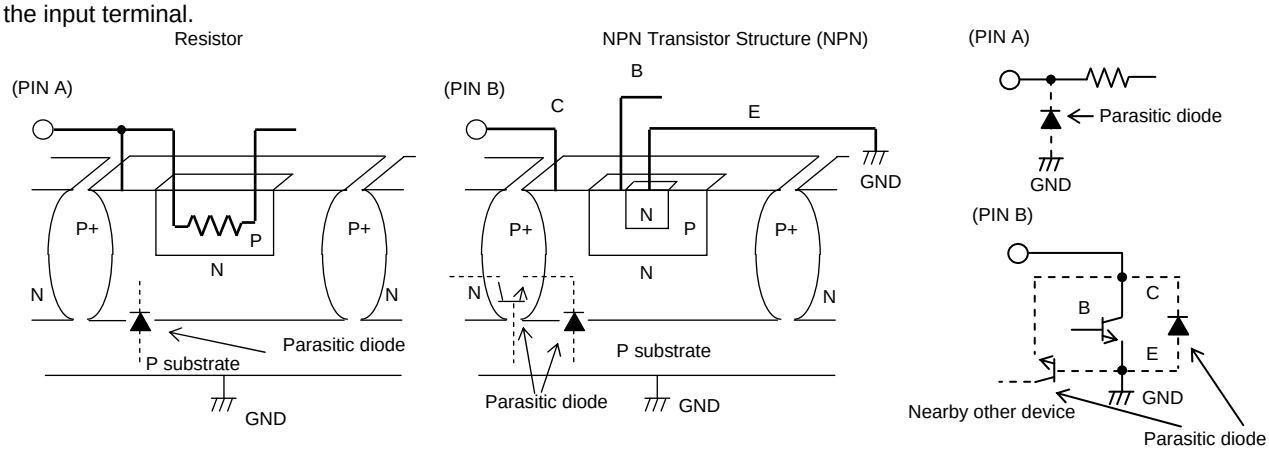
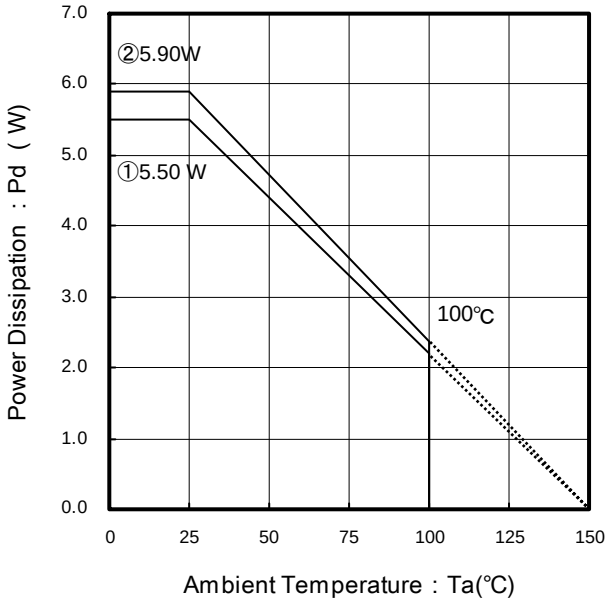
10. The present IC is a monolithic IC and has P^+ isolation between elements to separate elements and a P substrate. With this P layer and N layer of each element, PN junction is formed, and various parasitic elements are formed.
For example, when resistors and transistors are connected to terminals as illustrated below,
○at the resistor, when GND>terminal A, and at transistor (NPN),
when GND>terminal B,PN junction works as a parasitic diode.
○at the transistor (NPN), when GND>terminal B,the parasitic NPN transistor is operated
by the N-layer of other element adjacent to the parasitic diode.
The parasitic element is inevitably formed because of the IC construction. The operation of the parasitic element gives rise to mutual interference between circuits and results in malfunction, and eventually, breakdown. Consequently, take utmost care not to use the IC to operate the parasitic element such as applying voltage lower than GND (P substrate) to the input terminal.



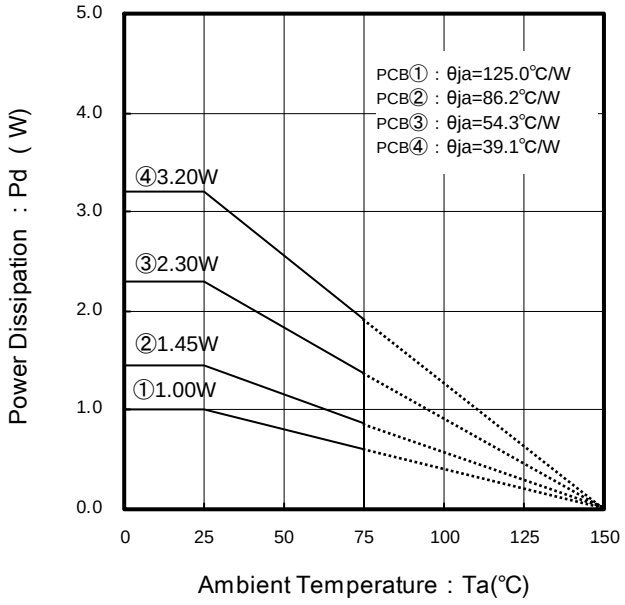
●Power Dissipation

SOP8



①Without heat sink
θj-a=222℃/W
②Mounted on board
70mm×70mm×1.6mm Glass-epoxy PCB
θj-a=181℃/W

HTSSOPB-20



measure : TH-156(Kuwano-Denki)
measure condition : Rohm Standard Board
PCB size : 70mm×70mm×1.6mmt(PCB with Thermal Via)
PCB① : Single-layer substrate
PCB② : Double-layer substrate
(substrate surface copper foil area 15mm×15mm)
PCB③ : Double-layer substrate
(substrate surface copper foil area 70mm×70mm)
PCB④ : Fourth-layer substrate
(substrate surface copper foil area 70mm×70mm)

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●Ordering part number

B	D	3	5	0	6	E	F	V	-	E	2

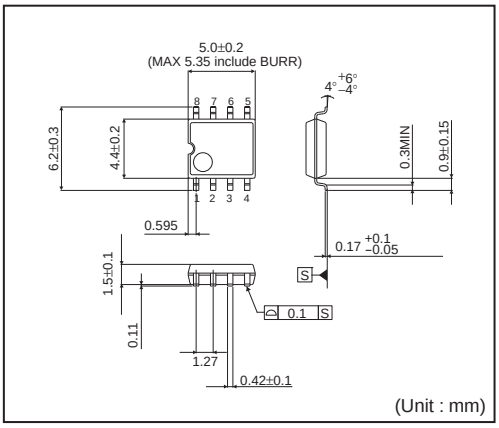
Part No. (BD)

Part No. (3506)

Package
F : SOP8
EFV : HTSSOPB-20

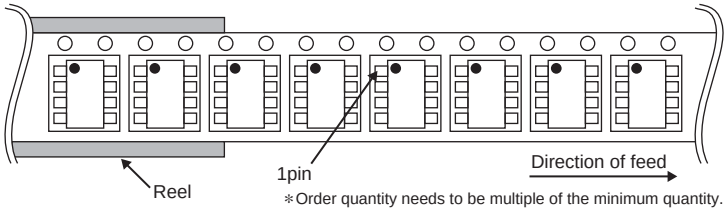
Packaging and forming specification
E2: Embossed tape and reel

SOP8



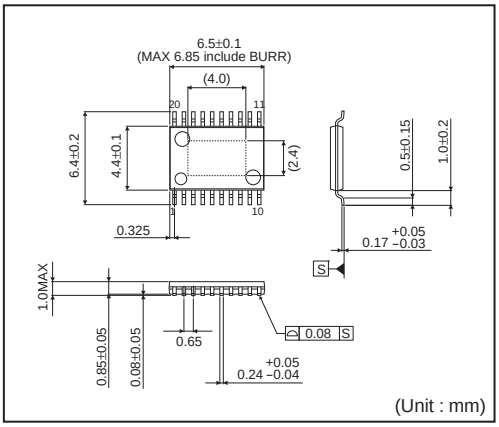
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



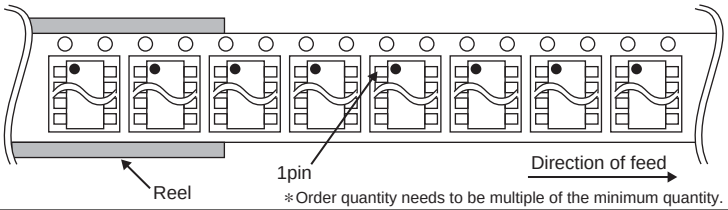
∗Order quantity needs to be multiple of the minimum quantity.

HTSSOP-B20



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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Notes

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