S-5855A Series

PWM OUTPUT TEMPERATURE SENSOR IC

www.sii-ic.com

Rev.1.3_00

The S-5855A Series, developed by CMOS technology, is a 1-wire PWM output temperature sensor IC of low current consumption that itself changes the duty ratio according to temperature.
The duty ratio decreases from 100% if exceeding the temperature set by user, and this decrease is linear against the temperature rise.
The output form is selectable from CMOS output and Nch open-drain output.
Its small packages SNT-4A and SOT-23-5 enable high-density mounting.

■ Features

- PWM output : 1-wire PWM interface
- Temperature accuracy : ±3.0°C
- Duty ratio change-start temperature : Selectable from +40°C to +80°C in 10°C step
- Duty ratio temperature sensitivity : Selectable from −1 %/°C to −4 %/°C in 1 %/°C step
- Low current consumption : 50 μA typ. (Ta = +25°C)
- Low power supply voltage : 1.65 V to 5.5 V
- Wide range of operation temperature : Ta = −40°C to +125°C
- Lead-free (Sn 100%), halogen-free

■ Application

- Temperature compensation for LED instruments

■ Packages

- SNT-4A
- SOT-23-5

■ Block Diagrams

1. CMOS output product

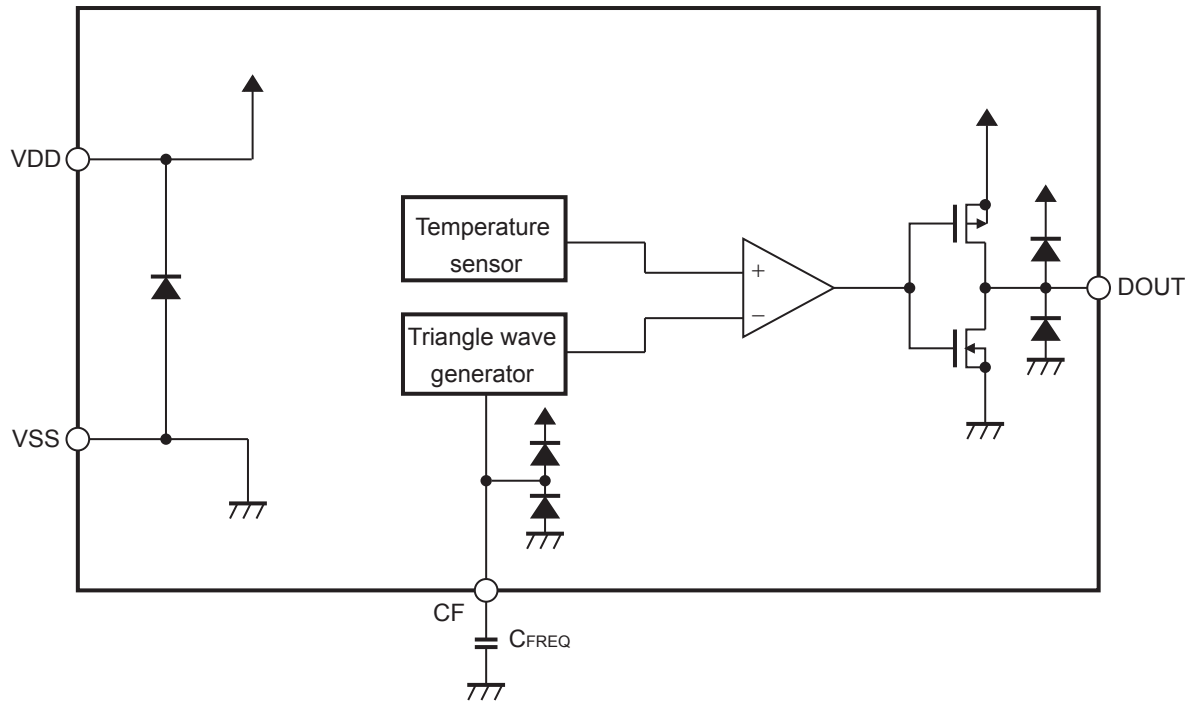


Figure 1

2. Nch open-drain output product

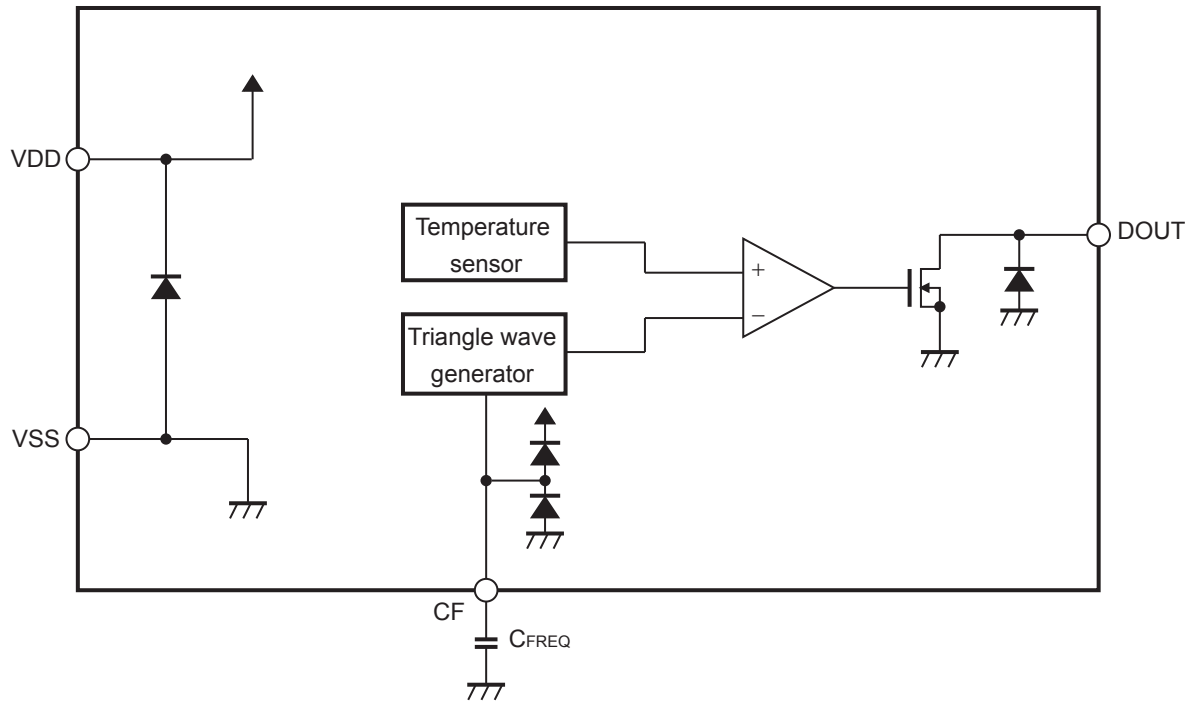
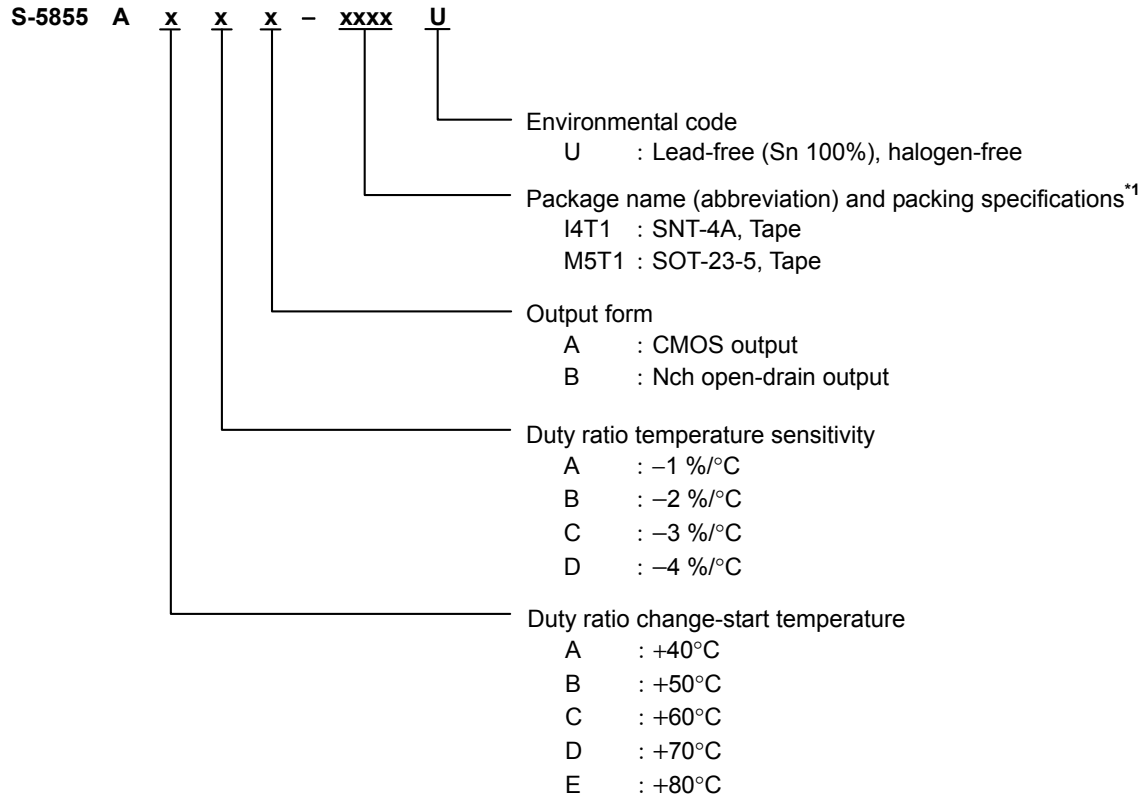


Figure 2

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.

2. Packages

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SNT-4A	PF004-A-P-SD	PF004-A-C-SD	PF004-A-R-SD	PF004-A-L-SD
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	–

3. Product name list

(1) SNT-4A

Table 1

Product name	Duty ratio change-start temperature T_S*1 [°C]	Duty ratio temperature sensitivity Ddt(s)*2 [%/°C]	Output form	T_{SP5}*3 [°C]	T_{EM5}*4 [°C]
S-5855AACA-I4T1U	+40	−3	CMOS output	+45	+60
S-5855AEAA-I4T1U	+80	−1	CMOS output	+85	+125
S-5855AECA-I4T1U	+80	−3	CMOS output	+85	+100

***1.** T_S : Duty ratio change-start temperature set by user
***2.** Ddt(s) : Duty ratio temperature sensitivity set by user
***3.** T_{SP5} : Temperature 5°C higher than duty ratio change-start temperature T_S (Refer to **Table 12** for details)
***4.** T_{EM5} : Higher temperature when measuring duty ratio temperature sensitivity (Refer to **Table 12** for details)

Remark Please contact our sales office for products other than those specified above.

(2) SOT-23-5

Table 2

Product name	Duty ratio change-start temperature T_S*1 [°C]	Duty ratio temperature sensitivity Ddt(s)*2 [%/°C]	Output form	T_{SP5}*3 [°C]	T_{EM5}*4 [°C]
S-5855AAAA-M5T1U	+40	−1	CMOS output	+45	+115
S-5855AAAB-M5T1U	+40	−1	Nch open-drain output	+45	+115
S-5855AADA-M5T1U	+40	−4	CMOS output	+45	+55

***1.** T_S : Duty ratio change-start temperature set by user
***2.** Ddt(s) : Duty ratio temperature sensitivity set by user
***3.** T_{SP5} : Temperature 5°C higher than duty ratio change-start temperature T_S (Refer to **Table 12** for details)
***4.** T_{EM5} : Higher temperature when measuring duty ratio temperature sensitivity (Refer to **Table 12** for details)

Remark Please contact our sales office for products other than those specified above.

■ Pin Configurations

SNT-4A
Top view

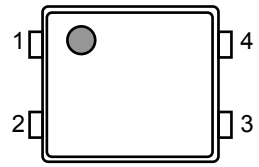


Figure 3

Table 3

Pin No.	Symbol	Pin Description
1	VSS	GND pin
2	CF	Connection pin for frequency control capacitor
3	VDD	Power supply pin
4	DOUT	Output pin

SOT-23-5
Top view

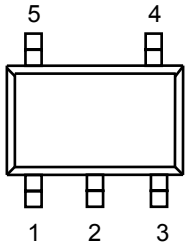


Figure 4

Table 4

Pin No.	Symbol	Pin Description
1	CF	Connection pin for frequency control capacitor
2	VSS	GND pin
3	NC*1	No connection
4	DOUT	Output pin
5	VDD	Power supply pin

***1.** The NC pin is electrically open.
The NC pin can be connected to VDD pin or VSS pin.

■ Absolute Maximum Ratings

Table 5

(Ta = +25°C, V_{SS} = 0 V, unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Power supply voltage		V_{DD}	V_{SS} −0.3 to V_{SS} +7.0	V
Output voltage	CMOS output product	V_{OUT}	V_{SS} −0.3 to V_{DD} +0.3	V
	Nch open-drain output product		V_{SS} −0.3 to V_{SS} +7.0	V
CF voltage		V_{CF}	V_{SS} −0.3 to V_{DD} +0.3	V
Output current		I_{OUT}	−13 to +13	mA
Power dissipation	SNT-4A	P_D	300[*1]	mW
	SOT-23-5		600[*1]	mW
Operating ambient temperature		T_{opr}	−40 to +125	°C
Storage temperature		T_{stg}	−65 to +150	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Electrical Characteristics

1. Common items

Table 6

($Ta = T_{SP5}$, V_{DD} = 3.0 V, V_{SS} = 0 V, unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Power supply voltage	V_{DD}	–		1.65	–	5.5	V	1
Current consumption	I_{DD}	No load at output pin	$Ta = T_{SP5}$	–	–	200	μA	1
			Ta = +25°C (Duty ratio 100%)	–	50	–	μA	1
Output leakage current	I_{LEAK}	Nch open-drain output product V_{OUT} = 5.5 V, Ta = +25°C		–	–	1	μA	3
Output source current	I_{SOURCE}	CMOS output product $V_{OUT} = V_{DD} - 0.3$ V		0.8	–	–	mA	3
Output sink current	I_{SINK}	$V_{OUT} = V_{SS} + 0.3$ V		3	–	–	mA	3
Fall time	t_F	C_L = 100 pF, R_L = 10 kΩ $V_{OUT} = 0.8 \times V_{DD}$ to $0.2 \times V_{DD}$	Nch open-drain output product	–	20	–	ns	5
			CMOS output product	–	20	–	ns	4
Rise time	t_R	Nch open-drain output product C_L = 15 pF, R_L = 10 kΩ $V_{OUT} = 0.2 \times V_{DD}$ to $0.8 \times V_{DD}$		–	300	–	ns	5
		CMOS output product C_L = 100 pF, R_L = 10 kΩ $V_{OUT} = 0.2 \times V_{DD}$ to $0.8 \times V_{DD}$		–	50	–	ns	4

2. Product with duty ratio temperature sensitivity Ddt(s) = –1 %/°C

Table 7

($Ta = T_{SP5}$, V_{DD} = 3.0 V , V_{SS} = 0 V, C_{FREQ} = 2.2 nF, unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Duty ratio accuracy	Dsp5	V_{DD} = 3.0 V		92.0	95.0	98.0	%	2
		V_{DD} = 1.65 V to 5.5 V		91.0	95.0	99.0	%	2
Duty ratio temperature sensitivity	Ddt(E)*1	Ta = T_{SP5}*2, T_{EM5}*3	V_{DD} = 3.0 V	–1.2	–1.0	–0.8	%/°C	2
			V_{DD} = 1.65 V to 5.5 V	–1.26	–1.0	–0.76	%/°C	2
Oscillation frequency	f_{OSC}	Ta = T_{SP5}	V_{DD} = 3.0 V	1950	2300	2650	Hz	2
			V_{DD} = 1.65 V to 5.5 V	1860	2300	2780	Hz	2
		Ta = T_{EM5}	V_{DD} = 3.0 V	1670	2300	3040	Hz	2

***1.** Ddt(E): Actual duty ratio temperature sensitivity
***2.** T_{SP5}: Temperature 5°C higher than duty ratio change-start temperature T_S (Refer to **Table 12** for details)
***3.** T_{EM5}: Higher temperature when measuring duty ratio temperature sensitivity (Refer to **Table 12** for details)

3. Product with duty ratio temperature sensitivity Ddt(s) = –2 %/°C

Table 8

($Ta = T_{SP5}$, V_{DD} = 3.0 V , V_{SS} = 0 V, C_{FREQ} = 4.7 nF, unless otherwise specified)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Duty ratio accuracy	Dsp5	V_{DD} = 3.0 V		84.0	90.0	96.0	%	2
		V_{DD} = 1.65 V to 5.5 V		82.0	90.0	98.0	%	2
Duty ratio temperature sensitivity	Ddt(E)*1	Ta = T_{SP5}*2, T_{EM5}*3	V_{DD} = 3.0 V	–2.4	–2.0	–1.6	%/°C	2
			V_{DD} = 1.65 V to 5.5 V	–2.52	–2.0	–1.52	%/°C	2
Oscillation frequency	f_{OSC}	Ta = T_{SP5}	V_{DD} = 3.0 V	1840	2160	2740	Hz	2
			V_{DD} = 1.65 V to 5.5 V	1750	2160	2600	Hz	2
		Ta = T_{EM5}	V_{DD} = 3.0 V	1560	2160	2850	Hz	2

***1.** Ddt(E): Actual duty ratio temperature sensitivity
***2.** T_{SP5}: Temperature 5°C higher than duty ratio change-start temperature T_S (Refer to **Table 12** for details)
***3.** T_{EM5}: Higher temperature when measuring duty ratio temperature sensitivity (Refer to **Table 12** for details)

4. Product with duty ratio temperature sensitivity Ddt(s) = –3 %/°C

Table 9

($Ta = T_{SP5}$, V_{DD} = 3.0 V , V_{SS} = 0 V, C_{FREQ} = 6.8 nF, unless otherwise specified)

Items	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Duty ratio accuracy	Dsp5	V_{DD} = 3.0 V		76.0	85.0	94.0	%	2
		V_{DD} = 1.65 V to 5.5 V		73.0	85.0	97.0	%	2
Duty ratio temperature sensitivity	Ddt(E)*1	$Ta = T_{SP5}$*2, T_{EM5}*3	V_{DD} = 3.0 V	–3.6	–3.0	–2.4	%/°C	2
			V_{DD} = 1.65 V to 5.5 V	–3.78	–3.0	–2.28	%/°C	2
Oscillation frequency	f_{OSC}	$Ta = T_{SP5}$	V_{DD} = 3.0 V	1900	2240	2570	Hz	2
			V_{DD} = 1.65 V to 5.5 V	1810	2240	2700	Hz	2
		$Ta = T_{EM5}$	V_{DD} = 3.0 V	1620	2240	2950	Hz	2

***1.** Ddt($E_)$: Actual duty ratio temperature sensitivity
***2.** T_{SP5}: Temperature 5°C higher than duty ratio change-start temperature T_S (Refer to **Table 12** for details)
***3.** T_{Em5}: Higher temperature when measuring duty ratio temperature sensitivity (Refer to **Table 12** for details)

5. Product with duty ratio temperature sensitivity Ddt(s) = –4 %/°C

Table 10

($Ta = T_{SP5}$, V_{DD} = 3.0 V , V_{SS} = 0 V, C_{FREQ} = 10 nF, unless otherwise specified)

Items	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Duty ratio accuracy	Dsp5	V_{DD} = 3.0 V		68.0	80.0	92.0	%	2
		V_{DD} = 1.65 V to 5.5 V		64.0	80.0	96.0	%	2
Duty ratio temperature sensitivity	Ddt(E)*1	$Ta = T_{SP5}$*2, T_{EM5}*3	V_{DD} = 3.0 V	–4.8	–4.0	–3.2	%/°C	2
			V_{DD} = 1.65 V to 5.5 V	–5.05	–4.0	–3.04	%/°C	2
Oscillation frequency	f_{OSC}	$Ta = T_{SP5}$	V_{DD} = 3.0 V	1730	2030	2330	Hz	2
			V_{DD} = 1.65 V to 5.5 V	1640	2030	2440	Hz	2
		$Ta = T_{EM5}$	V_{DD} = 3.0 V	1470	2030	2680	Hz	2

***1.** Ddt(E): Actual duty ratio temperature sensitivity
***2.** T_{SP5}: Temperature 5°C higher than duty ratio change-start temperature T_S (Refer to **Table 12** for details)
***3.** T_{EM5}: Higher temperature when measuring duty ratio temperature sensitivity (Refer to **Table 12** for details)

■ Test Circuits

1.

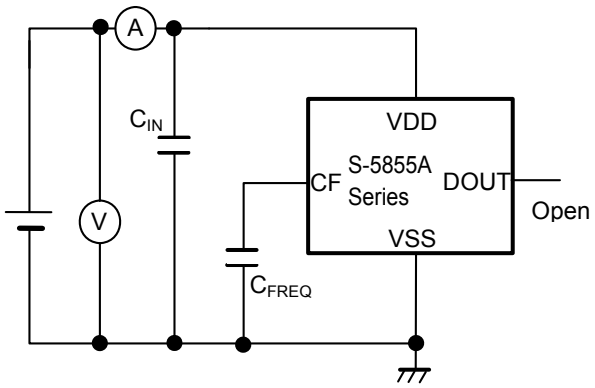
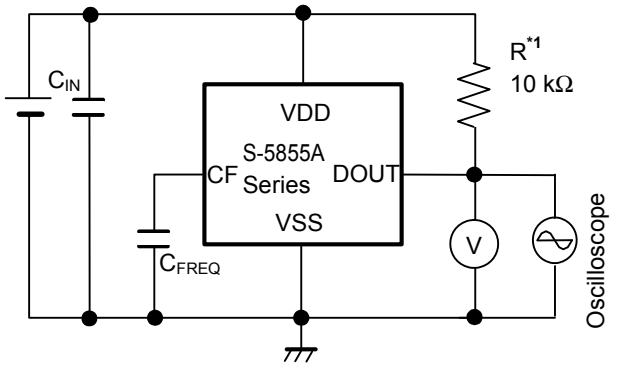


Figure 5

2.



***1.** Resistor (R) is unnecessary for the CMOS output product.

Figure 6

3.

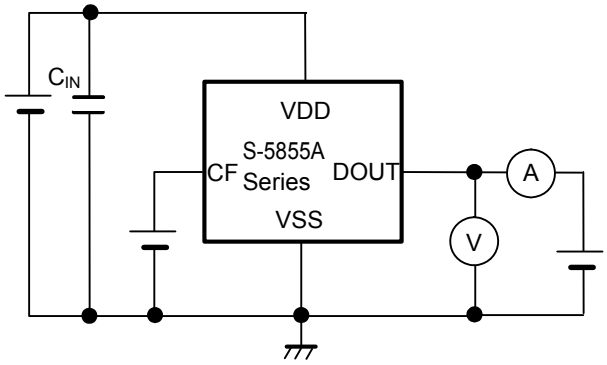


Figure 7

4.

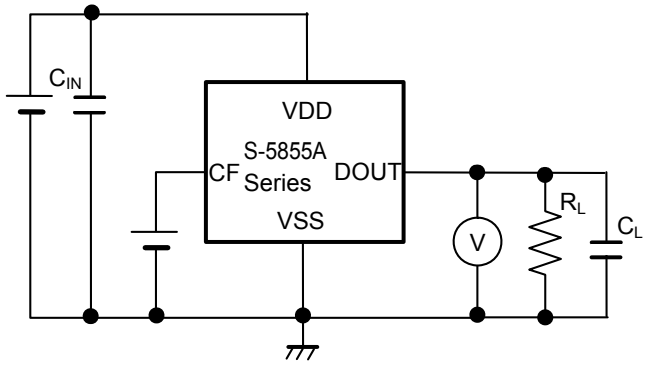


Figure 8

5.

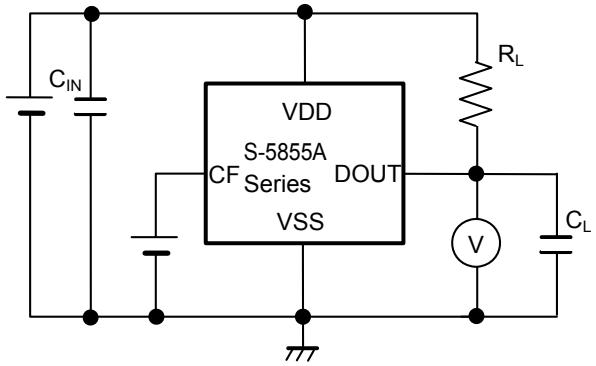
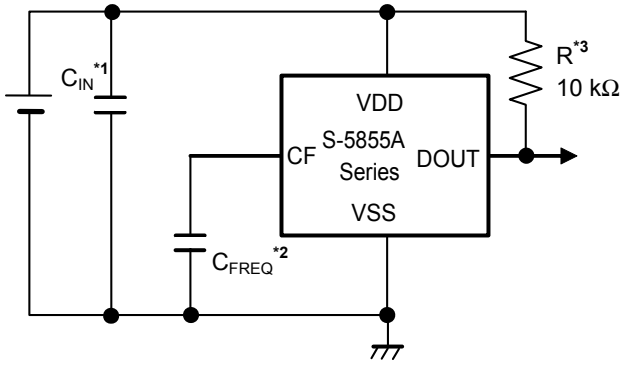


Figure 9

■ Standard Circuit



***1.** C_{IN} is a capacitor for stabilization.
***2.** C_{FREQ} is a capacitor for oscillation frequency.
***3.** Resistor (R) is unnecessary for the CMOS output product.

Figure 10

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Operation

1. Duty ratio

The following equation is the definition of duty ratio.
Duty ratio = PW / T × 100 [%]
The definitions of PW and T are shown in **Figure 11**.

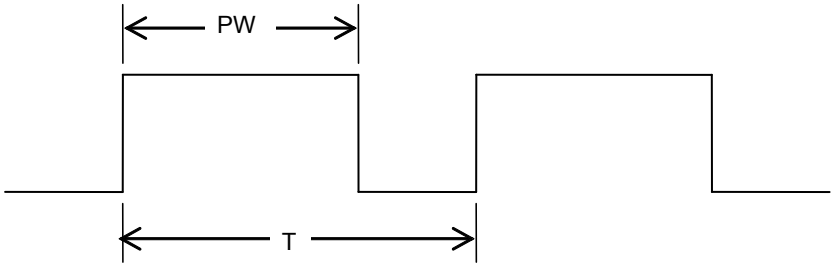


Figure 11

2. Oscillation frequency

The oscillation frequency is set by the capacitance value of the capacitor C_{FREQ} for the oscillation frequency.
The relationship between the C_{FREQ} capacitance value of each duty ratio temperature sensitivity and the center value of the oscillation frequency are shown in **Table 11**.

Table 11

Duty ratio temperature sensitivity Ddt(s) [%/°C]	C_{FREQ} capacitance value [nF]	Center value of oscillation frequency [Hz]
−1	2.2	2300
−2	4.7	2160
−3	6.8	2240
−4	10.0	2030

■ Explanation of Terms

1. Duty ratio accuracy (Dsp5)

Dsp5 shows duty ratio in temperature T_{SP5} 5°C higher than duty ratio change-start temperature T_S.

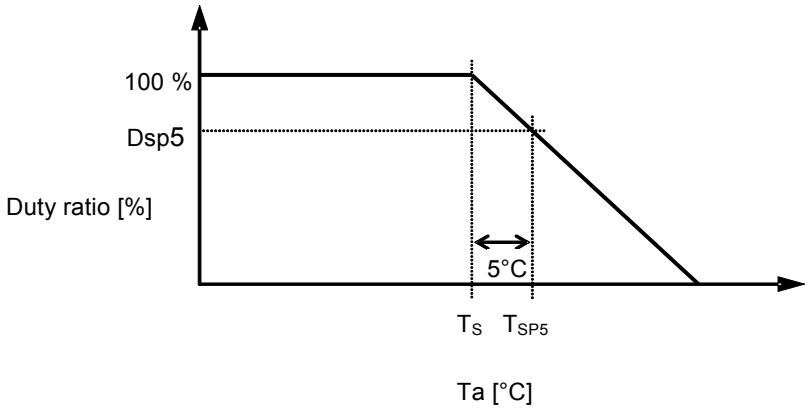
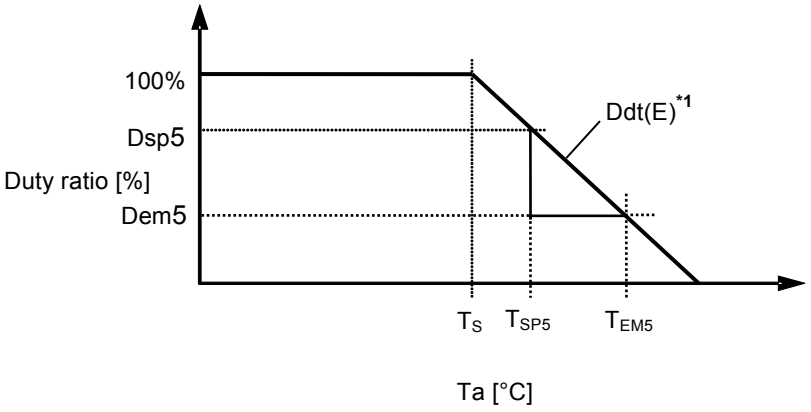


Figure 12

2. Duty ratio temperature sensitivity (Ddt(E))

Duty ratio temperature sensitivity (Ddt(E)) is the temperature coefficient of duty ratio calculated from the output duty ratio at Ta = T_{SP5} and Ta = T_{EM5}. T_{EM5} is the temperature decided for each product shown in **Table 11**, and Dem5 is the output duty ratio at Ta = T_{EM5}. Ddt(E) is calculated using the following formula.

$Ddt(E) = (Dem5 - Dsp5) / (T_{EM5} - T_{SP5})$ [%/°C]



***1.** Selectable from −1 %/°C to −4 %/°C in 1 %/°C step

Figure 13

Table 12 T_{SP5} and T_{EM5} in Each Product

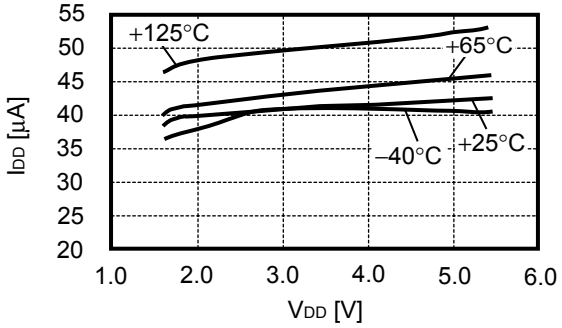
Duty ratio change-start temperature T_S [°C]	Duty ratio temperature sensitivity Ddt(s) [%/°C]	T_{SP5} [°C]	T_{EM5} [°C]
+40	−1	+45	+115
+40	−2	+45	+75
+40	−3	+45	+60
+40	−4	+45	+55
+50	−1	+55	+125
+50	−2	+55	+85
+50	−3	+55	+70
+50	−4	+55	+65
+60	−1	+65	+125
+60	−2	+65	+95
+60	−3	+65	+80
+60	−4	+65	+75
+70	−1	+75	+125
+70	−2	+75	+105
+70	−3	+75	+90
+70	−4	+75	+85
+80	−1	+85	+125
+80	−2	+85	+115
+80	−3	+85	+100
+80	−4	+85	+95

■ Precaution

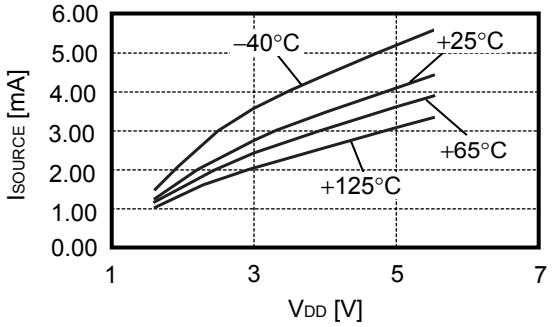
- Note that this IC may itself heat depending on a connected load to the output pin, resulting in error in measuring temperature.
- Set a capacitor (C_{IN}) of approx. 0.1 μF between the VDD pin and VSS pin for stabilization as close to IC as possible.
- Connect a capacitor C_{FREQ} for oscillation frequency as close to IC as possible.
- Leakage current applied on the CF pin may cause error in the output duty ratio. Do not connect other components than C_{FREQ}.
- Since the error of the output duty ratio may become large depending on an application circuit or the design of a board pattern on this IC, perform thorough evaluation with the actually mounted model in the case of use.
- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII Semiconductor Corporation claims no responsibility for any disputes arising out of or in connection with any infringement by products, including this IC, of patents owned by a third party.

■ Characteristics (Typical Data)

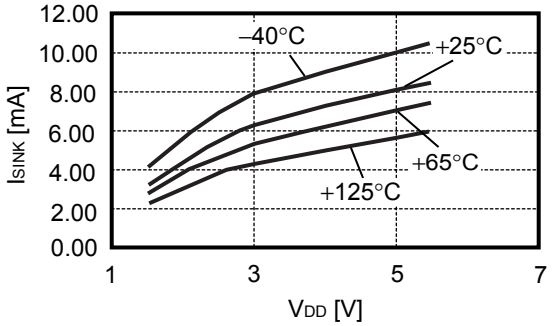
1. Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



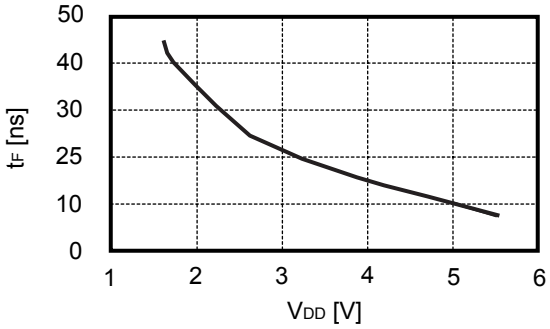
2. Output source current (I_{SOURCE}) vs. Power supply voltage (V_{DD})



3. Output sink current (I_{SINK}) vs. Power supply voltage (V_{DD})

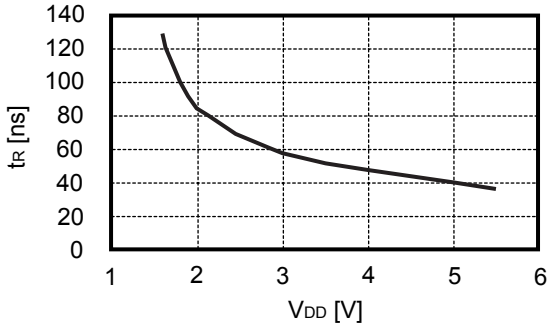


4. Fall time (t_F) vs. Power supply voltage (V_{DD}) dependency

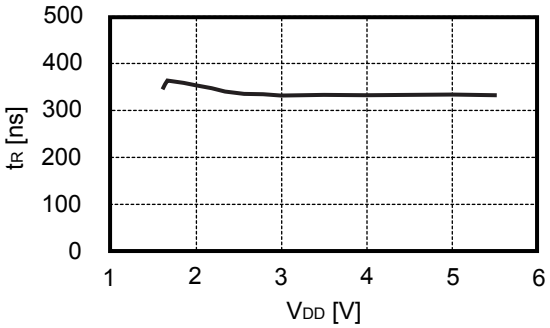


5. Rise time (t_R) vs.Power supply voltage (V_{DD}) dependency

5.1 CMOS output product

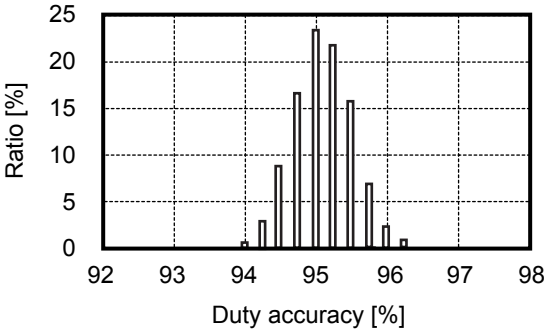


5.2 Nch open-drain output product

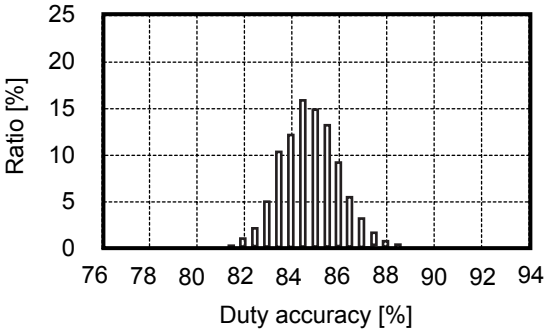


6. Duty ratio accuracy

6.1 Product with Ta = T_{SP5}, Ddt(s) = –1 %/°C

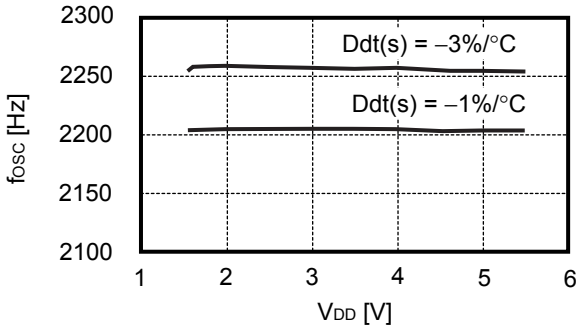


6.2 Product with Ta = T_{SP5}, Ddt(s) = –3 %/°C

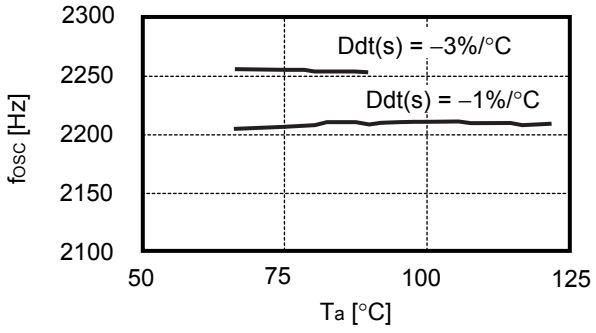


7. Oscillation frequency

7.1 Oscillation frequency (f_{OSC}) vs. Power supply voltage (V_{DD})



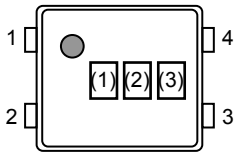
7.2 Oscillation frequency (f_{OSC}) vs. Temperature(Ta)



■ Marking Specifications

(1) SNT-4A

SNT-4A
Top view



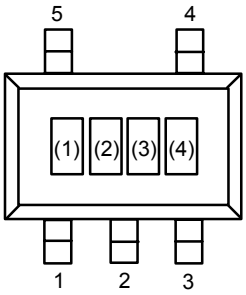
(1) to (3) : Product code (Refer to **Product name vs. Product code**.)

Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-5855AACA-I4T1U	V	Q	C
S-5855AEAA-I4T1U	V	Q	Y
S-5855AECA-I4T1U	V	Q	3

(2) SOT-23-5

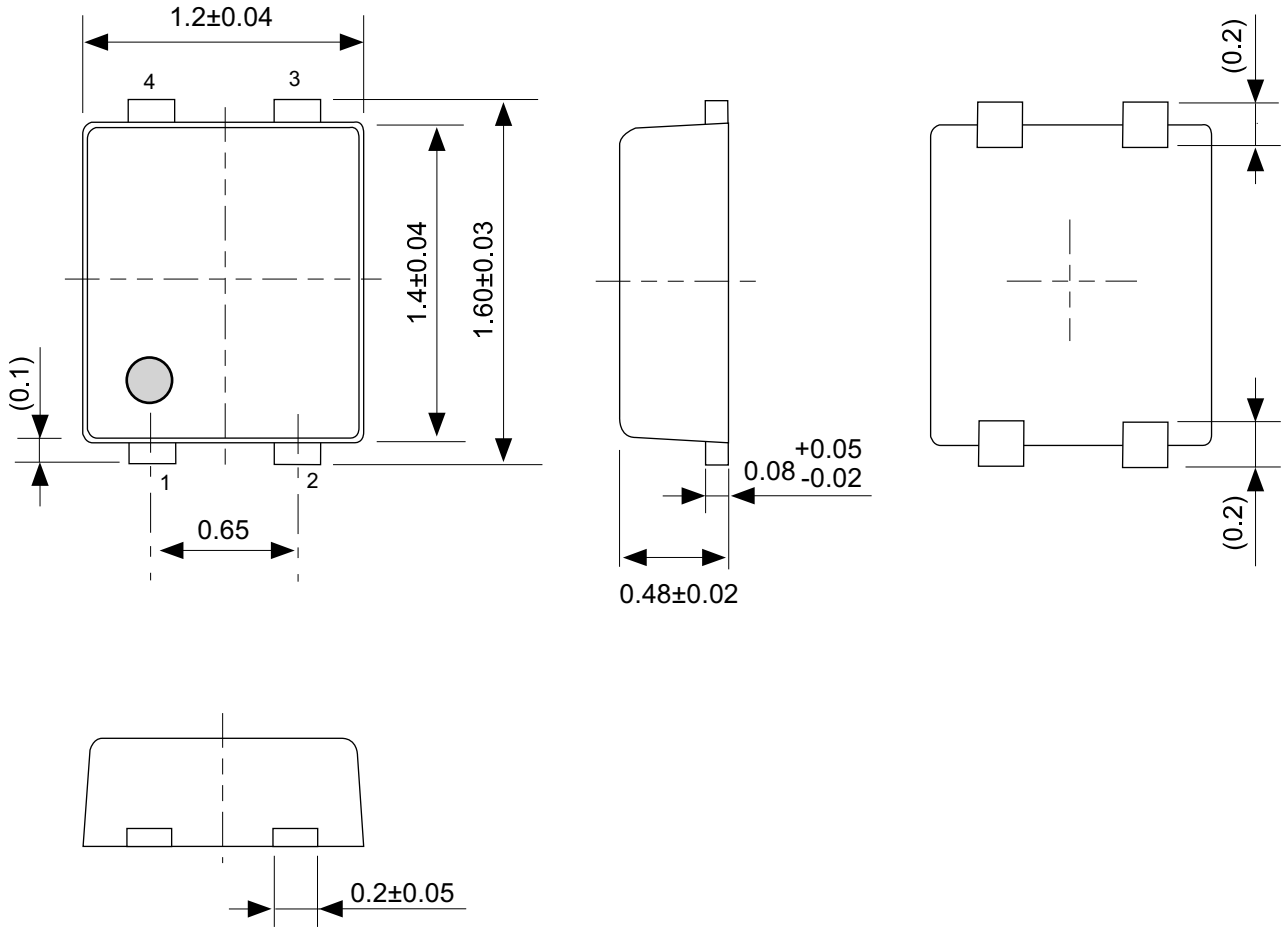
SOT-23-5
Top view



(1) to (3) : Product code (refer to **Product name vs. Product code**)
(4) : Lot number

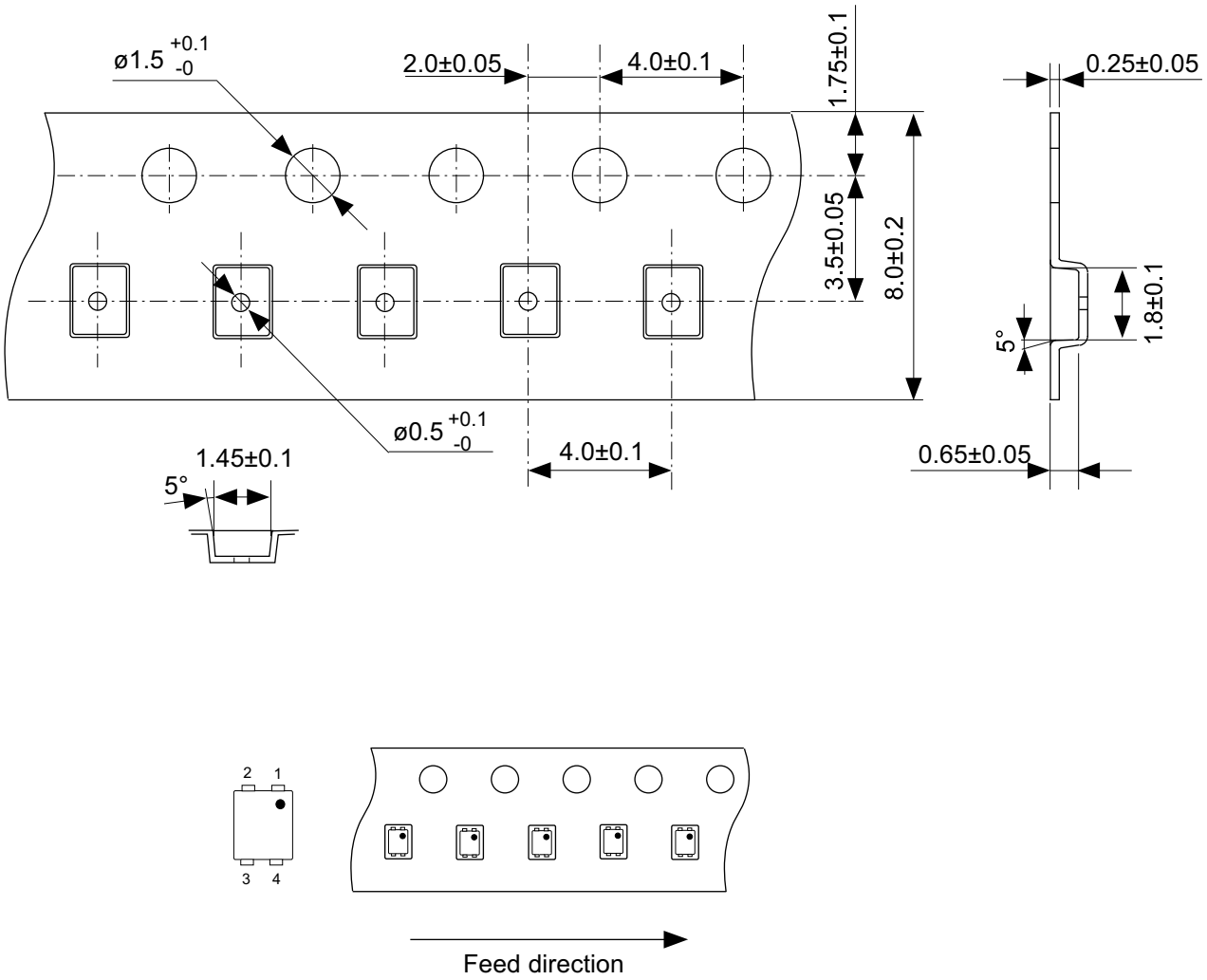
Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-5855AAAA-M5T1U	V	Q	A
S-5855AAAB-M5T1U	V	R	A
S-5855AADA-M5T1U	V	Q	D



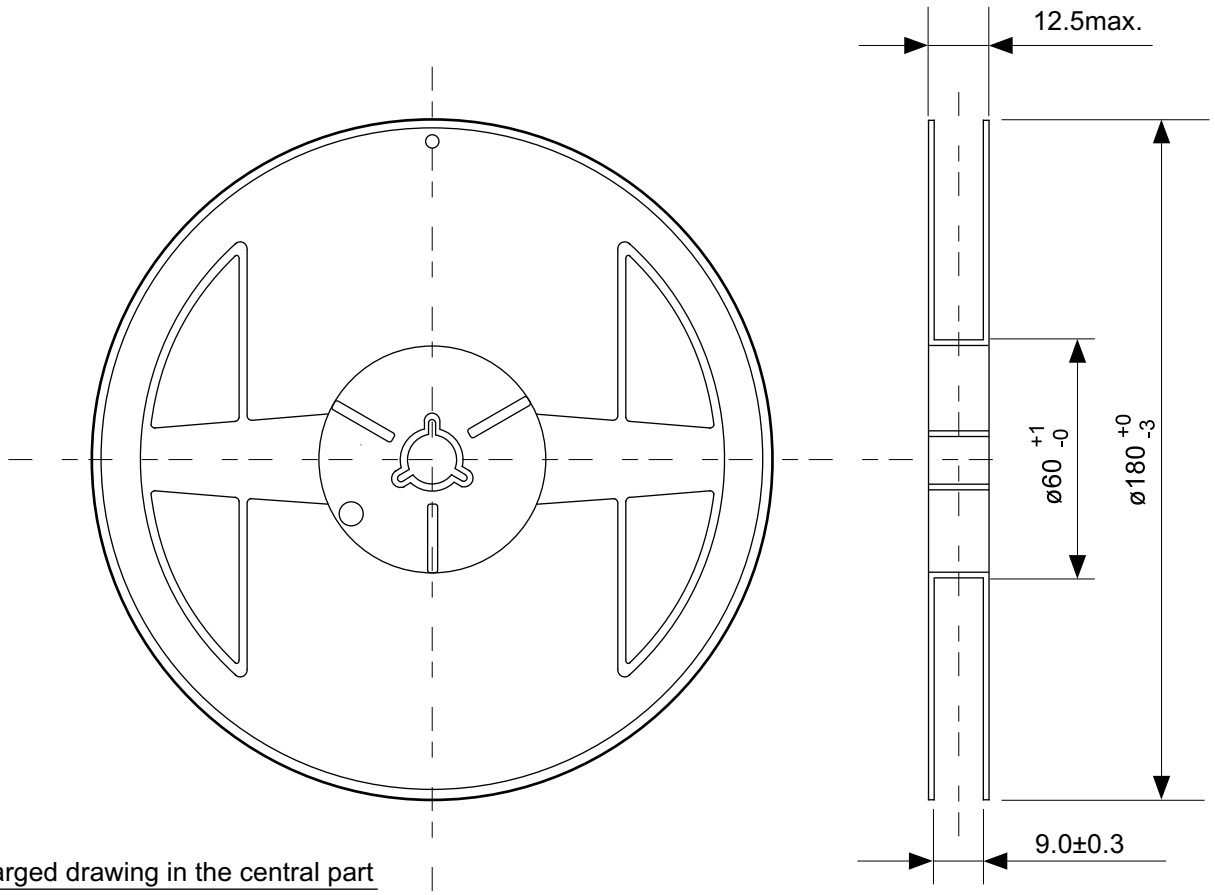
No. PF004-A-P-SD-6.0

TITLE	SNT-4A-A-PKG Dimensions
No.	PF004-A-P-SD-6.0
ANGLE	
UNIT	mm
SII Semiconductor Corporation	

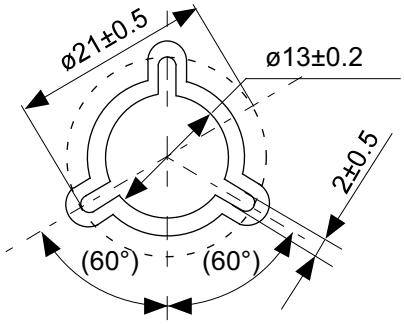


No. PF004-A-C-SD-1.0

TITLE	SNT-4A-A-Carrier Tape
No.	PF004-A-C-SD-1.0
ANGLE	
UNIT	mm
SII Semiconductor Corporation	

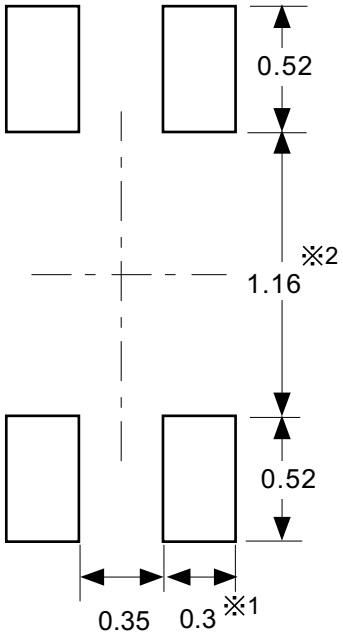


Enlarged drawing in the central part



No. PF004-A-R-SD-1.0

TITLE	SNT-4A-A-Reel		
No.	PF004-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
SII Semiconductor Corporation			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.10 mm ~ 1.20 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は ″SNTパッケージ活用の手引き″ を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.10 mm to 1.20 mm).

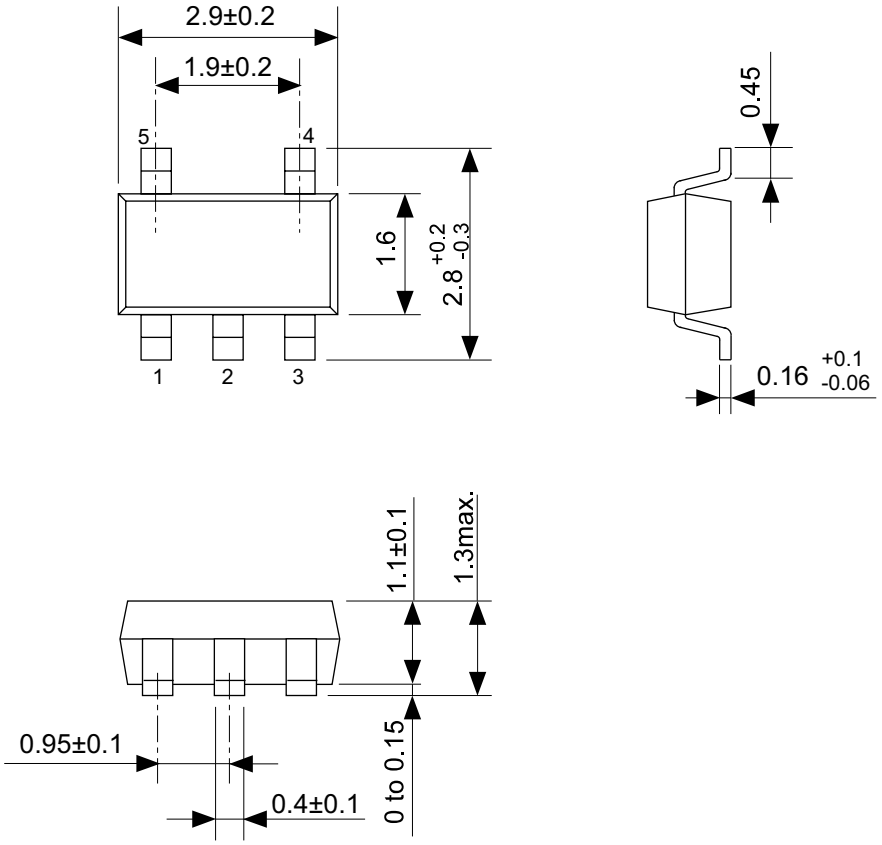
Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.10 mm ~ 1.20 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

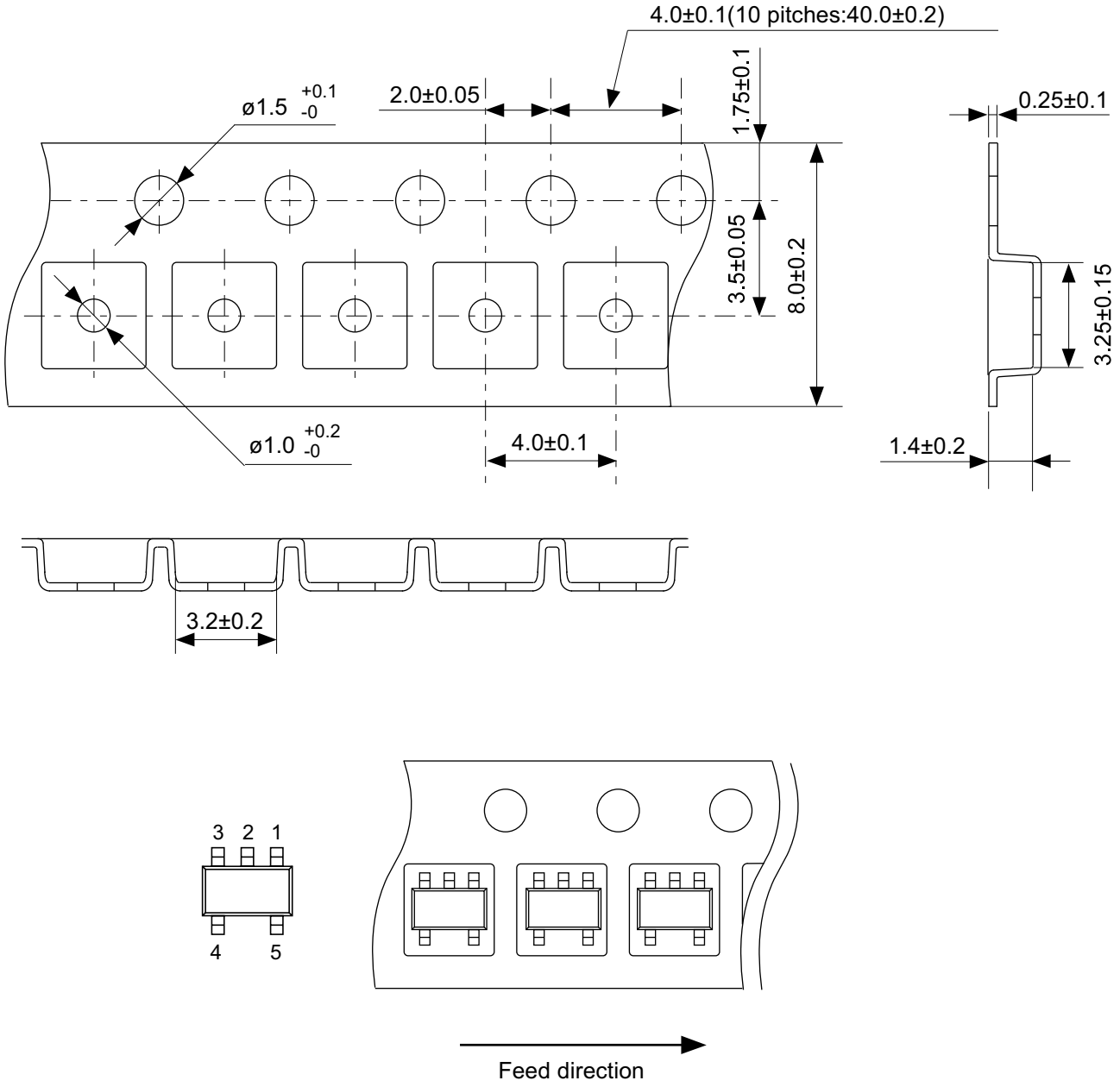
No. PF004-A-L-SD-4.1

TITLE	SNT-4A-A -Land Recommendation
No.	PF004-A-L-SD-4.1
ANGLE	
UNIT	mm
SII Semiconductor Corporation	



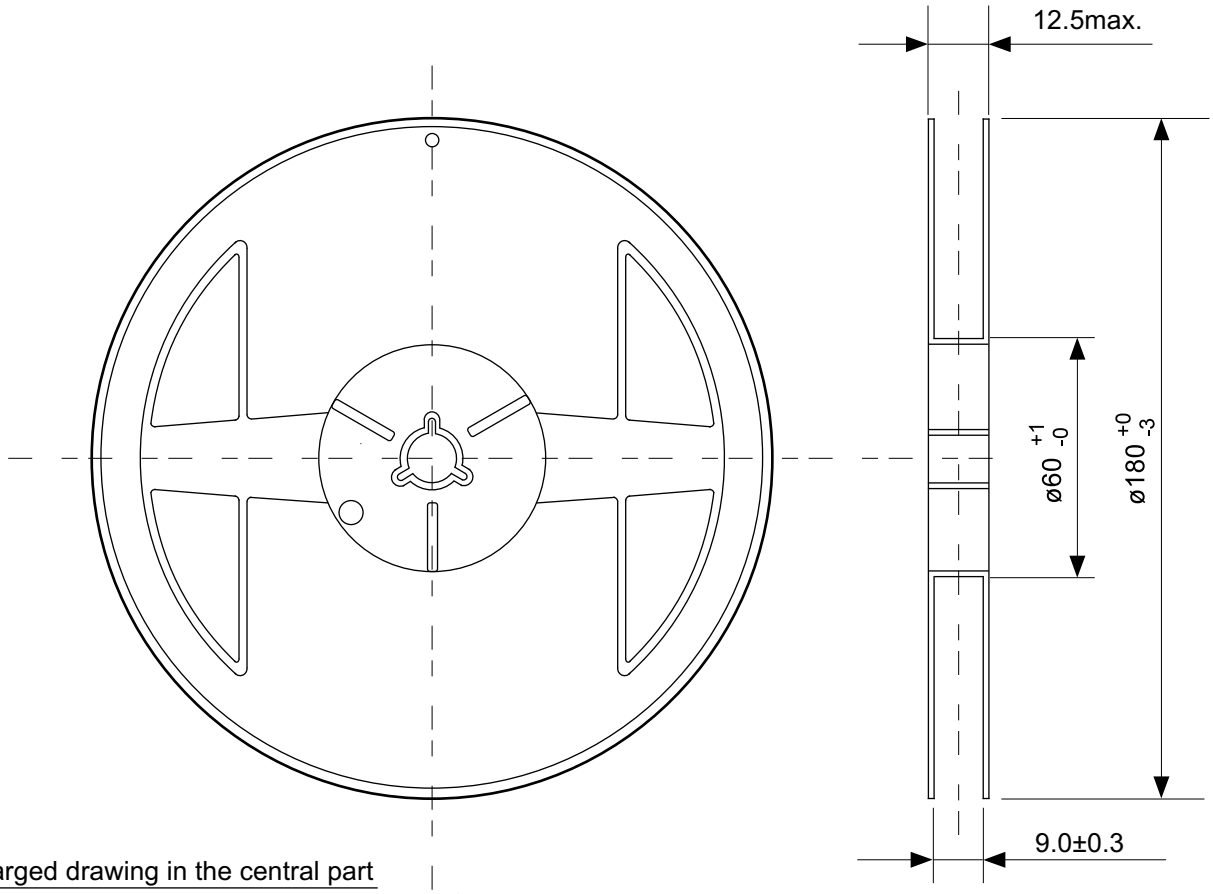
No. MP005-A-P-SD-1.3

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm
SII Semiconductor Corporation	

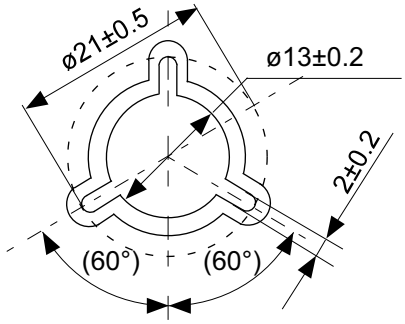


No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
SII Semiconductor Corporation	



Enlarged drawing in the central part



No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
SII Semiconductor Corporation			

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   SII Semiconductor Corporation is not responsible for damages caused by the reasons other than the products or infringement of third-party intellectual property rights and any other rights due to the use of the information described herein.
3. SII Semiconductor Corporation is not responsible for damages caused by the incorrect information described herein.
4. Take care to use the products described herein within their specified ranges. Pay special attention to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   SII Semiconductor Corporation is not responsible for damages caused by failures and/or accidents, etc. that occur due to the use of products outside their specified ranges.
5. When using the products described herein, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products described herein, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products described herein must not be used or provided (exported) for the purposes of the development of weapons of mass destruction or military use. SII Semiconductor Corporation is not responsible for any provision (export) to those whose purpose is to develop, manufacture, use or store nuclear, biological or chemical weapons, missiles, or other military use.
8. The products described herein are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses. Do not use those products without the prior written permission of SII Semiconductor Corporation.
   Especially, the products described herein cannot be used for life support devices, devices implanted in the human body and devices that directly affect human life, etc.
   Prior consultation with our sales office is required when considering the above uses.
   SII Semiconductor Corporation is not responsible for damages caused by unauthorized or unspecified use of our products.
9. Semiconductor products may fail or malfunction with some probability.
   The user of these products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system must be sufficiently evaluated and applied on customer's own responsibility.
10. The products described herein are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products described herein do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Take care when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products described herein, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of SII Semiconductor Corporation.
    The information described herein does not convey any license under any intellectual property rights or any other rights belonging to SII Semiconductor Corporation or a third party. Reproduction or copying of the information described herein for the purpose of disclosing it to a third-party without the express permission of SII Semiconductor Corporation is strictly prohibited.
14. For more details on the information described herein, contact our sales office.

1.0-2016.01