B`cﬄggR > A4 &' ! %A Microcontroller Ac`Uﬂ Te Brief

The Sqtﬂxxc'32-bit MPC5604P automotive oﬂetqeqpvtqﬁrgt'ﬂu'c'System-on-Chip (SoC) device fguﬂiﬁpgf'vq'dg'egpvtcﬂ'vq'ﬂjﬁg'development of the next wave of airbag/steering applications.

The MPC5604P is one of a series of next-generation automotive microcontrollers based on the Power Architecture™ Book E architecture and designed specifically for embedded applications.

This document describes the features of the MPC5604P and highlights important electrical and physical characteristics of the device.

Contents

1   Introduction

The MPC5604P family integrates all the most advanced and up-to-date motor control design features. It targets the following market segments:

- Chassis applications, specifically the Electrical Hydraulic Power Steering (EHPS) and the lower end of Electrical Power Steering (EPS)
- Airbag applications

2 Block diagram

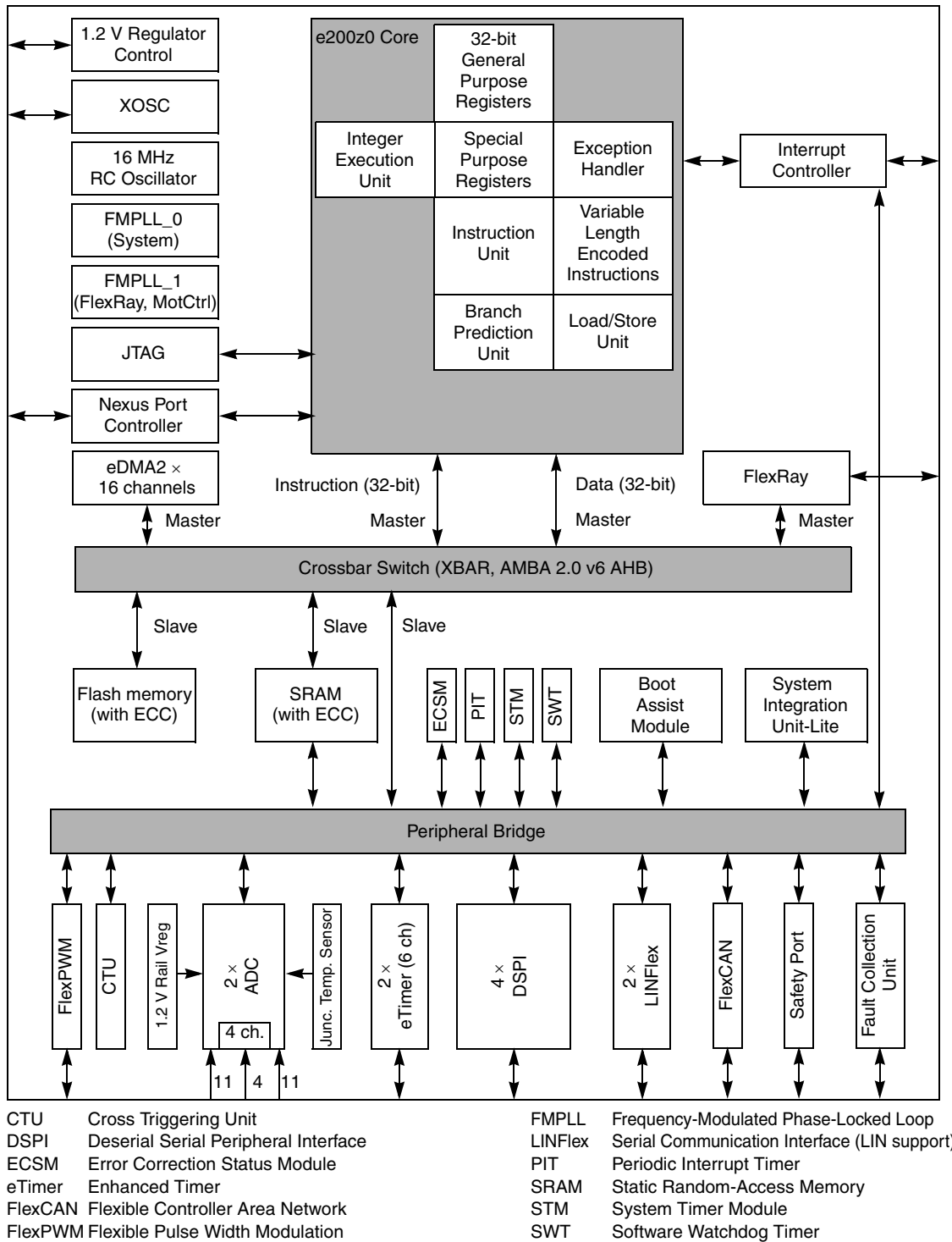Figure 1 shows a top-level block diagram of the MPC5604P microcontroller.

Figure 1. MPC5604P block diagram

CTU   Cross Triggering Unit
DSPI   Deserial Serial Peripheral Interface
ECSM   Error Correction Status Module
eTimer   Enhanced Timer
FlexCAN   Flexible Controller Area Network
FlexPWM Flexible Pulse Width Modulation

FMPLL   Frequency-Modulated Phase-Locked Loop
LINFlex   Serial Communication Interface (LIN support)
PIT   Periodic Interrupt Timer
SRAM   Static Random-Access Memory
STM   System Timer Module
SWT   Software Watchdog Timer

3   Overview of the MPC5604P

The following sections provide high-level descriptions of the features found on the MPC5604P.

3.1   Device summary

Table 1. MPC5604P device comparison

Feature	MPC5603P	MPC5604P
Code Flash memory (with ECC)	384 KB	512 KB
Data Flash / EE (with ECC)	64 KB	64 KB
RAM (with ECC)	36 KB	40 KB
Processor core	32-bit e200z0h	
Instruction set	VLE	
CPU performance	0–64 MHz	
FMPLL (frequency-modulated phase-locked loop) modules	2	
INTC (interrupt controller) channels	147	
PIT (periodic interrupt timer)	1 (includes four 32-bit timers)	
Enhanced DMA (direct memory access) channels	16	
FlexRay	Yes[1]	
FlexCAN (controller area network)	2[2,3]	
Safety port	Yes (via second FlexCAN module)	
FCU (fault collection unit)	Yes	
CTU (cross triggering unit)	Yes	
eTimer channels	2 × 6	
FlexPWM (pulse-width modulation) channels	8	
Analog-to-digital converters (ADC)	Two (10-bit, 16-channel)	
LINFlex modules	2	
DSPI (deserial serial peripheral interface) modules	4	
CRC (cyclic redundancy check) unit	Yes	
Junction temperature sensor	Yes	
JTAG interface	Yes	
Nexus port controller (NPC)	Yes (Level 2+)	

Table 1. MPC5604P device comparison (continued)

Feature		MPC5603P	MPC5604P
Supply	Digital power supply[4]	3.3 V or 5 V single supply with external transistor	
	Analog power supply	3.3 V or 5 V	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4–40 MHz	
Packages		100 LQFP 144 LQFP	
Temperature	Standard ambient temperature	–40 to 125 °C	
	Extended ambient temperature[5]	–40 to 145 °C	

NOTES:
[1] 32 message buffers, dual-channel.

[2] Each FlexCAN module has 32 message buffers.

[3] One FlexCAN module can act as a Safety Port with a bit rate as high as 7.5 Mbit/s.

[4] 3.3 V range and 5 V range correspond to different orderable parts.

[5] Thermally enhanced 100-pin and 144-pin LQFP packages are under analysis to support an extended ambient temperature range of –40 to 145 °C. The packages are not yet available.

3.2   Feature list

- High performance 64 MHz e200z0h CPU
    - — 32-bit Power Architecture Book E CPU
    - — Variable Length Encoding (VLE)
- Available memory
    - — As much as 512 KB on-chip code flash memory with additional 64 KB for EEPROM emulation (data flash), with ECC, with erase/program controller
    - — As much as 40 KB on-chip RAM with ECC
- Fail safe protection
    - — Programmable watchdog timer
    - — Junction temperature sensor
    - — Non-maskable interrupt
    - — Fault collection unit
- Nexus L2+ interface
- Interrupts
    - — 16 priority level controller
- 16-channel eDMA controller
- General purpose I/Os

— Individually programmable as input, output or special function
- Two general purpose eTimer units
  — Six timers each with up/down count capabilities
  — 16-bit resolution, cascadable counters
  — Quadrature decode with rotation direction flag
  — Double buffer input capture and output compare
- Communications interfaces
  — Two LINFlex channels (LIN 2.1)
  — Four DSPI channels with automatic chip select generation
  — FlexCAN interface (2.0B Active) with 32 message objects
  — Safety port based on FlexCAN with 32 message objects and up to 7.5Mbit/s capability; usable as second CAN when not used as safety port
  — FlexRay™ module (V2.1) with dual or single channel, 32 message objects and up to 10 Mbit/s
- Two 10-bit A/D converters
  — Two × 15 input channels, four channels shared among the two A/D converters
  — Conversion time < 1 µs including sampling time at full precision
  — Programmable Cross Triggering Unit (CTU)
  — Four analog watchdogs with interrupt capability
- On-chip CAN/UART/FlexRay Bootstrap loader with Boot Assist Module (BAM)
- FlexPWM unit
  — Eight complementary or independent outputs with ADC synchronization signals
  — Polarity control, reload unit
  — Integrated configurable dead time unit and inverter fault input pins
  — 16-bit resolution, up to $2 \times f_{CPU}$
  — Lockable configuration
- Clock generation
  — 4–40 MHz main oscillator
  — 16 MHz internal RC oscillator
  — Software controlled FMPLL capable of speeds as fast as 64 MHz
- Voltage supply
  — 3.3 V or 5 V supply for I/Os and ADC
  — On-chip single supply voltage regulator with external ballast transistor
- Operating temperature ranges: –40 to 125 °C or –40 to 105 °C

3.3   Feature details

3.3.1   High performance e200z0 core processor

The e200z0 Power Architecture^{TM} core provides the following features:

- High performance e200z0 core processor for managing peripherals and interrupts
- Single issue 4-stage pipeline in-order execution 32-bit Power Architecture^{TM} CPU
- Harvard architecture
- Variable length encoding (VLE), allowing mixed 16-bit and 32-bit instructions
  — Results in smaller code size footprint
  — Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
  — 1-cycle load latency
  — Misaligned access support
  — No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port
- Non maskable Interrupt support

3.3.2   Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. Requesting masters will be treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- Four master ports:
  — e200z0 core complex Instruction port
  — e200z0 core complex Load/Store Data port

— eDMA

— FlexRay

- Three slave ports:
  - Flash memory (code flash and data flash)
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on Port Master
- Temporary dynamic priority elevation of masters

3.3.3   Enhanced Direct Memory Access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels support independent 8, 16, or 32 bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPI's, ADC, FlexPWM, eTimer and CTU
- Programmable DMA Channel Mux allows assignment of any DMA source to any available DMA channel with as many as 30 potential request sources.
- eDMA abort operation through software

3.3.4   On-chip flash memory with ECC

The MPC5604P provides as much as 576 KB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash memory module interfaces the system bus to a dedicated flash memory array controller. It supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains a four-entry, 4x128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Normal flash memory array accesses are registered and are forwarded to the system bus on the following cycle, incurring 3 wait-states.

The flash memory module provides the following features:

- As much as 576 KB flash memory
  - Eight blocks (32 KB + 2×16 KB + 32 KB + 32 KB + 3×128 KB) code flash
  - Four blocks (16 KB + 16 KB + 16 KB + 16 KB) data flash
  - Full Read While Write (RWW) capability between code and data flash
- Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)
- Typical flash memory access time: 0 wait states for buffer hits, 3 wait states for page buffer miss at 60 MHz
- Hardware managed flash memory writes handled by 32-bit RISC Krypton engine
- Hardware and software configurable read and write access protections on a per-master basis.
- Configurable access timing allowing use in a wide range of system frequencies.
- Multiple-mapping support and mapping-based block access timing (0–31 additional cycles) allowing use for emulation of other memory types.
- Software programmable block program/erase restriction control.
- Erase of selected block(s)
- Read page size of 128 bits (4 words)
- 64-bit ECC with single-bit correction, double-bit detection for data integrity
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Censorship protection scheme to prevent flash memory content visibility
- Hardware support for EEPROM emulation

3.3.5 On-chip SRAM with ECC

The MPC5604P SRAM module provides a general-purpose memory of as much as 40 KB.

ECC handling is done on a 32-bit boundary and is completely software compatible with MPC55xx family devices with an e200z6 core and 64-bit wide ECC.

The SRAM module provides the following features:

- Supports read/write accesses mapped to the SRAM memory from any master
- 40 KB general purpose RAM
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait state for 8- and 16-bit writes if back to back with a read to same memory block

3.3.6 Interrupt Controller (INTC)

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- Eight software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority.
  - Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
- Two external high priority interrupts directly accessing the main core and IOP critical interrupt mechanism

3.3.7 System clocks and clock generation

The following list summarizes the system clock and clock generation on the MPC5604P:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider ($\div 1$, $\div 2$, $\div 4$, $\div 8$)
- FlexPWM module and eTimer module can run on an independent clock source
- On-chip oscillator with automatic level control (tbc)
- Internal 16 MHz RC oscillator for rapid start-up and safe mode
  - Supports frequency trimming by user application

3.3.8 Frequency modulated PLL (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

The PLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock

- Frequency modulated PLL
  - — Modulation enabled/disabled through software
  - — Triangle wave modulation
- Programmable modulation depth (±0.25% to ±4% deviation from center frequency)
  - — Programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation

3.3.9 Main oscillator

The main oscillator provides these features:

- Input frequency range 4 MHz to 40 MHz
- Crystal input mode or Oscillator input mode
- PLL reference

3.3.10 Internal RC oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC Oscillator provides these features:

- Nominal frequency 16MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as systemclock source in case loss oflock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup

3.3.11 Periodic Interrupt Timer Module (PIT)

The PIT module implements these features:

- As many as four general purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel can be used as trigger for a DMA request

3.3.12 System Timer Module

The STM module implements these features:

- 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

3.3.13   Software Watchdog Timer

The SWT has the following features:

- — 32-bit time-out register to set the time-out period
- — Programmable selection of system or oscillator clock for timer operation
- — Programmable selection of window mode or regular servicing
- — Programmable selection of reset or interrupt on an initial time-out
- — Master access protection
- — Hard and soft configuration lock bits
- — Reset configuration inputs allow timer to be enabled out of reset

3.3.14   Fault Collection Unit

The FCU provides an indipendent fault reporting mechanism even in case the CPU is misbehaving. The FCU module has the following features:

- FCU status register reporting the device status
- Continuous monitoring of critical fault signals
- User selection of critical signals from different fault sources inside the device
- Critical fault events trigger two external pins (user selected signal protocol) that can be used externally to reset the device and/or other circuitry (ex: safety relay, Flexray transceiver)
- Faults are latched into a register

3.3.15   System Integration Unit (SIU-Lite)

The MPC5604P SIU-Lite controls MCU pad configuration, external interrupt, general purpose I/O (GPIO), and internal peripheral multiplexing.

The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIU provides the following features:

- Centralized general purpose input output (GPIO) control of as many as 82 input/output pins and 26 analog input-only pads (package dependent)
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins (except ADC channels) can be alternatively configured as both general purpose input or output pins
- ADC channels support alternative configuration as general purpose inputs
- Direct readback of the pin value is supported on all pins through the SIU
- Configurable digital input filter that can be applied to some general purpose input pins for noise elimination
  - — As many as four internal functions can be multiplexed onto one pin

3.3.16 Boot and censorship

Different booting modes are available in the MPC5604P: booting from internal flash memory and booting via a serial link.

The default booting scheme is the one which uses the internal flash memory (an internal pull-down is used to select this mode). The alternate option allows the user to boot via FlexCAN or LINFlex (using the boot assist module software) or via FlexRay.

A censorship scheme is provided to protect the content of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non-volatile memory.

3.3.16.1 Boot Assist Module (BAM)

The BAM is a block of read-only one-time programmed memory and is identical for all MPC5604P devices that are based on the e200z0h core. The BAM program is executed every time the device is powered-on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Serial bootloading via FlexCAN, LINFlex, or FlexRay.
- BAM can accept a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory.

3.3.17 Error Correction Status Module (ECSM)

The ECSM on this device features the following:

- Platform configuration and revision
- ECC error reporting for flash memory and SRAM
- ECC error injection for RAM

3.3.18 CAN (FlexCAN)

The MPC5604P MCU contains one controller area network (FlexCAN) module. This module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. FlexCAN module contains 32 message buffers.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, Version 2.0B
  — Standard data and remote frames
  — Extended data and remote frames
  — 0 to 8 bytes data length
  — Programmable bit rate as fast as 1 Mbit/s

- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- Three programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  — Supports configuration of multiple mailboxes to form message queues of scalable depth
  — Arbitration scheme according to message ID or message buffer number
  — Internal arbitration to guarantee no inner or outer priority inversion
  — Transmit abort procedure and notification
- Receive features
  — Individual programmable filters for each mailbox
  — Eight mailboxes configurable as a six-entry receive FIFO
  — Eight programmable acceptance filters for receive FIFO
- Programmable clock source
  — System clock
  — Direct oscillator clock to avoid PLL jitter

3.3.19   Safety port (FlexCAN)

The MPC5604P MCU has a second CAN controller synthesized to run at high bit rates to be used as a safety port. The CAN module of the safety port provides the following features:

- Identical to the FlexCAN module
- Bit rate as fast as 7.5 Mb at 60 MHz CPU clock using direct connection between CAN modules (no physical transceiver required)
- 32 Message Buffers of 0 to 8 bytes data length
- Can be used as a second independent CAN module

3.3.20   FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1
- 32 configurable message buffers can be handled

- Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
- Message buffers configurable as Tx, Rx or RxFIFO
- Message buffer size configurable
- Message filtering for all message buffers based on FrameID, cycle count and message ID
- Programmable acceptance filters for RxFIFO message buffers

3.3.21   Serial communication interface module (LINFlex)

The LINFlex on the MPC5604P features the following:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 Specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  — Autonomous LIN frame handling
  — Message buffer to store Identifier and as much as 8 data bytes
  — Supports message length as long as 64 bytes
  — Detection and flagging of LIN errors: Sync field; Delimiter; ID parity; Bit; Framing; Checksum and Time-out errors
  — Classic or extended checksum calculation
  — Configurable Break duration as long as 36-bit times
  — Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
  — Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
  — Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features
  — Autonomous LIN header handling
  — Autonomous LIN response handling
- UART mode
  — Full-duplex operation
  — Standard non return-to-zero (NRZ) mark/space format
  — Data buffers with 4-byte receive, 4-byte transmit
  — Configurable word length (8-bit or 9-bit words)
  — Error detection and flagging
  — Parity, Noise and Framing errors
  — Interrupt-driven operation with four interrupt sources
  — Separate transmitter and receiver CPU interrupt sources
  — 16-bit programmable baud-rate modulus counter and 16-bit fractional
  — Two receiver wake-up methods

3.3.22   Deserial serial peripheral interface (DSPI) module

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the MPC5604P MCU and external devices.

The DSPI modules provide these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- As many as eight chip select lines available per DSPI module, depending on package and pin multiplexing, enable 12 external devices to be selected using external muxing from a single DSPI
- Eight clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for de-glitching
- FIFOs for buffering as many as five transfers on the transmit and receive side
- Queueing operation possible through use of the eDMA
- General purpose I/O functionality on pins when not used for SPI

3.3.23   FlexPWM

The pulse width modulator module (PWM) contains four PWM submodules, each capable of controlling a single half-bridge power stage. There are also four fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), Permanent Magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

The FlexPWM block implements the following features:

- 16-bit resolution for center, edge aligned, and asymmetrical PWMs
- PWM outputs can operate as complementary pairs or independent channels
- Can accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
    — Integral reload rates from 1 to 16
    — Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Write protection for critical registers
- Fault inputs can be assigned to control multiple PWM outputs

- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software-control for each PWM output
- All outputs can be programmed to change simultaneously via a "Force Out" event
- PWMX pin can optionally output a third PWM signal from each submodule
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual edge capture functionality
- eDMA support with automatic reload

3.3.24   eTimer

Two eTimer modules are provided, each with six 16-bit general purpose up/down timer/counter per module. The following features are implemented:

- Individual channel capability
  — Input capture trigger
  — Output compare
  — Double buffer (to capture rising edge and falling edge)
  — Separate prescaler for each counter
  — Selectable clock source
  — 0% to 100% pulse measurement
  — Rotation direction flag (Quad decoder mode)
- Maximum count rate
- Counters are cascadeable
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Counters are pre-loadable
- Pins available as GPIO when timer functionality not in use

3.3.25   Analog to digital converter module

The ADC module provides the following features:

Analog part:

- Two on-chip AD converters
  — 10-bit AD resolution

— One sample and hold unit per ADC

— Conversion time, including sampling time, less than 1 μs (at full precision)

— Typical sampling time is 150 ns min. (at full precision)

— Differential non-linearity error (DNL) ±1 LSB

— Integral non-linearity error (INL) ±1.5 LSB

— TUE <3 LSB

— Single-ended input signal range from 0 to 3.3 V

— The ADC and its reference can be supplied with a voltage independent from V_{DDIO}

— The ADC supply can be equal or higher than V_{DDIO}

— The ADC supply and the ADC reference are not independent from each other (they are internally bonded to the same pad)

— Sample times of 2 (default), 8, 64, or 128 ADC clock cycles

Digital part:

- Two × 13 input channels

  — The total 26 channels includes four channels shared among the two converters

- Four analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location,

- Two modes of operation: Normal mode or CTU control mode

- Normal mode features

  — Register-based interface with the CPU: control reg., status reg., one result register per channel

  — ADC state machine managing 3 request flows: regular command, hardware injected command, software injected command

  — Selectable priority between software and hardware injected commands

  — Four analog watchdogs comparing ADC results against predefined levels (low, high, range)

  — DMA compatible interface

- CTU control mode features

  — Triggered mode only

  — Four independent result queues (2 × 16 entries, 2 × 4 entries)

  — Result alignment circuitry (left justified; right justified)

  — 32-bit read mode allows to have channel ID on one of the 16-bit part

  — DMA compatible interfaces

3.3.26   Cross Triggering Unit (CTU)

The Cross Triggering Unit (CTU) allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

It implements the following features:

- Double buffered trigger generation unit with as many as eight independent triggers generated from external triggers
- Trigger generation unit configurable in sequential mode or in triggered mode
- Each Trigger can be appropriately delayed to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with as many as 24 ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows to control ADC channel from each ADC, single or synchronous sampling, independent result queue selection

3.3.27   Junction temperature sensor

The MPC5604P has a junction temperature sensor to allow measuring the temperature of the silicon via the ADC. The junction temperature sensor has these key parameters:

- Nominal temperature range from –40 °C to +150 °C
- Calibrated sensor accuracy:
  — ±10 °C, –40 to 25 °C ambient
  — ±7 °C, 25 to 125 °C ambient

3.3.28   Nexus Development Interface (NDI)

The NDI (Nexus Debug Interface) block provides real-time development support capabilities for the MPC5604P Power Architecture based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI block is an integration of several individual Nexus blocks that are selected to provide the development support interface for this device. The NDI block interfaces to the host processor and internal busses to provide development support as per the IEEE-ISTO 5001-2003 Class 2+ standard. The development support provided includes access to the MCUs internal memory map and access to the processors internal registers during run time.

The Nexus Interface provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)
- Nexus 2+ features supported
  — Static debug
  — Watchpoint messaging
  — Ownership trace messaging
  — Program trace messaging
  — Real time read/write of any internally memory mapped resources through JTAG pins

— Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information

— Watchpoint triggering, watchpoint triggers program tracing

- Auxiliary Output Port
  - Four MDO (Message Data Out) pins
  - MCKO (Message Clock Out) pin
  - Two $\overline{\text{MSEO}}$ (Message Start/End Out) pins
  - $\overline{\text{EVTO}}$ (Event Out) pin
- Auxiliary Input Port
  - $\overline{\text{EVTI}}$ (Event In) pin

3.3.29   IEEE 1149.1 JTAG controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All datainput to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with four pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_ONCE
- Three test data registers: a bypass register, a boundary scan register, and a device identification register.
- A TAP controller state machine thatcontrols the operation of the dataregisters, instruction register and associated circuitry.

3.3.30   On-chip Voltage Regulator (VREG)

The on-chip voltage regulator module provides the following features:

- Uses external NPN transistor
- Regulates external 3.3 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

4   Application examples

4.1   Electric power steering

Figure 2 outlines a typicalelectric power steeringapplication built around theMPC5604P microcontroller.
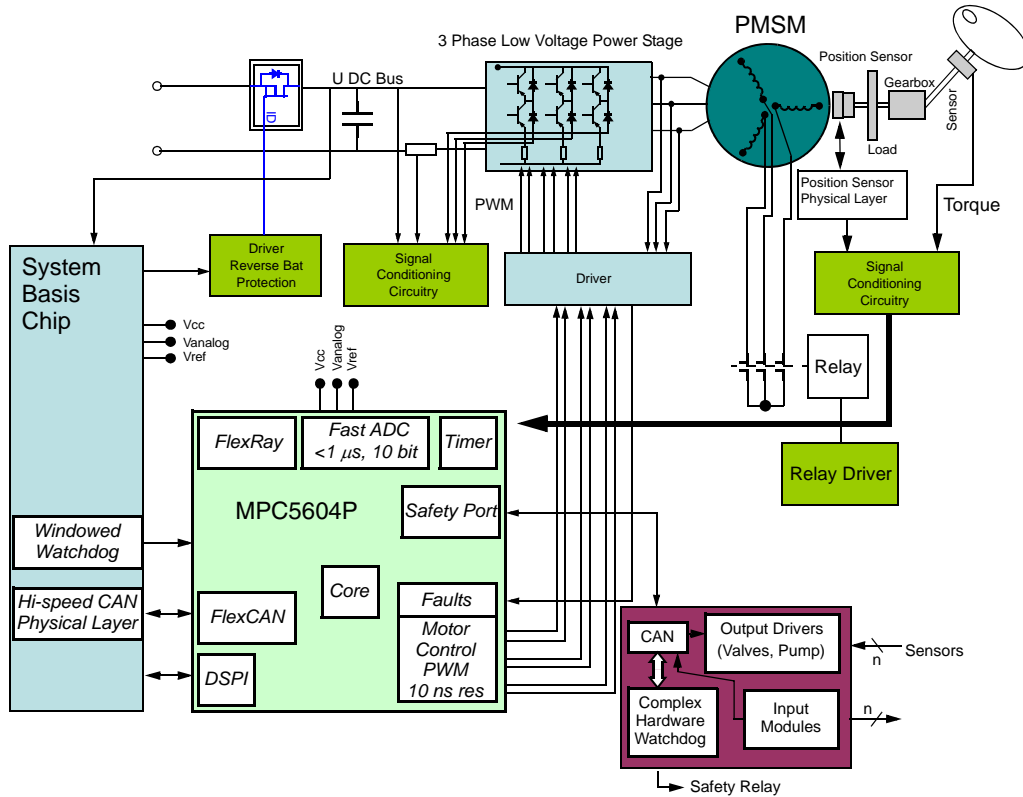
Figure 2. Electric power steering application

4.2 Airbag

outlines a typical airbag application built around the MPC5604P microcontroller.
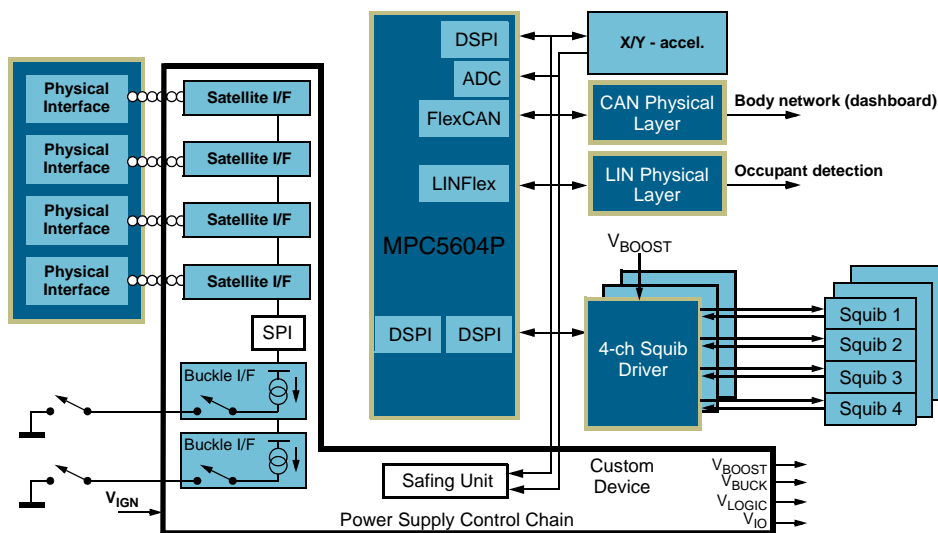
Figure 3. Airbag application

5 Developer environment

The MPC5604P family of MCUs supports tools and third-party developers similar to those used for the Freescale MPC5500 product family, offering a widespread, established network of tools and software vendors. It also features a high-performance Nexus debug interface.

The following development support is available:

- Automotive Evaluation Boards (EVB) featuring CAN, LIN interfaces and more
- Compilers
- Debuggers
- JTAG and Nexus interfaces
- Autocode generation tools
- Initialization tools

The following software support is available:

- Core and peripheral self tests

6 Orderable parts

Table 2. Orderable Part Number Summary

Part Number	Code Flash / Data Flash (EE) (KB)	SRAM (KB)	Package	Characteristics
MPC5604PEFMLQ	512 / 64	40	144 LQFP	FlexRay
MPC5604PEFMLL	512 / 64	40	100 LQFP	FlexRay
MPC5603PEFMLQ	384 / 64	36	144 LQFP	FlexRay
MPC5603PEFMLL	384 / 64	36	100 LQFP	FlexRay

7 Revision history

Table $. Revision history

Revision (Date)	Description
2	Not released; no changes to Rev. 1
3	Not released; no changes to Rev. 1
4 (27 Feb 2009)	Formatting and style corrections. Revised the document to reflect the correct information on the two available devices (with 384 KB and 512 KB flash memory). Removed information about the MPC5602P device. Replaced erroneous 60 MHz core speed with 64 MHz core speed. Consolidated the two feature lists (in the Introduction and Overview sections) into one list (in the Overview section). In the DSPI section, changed the number of chip selects (was up to 4, is up to 8). Added a revision history.
5 (30 Oct 2009)	Editorial changes. In the block diagram: • Removed the Nexus block from the core. • Moved the JTAG block to outside the core. • Move the ECSM block. In the device comparison table: • Added entries for Safety Channel and Data Flash • Changed the flash memory information to indicate only the program flash memory In the feature list: • Replaced "32-bit Power Architecture Book E CPU" with "32-bit Power Architecture™ Book III-E CPU". • Specified LIN 2.1 in communications interfaces feature. • Updated "Available memory" sub-bullet to "As much as 512 KB on-chip code flash memory with additional 64 KB for EEPROM emulation (Data Flash), with ECC, with erase/program controller". • Changed ADC sub-bullet to "Two × 15 input channels, four channels shared among the two A/D converters". In the feature details: • In the ADC section, changed "TUE <1.5 LSB" to "TUE <3 LSB". • In the temperature sensor section, changed "Accuracy of the sensor ±5 °C (tbc)" to "Calibrated sensor accuracy ±5 °C" • In the JTAG section, removed sentence "The size of the boundary scan register is parameterized to support a variety of boundary scan chain lengths." • In the CTU section, changed CTU queue bullet to "4 independent result queues (2 × 16 entries, 2 × 4 entries)". In the orderable parts table: • Renamed the "Flash (KB)" heading column in "Code Flash / Data Flash (EE) (KB)". • Replaced the value of RAM from 32 to 36KB in the last four rows.
No change (5 April 2012)[1]	• Front page: Add SafeAssure branding. • Title and page 1: Add Qorivva branding. • Back page: Apply new back page format.

NOTES:
[1] No substantive changes were made to the content of this document; therefore the revision number was not incremented.