SP3508
Evaluation Board Manual

FEATURES

- Easy Evaluation of SP3508 Multi-Protocol Transceiver
- Eight (8) Drivers and Eight (8) Receivers
- Current Mode V.35 Drivers
- Internal Line or Digital Loopback
- Internal Transceiver Termination Resistors for V.11 and V.35
- Termination Network Disable Option
- Fast 20Mbps Differential Transmission Rates
- Adheres to CTR1/CTR2 Compliancy Requirements
- Interface modes:

RS-232(V.28)	EIA-530(V.10&V.11)
X.21(V.11)	EIA-530A(V.10&V.11)
RS-449/V.36(V.10&V.11)	V.35(V.35&V.28)

DESCRIPTION

The SP3508 Evaluation Board is designed to analyze the SP3508 multi-protocol transceivers. The evaluation board provides access points to all of the driver and receiver I/O pins so that the user can measure electrical characteristics and waveforms of each signal. The SP3508 Evaluation Board also includes a DB-25 serial port connector which is configured to a EIA-530 pinout. This allows easy connections to other DTE or DCE systems as well as network analyzers. The evaluation board also has a set of jumpers to allow the user to select the mode of operation and test the data latch feature. Furthermore, the SP3508 Evaluation Board provides the means to test both local and remote driver/receiver Loopback as well as evaluate the SP3508 in a DCE or DTE configuration.

This Manual is split into sections to give the user the information necessary to perform a thorough evaluation of the SP3508. The Board Schematic and Layout section describes the I/O pins, the jumpers and the other components used on the evaluation board. The board schematic, layout diagram and DB-25 connector are also covered in the Board Schematic and Layout section. The Using the SP3508 Evaluation Board section details the configuration of the SP3508 evaluation board for parametric testing.

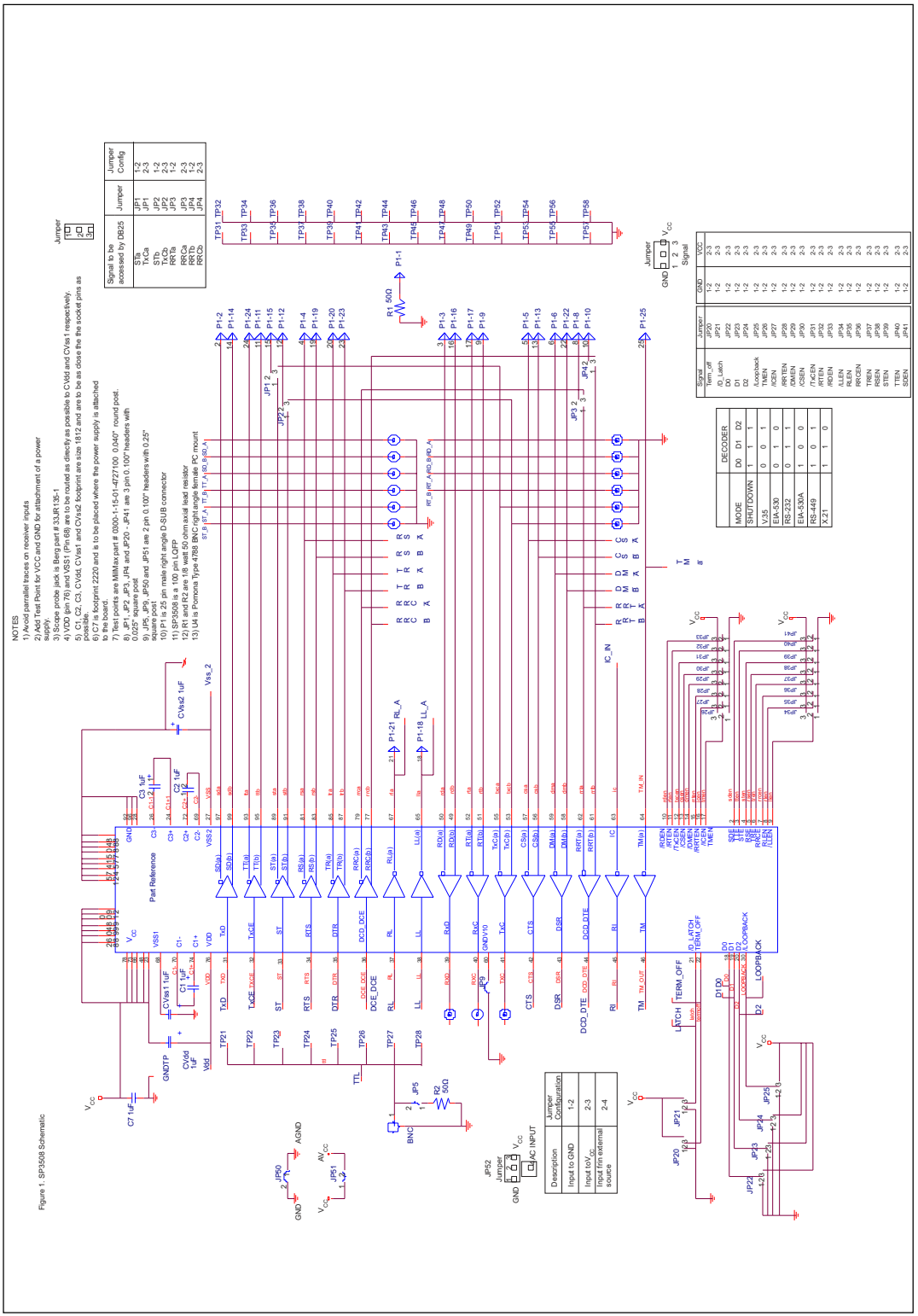

Figure 1

BOARD LAYOUT

1. The SP3508 Evaluation Board has been designed to easily and conveniently provide access to all inputs and outputs under test.

2. Figure 1 is a schematic of the evaluation board. The schematic shows the location of the driver and receiver access points as well as the Jumpers, V_{CC}, GND and the DB-25 Connector.

3. Figure 3 to Figure 6 shows the layout of the SP3508 Evaluation Board.

4. I/O Pinouts
The SP3508 Evaluation Board has been designed to easily and conveniently provide access to all inputs and outputs to the device under test. Each Driver has probe points for the inputs and outputs. Each Receiver has probe points for the inputs and outputs.

5. At the left of the board is a set of jumpers. Each driver and receiver has its own individual enable pin. This set of jumpers controls the enabling and disabling of each driver and receiver. Another set of jumpers is to configure the 3 bit decoder, to enable/disable loopback, to enable/disable latch and to enable/disable term_off functions. In addition, JP1 - JP4 allow the user to choose which signals the user can access through the DB-25 connector. JP5 allows the user to set the driver input to GND, V_{CC} or external source.

6. Also located on the SP3508 evaluation board are six 1uf charge pump capacitors, a 1μF bypass capacitor for V_{CC} and two 50Ω termination resistors.

7. 1 Pomona BNC female connector is mounted on the board to provide input signal for evaluation.

8. Figure 2 shows a RS-232 & EIA530 DB-25 Connector.

9. Table 1 shows the pinout of the DB-25 connector used to connect to a communication analyzer such as the TTC Firebird 6000.

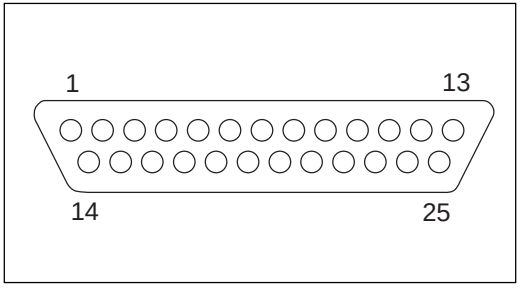

Figure 2. RS-232 & EIA530 Connector (ISO 2110), DTE Connector σ DB-25 Male, DCE Connector σ DB-25 Female

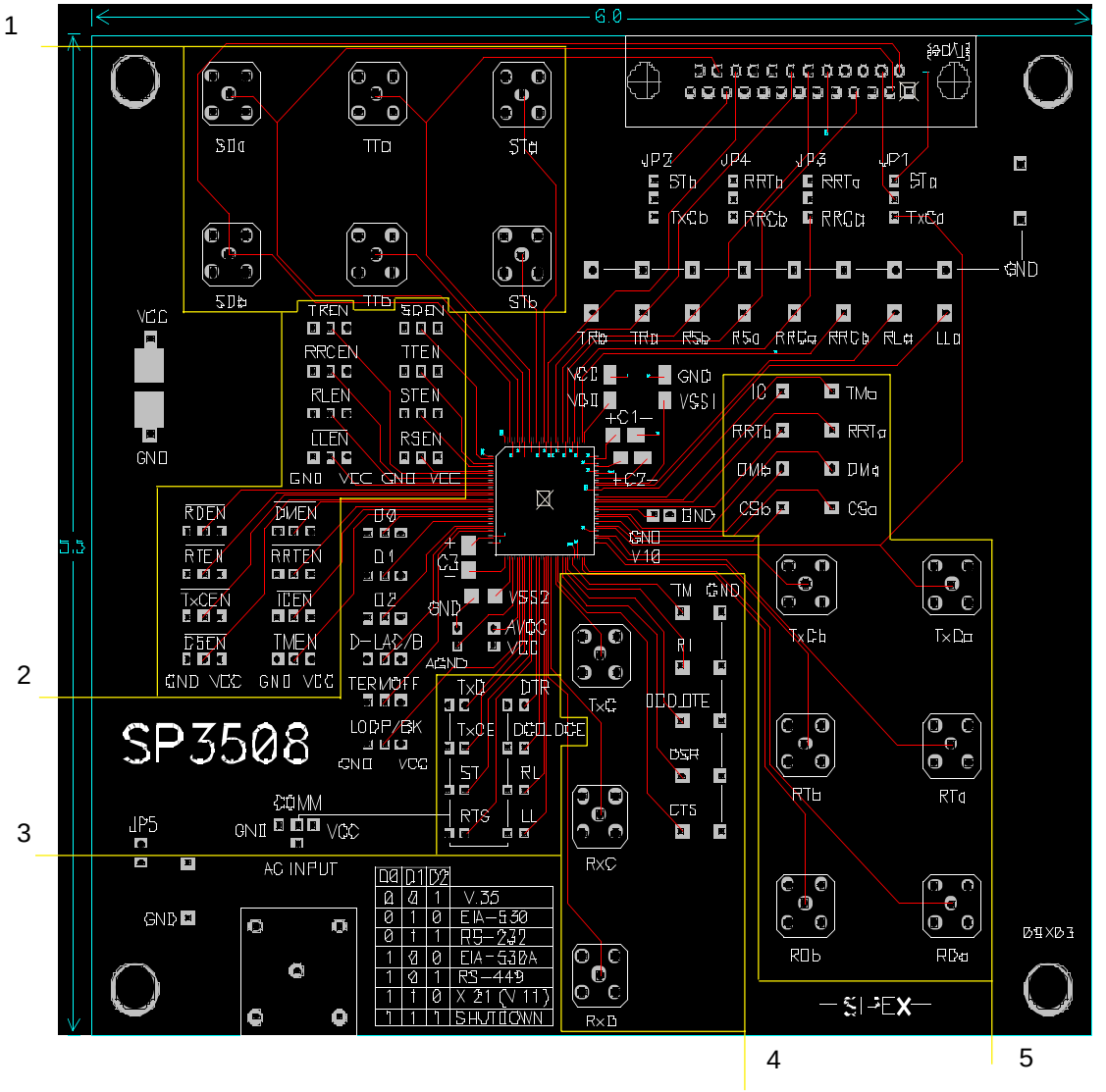

Figure 3. SP3508 Evaluation Board Layout

Note	Configuration
1	Transmitter Outputs
2	Transmitter and Receiver Enable Pins
3	Transmitter Inputs
4	Receiver Outputs
5	Receiver Inputs

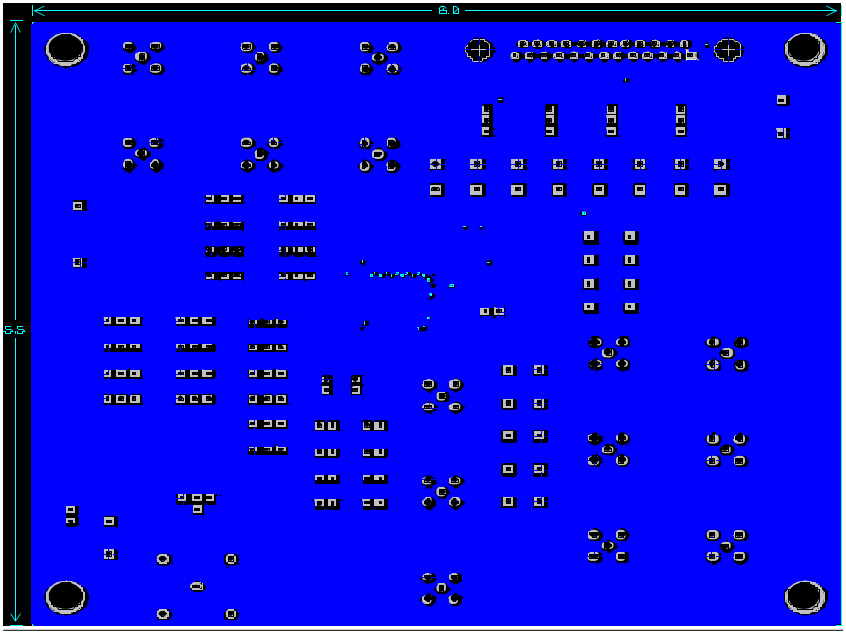

Figure 4. SP3508 Evaluation Board Ground Plane

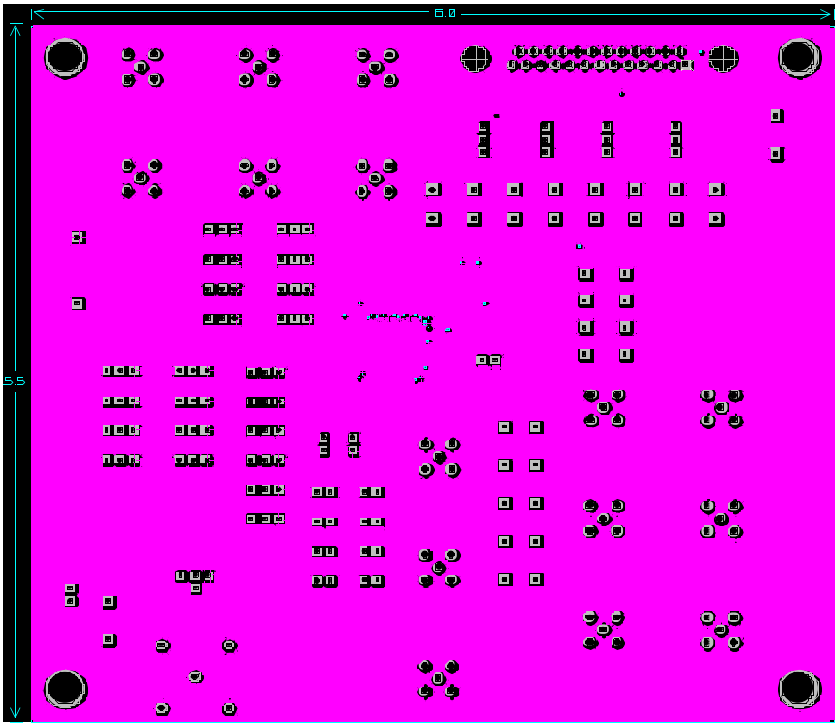

Figure 5. SP3508 Evaluation Board V_{CC} Plane

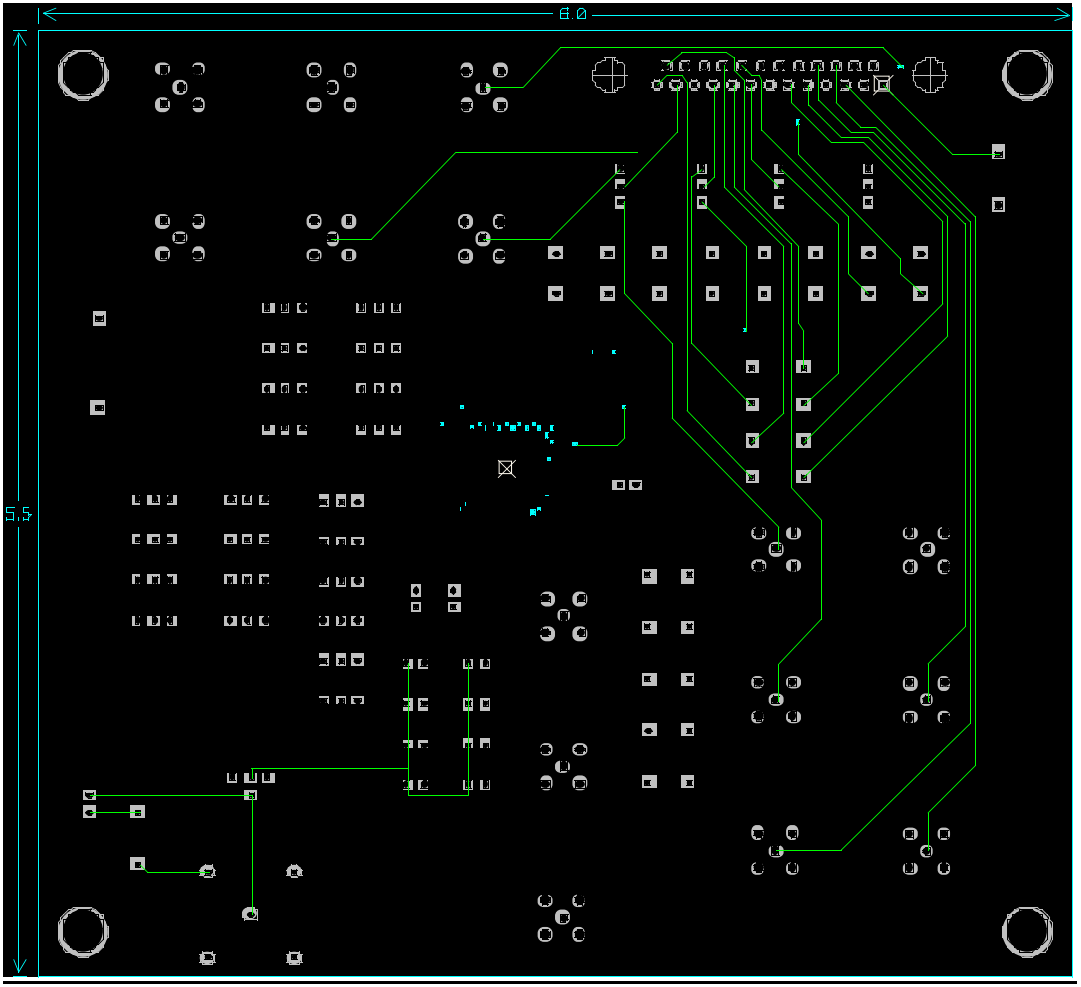

Figure 6. SP3508 Evaluation Board Layout Bottom Layer

TABLE 1.

		EIA-232		EIA-530		EIA-449		V.35		X.21	
Signal Name	**source**	**Mnemonic**	**Pin**	**Mnemonic**	**Pin**	**Mnemonic**	**Pin**	**Mnemonic**	**Pin**	**Mnemonic**	**Pin**
Shield	—	—	1	—	1	—	1	—	A	—	1
Transmitted data	DTE	BA	2	BA(A)	2	SD(A)	4	103	P	Circuit T(A)	2
				BA(B)	14	SD(B)	22	103	S	Circuit T(B)	9
Received Data	DCE	BB	3	BB(A)	3	RD(A)	6	104	R	Circuit R(A)	4
				BB(B)	16	RD(B)	24	104	T	Circuit R(B)	11
Request To Send	DTE	CA	4	CA(A)	4	RS(A)	7	105	C	Circuit C(A)	3
				CA(B)	19	RS(B)	25			Circuit C(B)	10
Clear To Send	DCE	CB	5	CB(A)	5	CS(A)	9	106	D	Circuit I(A)	5
				CB(B)	13	CS(B)	27			Circuit I(B)	12
DCE Ready (DSR)	DCE	CC	6	CC(A)	6	DM(A)	11	107	E		
				CC(B)	22	DM(B)	29				
DTE Ready (DTR)	DTE	CD	20	CD(A)	20	TR(A)	12	108	H*		
				CD(B)	23	TR(B)	30				
Signal Ground	—	AB	7	AB	7	SG	19	102	B	Circuit G	8
Recv. Line Sig. Det. (DCD)	DCE	CF	8	CF(A)	8	RR(A)	13	109	F		
				CF(B)	10	RR(B)	31				
Trans. Sig. Elemt. Timing	DCE	DB	15	DB(A)	15	ST(A)	5	114	Y	Circuit S(A)	6
				DB(B)	12	ST(B)	23	114	AA	Circuit S(B)	13
Recv. Sig.	DTE	RL	17	DD(A)	17	RT(A)	8	115	V	Circuit B(A)**	7
Elemt. Timing				DD(B)	9	RT(B)	26	115	X	Circuit B(B)**	14
Local Loopback	DCE	DD	18	LL	18	LL	10	141	L*		
Remote Loopback	DTE	LL	21	RL	21	RL	14	140	N*		
Ring Indicator	DCE	CE	22	—	—	—	—	125	J*		
Trans. Sig. Elemt. Timing	DTE	DA	24	DA(A)	24	TT(A)	17	113	U*	Circuit X(A)**	7
				DA(B)	11	TT(B)	35	113	W*	Circuit X(B)**	14
Test Mode	DCE	TM	25	TM	25	TM	18	142	NN*		

* Optional signals
** Only one of the two x.21 signals, Circuit B or X, can be implemented and active at one time.

Recommended Equipment

- Oscilloscope
- Digital multimeter
- Signal Generator capable of >40MHz
- Communications Analyzer (such as Firebird 6000)

Parametric Evaluation

Located on the board are two pins identified as VCC and SIGNAL GND. Connect VCC to a +3.3V DC supply. If possible limit the supply current to 0.5 to 1.0 Amps. Be sure to have power off when connecting the supply to the board.

SP3508 Decoder

The SP3508 uses a 3 bit decoder to designate the protocol selected. There is also a decoder latch pin available. Table 2 and Table 3 show the decoder modes for the driver and receiver. Upon power up the latch pin needs to be in a transparent state (logic low or floating) or the SP3508 will be in an unknown state. Note that D0, D1, and D2 set as logic high will put the device shutdown overriding all individual enable/disable lines and the drivers outputs and receiver inputs will tri-state. In shutdown mode the termination resistors also disconnect.

Driver Evaluation

Each driver has an internal pull-up; therefore, it is in a defined state when the input is open. Connect a system clock or a signal generator with a TTL-level output and the appropriate frequency within the acceptable range of the driver to the input BNC connector. Set the jumper to the desired driver input to be evaluated. There is an individual enable line for each driver that can be used to tri-state the driver. Each enable line has an internal pull up or pull down to insure the driver is enabled if the enable pin is not connected or floating. Set the appropriate jumper to enable the driver under test. Once the power is on and the driver input receives a signal, the driver outputs can be analyzed with an oscilloscope or a digital multimeter. Mode selection can be performed at any time by changing the jumper settings for the 3 bit decoder (D0-D2). The appropriate termination for the driver under test can be added to driver output and tied to the ground bus.

Receiver Evaluation

The SP3508 receivers have internal termination appropriate for V.35 and RS-422 modes (refer to the SP3508 datasheet for more detail on the receiver termination). This is activated when the receiver is set to act as a V.11 receiver (see Table 3) and the TERM_OFF pin is logic “0”. Each receiver has a fail-safe feature that outputs a logic “1” when the receiver is open, terminated but open, or shorted together. There is an individual enable line for each receiver that can be used to tri-state the receiver. Each enable line has an internal pull up or pull down to insure the receiver is enabled if the enable pin is not connected or floating. Set the appropriate jumper to enable the receiver under test. The mode selection can be performed at any time after power up by changing the state of the 3 bit decoder (D0-D2). To evaluate the receiver the appropriate input signal needs to be applied. This can be accomplished by providing a signal from an external source or use the SP3508 driver output and jumper it to the receiver input. For single ended receivers, tie the active driver output to the active receiver input. For differential drivers, tie the “A” driver output to the “A” receiver input and the “B” driver output to the “B” receiver input. Using the TTL signal on the driver input will allow the user to analyze receiver levels and timing characteristics.

Driver/Receiver Remote Loopback

The following example uses the ST driver looped back into the TxC receiver. Use the 3 bit decoder to configure the SP3508 for the desired protocol. Connect a jumper cable between the ST(a) pin and the TxC(a) pin. If your mode select is set for a differential driver/receiver, then also connect a jumper cable between the ST(b) pin and the TxC(b) pin. The next step is to connect a signal generator to the ST input pin through BNC input connector. The signal generator output must be a TTL-level output at a frequency within the acceptable range of the driver mode under test. Be sure that the jumper settings of STEN signal and TxCEN signal are set to enable the ST driver and TxC receiver. The driver outputs are now connected back to the receiver inputs so that the driver input to receiver output can be examined. This configuration is similar for all other drivers.

Driver/Receiver Local Loopback

The SP3508 has the ability to provide an internal loopback. This feature is invoked by a logic "0" on the /LOOPBACK pin. The driver input and receiver output characteristics adhere to the appropriate specifications outlined in the datasheet under loopback conditions. The /LOOPBACK pin has an internal pull-up resistor so that the SP3508 defaults to normal operation during power-up or if the pin is left floating.

DCE DTE selectable configuration

• Configure the decoder for the desired mode.

• The SP3508 evaluation board has jumper setup to allow for the evaluation of a selectable DCE DTE configuration.

• Set the STEN and RRCEN to Logic "0". This will disable the ST and RRC driver outputs. (Refer to the Jumper Setting Guide in the next section)

• Set the /TxCEN and /RRTEN to Logic "1". This will disable the TxC and RRT receiver inputs. (Refer to the Jumper Setting Guide in the next section)

• Use an external wire to tie the ST driver outputs to the TxC Receiver inputs.

• Use an external wire to tie the RRC driver outputs to the RRT receiver inputs.

• To enable a DTE configuration, set the STEN and RRCEN to Logic "1". Be sure the TxC and RRT receivers are disabled by setting the /TxCEN and /RRTEN to Logic "1". (Refer to the Jumper Setting Guide in the next section)

• To enable a DCE configuration, set the /TxCEN and /RRTEN to Logic "0". Be sure to disable the ST and RRC driver outputs by setting the STEN and RRCEN to Logic "0". (Refer to the Jumper Setting Guide in the next section)

System Level Evaluation

• Use DB-25 Connector if the evaluation board is configured as a DTE for EIA-530 pinout. In order to connect to other DCE equipment or network analyzers (i.e. the TTC Firebird 6000A), the RxC receiver output must be looped back to the TxCE driver input. The RxD output can also be looped back to the TxD input.

• If connecting the evaluation board to a microcontroller such as the Motorola MC68360, jumper wires of the driver inputs and receiver outputs must connect to the uC's appropriate pins.

TABLE 2

Driver Output Pin	V.35 Mode	EIA-530 Mode	RS-232 Mode (V.28)	EIA-530A Mode	RS-449 Mode (v.36)	X.21 Mode (v.11)	Shutdown	Suggested Signal
MODE (D0,D1,D2)	001	010	011	100	101	110	111	
T1OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxD(a)
T1OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxD(b)
T2OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxCE(a)
T2OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxCE(b)
T3OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxC_DCE(a)
T3OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxC_DCE(b)
T4OUT(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	RTS(a)
T4OUT(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	RTS(b)
T5OUT(a)	V.28	V.11	V.28	V.10	V.11	V.11	High-Z	DTR(a)
T5OUT(b)	High-Z	V.11	High-Z	High-Z	V.11	V.11	High-Z	DTR(b)
T6OUT(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	DCD_DCE(a)
T6OUT(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	DCD_DCE(b)
T7OUT(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	RL
T8OUT(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	LL

TABLE 3

Receiver Input Pin	V.35 Mode	EIA-530 Mode	RS-232 Mode (V.28)	EIA-530A Mode	RS-449 mode (v.36)	X.21 Mode (v.11)	Shutdown	Suggested Signal
MODE (D0,D1,D2)	001	010	011	100	101	110	111	
R1IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	RxD(a)
R1IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	RxD(b)
R2IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	RxC(a)
R2IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	RxC(b)
R3IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxC_DTE(a)
R3IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxC_DTE(b)
R4IN(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	CTS(a)
R4IN(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	CTS(b)
R5IN(a)	V.28	V.11	V.28	V.10	V.11	V.11	High-Z	DSR(a)
R5IN(b)	High-Z	V.11	High-Z	High-Z	V.11	V.11	High-Z	DSR(b)
R6IN(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	DCD_DTE(a)
R6IN(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	DCD_DTE(b)
R7IN(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	RI
R8IN(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	TM

JUMPER SETTING GUIDE

JP52 allows the user to set the driver input to GND, V_{CC} or external source.

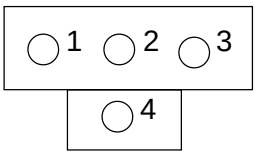

Figure 7. JP52 Jumper Configuration.

TABLE 4. JP52 JUMPER SETTING

Description	Jumper Configuration
Input to GND	1-2
Input to V_{CC}	2-3
Input from External Source	2-4

Figure 8 shows 3-pin jumper configuration and Table 5 describes the fuctionalities of each jumper setting configuration.

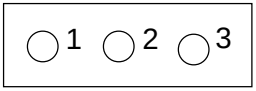

Figure 8. 3-Pin Jumper Configuration

TABLE 5. SP3508 LOGIC JUMPER SETTING

Switch	Jumper	LOGIC 1	LOGIC 2	
D0	JP22	VCC (2-3)	GND (1-2)	DECODER
D1	JP23	VCC (2-3)	GND (1-2)	DECODER
D2	JP24	VCC (2-3)	GND (1-2)	DECODER
LOOPBACK	JP25	VCC (2-3)	GND (1-2)	Logic 0 indicates SP508 is in LOOPBACK mode
TERM_OFF	JP20	VCC (2-3)	GND (1-2)	Logic 1 internal termination is disables
D_LATCH	JP21	VCC (2-3)	GND (1-2)	Logic 0 Latch is disabled
SDEN	JP41	VCC (2-3)	GND (1-2)	Logic 1 TXD driver is enabled
TTEN	JP40	VCC (2-3)	GND (1-2)	Logic 1 TXCE driver is enabled
STEN	JP39	VCC (2-3)	GND (1-2)	Logic 1 ST driver is enabled
RSEN	JP38	VCC (2-3)	GND (1-2)	Logic 1 RTS driver is enabled
TREN	JP37	VCC (2-3)	GND (1-2)	Logic 1 DTR driver is enabled
RRCEN	JP36	VCC (2-3)	GND (1-2)	Logic 1 DCD_DCE driver is enabled
RLEN	JP35	VCC (2-3)	GND (1-2)	Logic 1 SD driver is enabled
/LLEN	JP34	VCC (2-3)	GND (1-2)	Logic 0 LL driver is enabled
/RDEN	JP33	VCC (2-3)	GND (1-2)	Logic 0 RXD receiver is enabled
/RTEN	JP32	VCC (2-3)	GND (1-2)	Logic 0 RXT receiver is enabled
/TXCEN	JP31	VCC (2-3)	GND (1-2)	Logic 0 TXC receiver is enabled
/CSEN	JP30	VCC (2-3)	GND (1-2)	Logic 0 CTS receiver is enabled
/DMEN	JP29	VCC (2-3)	GND (1-2)	Logic 0 DSR receiver is enabled
/RRTEN	JP28	VCC (2-3)	GND (1-2)	Logic 0 DCD_DTE receiver is enabled
/ICEN	JP27	VCC (2-3)	GND (1-2)	Logic 0 RI receiver is enabled
TMEN	JP26	VCC (2-3)	GND (1-2)	Logic 1 TM receiver is enabled

JP1 - JP4 are set of jumpers that the user can select which signals to be accessed by DB25. Figure 9 shows 3-pin jumper configuration and Table 5 describes the signal to be accessed by DB25 per its configuration.

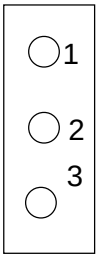

Figure 9. 3-Pin Jumper Configuration

TABLE 6. SP3508 JUMPER SETTINGS

Signal to be accessed by DB25	Jumper	Jumper Configuration
STa	JP1	1-2
TxCa	JP1	2-3
STb	JP2	1-2
TxCb	JP2	2-3
RRTa	JP3	1-2
RRCa	JP3	2-3
RRTb	JP4	1-2
RRCb	JP4	2-3

		SP3508 Pin Designation				
Pin Number	**Pin Name**	**Description**		**Pin Number**	**Pin Name**	**Description**
1	GND	Signal Ground		51	RT(B)	RxC Non-Inverting Input
2	SDEN	TxD Driver Enable Input		52	RT(A)	RxC Inverting Input
3	TTEN	TxCE Driver Enable Input		53	TxC(B)	TxC Non-Inverting Input
4	STEN	ST Driver Enable Input		54	GND	Signal Ground
5	RSEN	RTS Driver Enable Input		55	TxC(A)	TxC Inverting Input
6	TREN	DTR Driver Enable Input		56	CS(B)	CTS Non-Inverting Input
7	RRCEN	DCD Driver Enable Input		57	CS(A)	CTS Inverting Input
8	RLEN	RL Driver Enable Input		58	DM(B)	DSR Non-Inverting Input
9	$\overline{\text{LLEN}}$	LL Driver Enable Input		59	DM(A)	DSR Inverting Input
10	$\overline{\text{RDEN}}$	RxD Receiver Enable Input		60	GNDV10	V.10 Rx Reference Node
11	$\overline{\text{RTEN}}$	RxC Receiver Enable Input		61	RRT(B)	DCD_{DTE} Non-Inverting Input
12	$\overline{\text{TxCEN}}$	TxC Receiver Enable Input		62	RRT(A)	DCD_{DTE} Inverting Input
13	$\overline{\text{CSEN}}$	CTS Receiver Enable Input		63	IC	RI Receiver Input
14	$\overline{\text{DMEN}}$	DSR Receiver Enable Input		64	TM(A)	TM Receiver Input
15	$\overline{\text{RRTEN}}$	DCD_{DTE} Receiver Enable Input		65	LL(A)	LL Driver Output
16	$\overline{\text{ICEN}}$	RI Receiver Enable Input		66	VCC	Power Supply Input
17	TMEN	TM Receiver Enable Input		67	RL(A)	RL Driver Output
18	D0	Mode Select Input		68	VSS1	-2xVCC Charge Pump Output
19	D1	Mode Select Input		69	C2N	Charge Pump Capacitor
20	D2	Mode Select Input		70	C1N	Charge Pump Capacitor
21	$\overline{\text{D\_LATCH}}$	Decoder Latch Input		71	GND	Signal Ground
22	TERM_OFF	Termination Disable Input		72	C2P	Charge Pump Capacitor
23	VCC	Power Supply Input		73	VCC	Power Supply Input
24	C3P	Charge Pump Capacitor		74	C1P	Charge Pump Capacitor
25	GND	Signal Ground		75	GND	Signal Ground
26	C3N	Charge Pump Capacitor		76	VDD	2xVCC Charge Pump Output
27	VSS2	Minus VCC		77	RRC(B)	DCD_{DCE} Non-Inverting Output
28	AGND	Signal Ground		78	VCC	Power Supply Input
29	AVCC	Power Supply Input		79	RRC(A)	DCD_{DCE} Inverting Output
30	$\overline{\text{LOOPBACK}}$	Loopback Mode Enable Input		80	GND	Signal Ground
31	TxD	TxD Driver TTL Input		81	RS(A)	RTS Inverting Output
32	TxCE	TxCE Driver TTL Input		82	VCC	Power Supply Input
33	ST	ST Driver TTL Input		83	RS(B)	RTS Non-Inverting Output
34	RTS	RTS Driver TTL Input		84	GND	Signal Ground
35	DTR	DTR Driver TTL Input		85	TR(A)	DTR Inverting Output
36	DCD_DCE	DCD_{DCE} Driver TTL Input		86	VCC	Power Supply Input
37	RL	RL Driver TTL Input		87	TR(B)	DTR Non-Inverting Output
38	LL	LL Driver TTL Input		88	GND	Signal Ground
39	RxD	RxD Receiver TTL Output		89	ST(A)	ST Inverting Output
40	RxC	RxC Receiver TTLOutput		90	VCC	Power Supply Input
41	TxC	TxC Receiver TTL Output		91	ST(B)	ST Non-Inverting Output
42	CTS	CTS Receiver TTL Output		92	GND	Signal Ground
43	DSR	DSR Receiver TTL Output		93	TT(A)	TxCE Inverting Output
44	DCD_DTE	DCD_{DTE} Receiver TTL Output		94	VCC	Power Supply Input
45	RI	RI Receiver TTL Output		95	TT(B)	TxCE Non-Inverting Output
46	TM	TM Receiver TTL Output		96	GND	Signal Ground
47	GND	Signal Ground		97	SD(A)	TxD Inverting Output
48	VCC	Power Supply Input		98	VCC	Power Supply Input
49	RD(B)	RXD Non-Inverting Input		99	SD(B)	TxD Non-Inverting Output
50	RD(A)	RXD Inverting Input		100	VCC	Power Supply Input

ORDERING INFORMATION

Model	TEMPERATURE	Package
SP3508CF	0°C TO +70°C	100-pin JEDEC LQFP
SP3508CEB	0°C TO +70°C	SP3508 Evaluation Board

ANALOG EXCELLENCE

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