SY58606U

4.25Gbps Precision, 1:2 CML Fanout Buffer with Internal Termination and Fail Safe Input

General Description

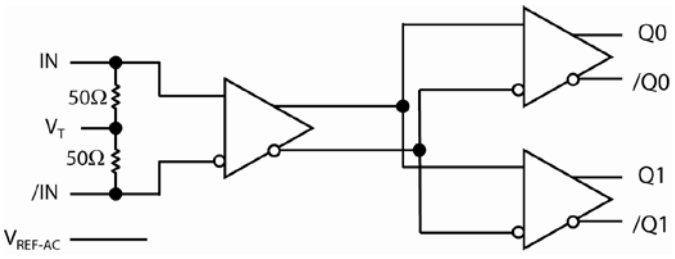
The SY58606U is a 2.5/3.3V, high-speed, fully differential 1:2 CML fanout buffer optimized to provide two identical output copies with less than 15ps of skew and $100fs_{RMS}$ of typical additive phase jitter. The SY58606U can process clock signals as fast as 3GHz or data patterns up to 4.25Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals, (AC- or DC-coupled) as small as 100mV ($200mV_{pp}$) without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an integrated voltage reference (V_{REF-AC}) is provided to bias the V_T pin. The outputs are 400mV CML, with extremely fast rise/fall times guaranteed to be less than 85ps.

The SY58606U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require LVPECL or LVDS outputs, consider Micrel's SY58607U and SY58608U, 1:2 fanout buffers with 800mV and 325mV output swings respectively. The SY58606U is part of Micrel's high-speed, Precision Edge® product line.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram



Features

- Precision 1:2, 400mV CML fanout buffer
- Guaranteed AC performance over temperature and voltage:
  - DC-to > 4.25Gbps throughput
  - <320ps propagation delay (IN-to-Q)
  - <15ps within-device skew
  - <85ps rise/fall times
- Fail Safe Input
  - Prevents outputs from oscillating when input is invalid
- Ultra-low jitter design
  - $100fs_{RMS}$ typical additive jitter
- High-speed CML outputs
- 2.5V ±5% or 3.3V ±10% power supply operation
- Industrial temperature range: –40°C to +85°C
- Available in 16-pin (3mm x 3mm) QFN package

Applications

- Data Distribution: OC-48, OC-48+FEC, XAUI
- SONET clock and data distribution
- Fibre Channel clock and data distribution
- Gigabit Ethernet clock and data distribution

Markets

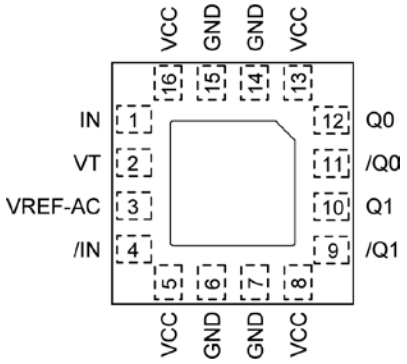
- Storage
- ATE
- Test and measurement
- Enterprise networking equipment
- High-end servers
- Access
- Metro area network equipment

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58606UMG	QFN-16	Industrial	606U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY58606UMGTR[2]	QFN-16	Industrial	606U with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:
1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



16-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair is the differential signal input to the device. Input accepts DC-coupled differential signals as small as 100mV (200mV$_{PP}$). Each pin of this pair internally terminates with 50Ω to the VT pin. If the input swing falls below a certain threshold (typical 30mV), the Fail Safe Input (FSI) feature will guarantee a stable output by latching the output to its last valid state. See “Input Interface Applications” section.
2	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section.
3	VREF-AC	Reference Voltage: This output biases to V_{CC}–1.2V. It is used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the VT pin. Bypass with 0.01µF low ESR capacitor to VCC. Maximum sink/source current is ±1.5mA. See “Input Interface Applications” section.
5, 8,13, 16	VCC	Positive Power Supply: Bypass with 0.1uF//0.01uF low ESR capacitors as close to the V_{CC} pins as possible.
6, 7, 14, 15	GND, Exposed Pad	Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pins.
9, 10 11, 12	/Q1, Q1 /Q0, Q0	CML Differential Output Pairs: Differential buffered copies of the input signal. The output swing is typically 400mV. Unused output pair may be left floating with no impact on jitter. See “CML Output Termination” section.

Absolute Maximum Ratings[3]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
CML Output Voltage (V_{OUT}) ..... V_{CC}-1.0V to V_{CC}+0.5V
Current (V_T)
Source or sink on V_T pin ..... ±100mA
Input Current
Source or sink Current on (IN, /IN) ..... ±50mA
Current (V_{REF})
Source or sink current on V_{REF-AC}[6] ..... ±1.5mA
Maximum operating Junction Temperature ..... 125°C
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[4]

Supply Voltage (V_{IN}) ..... +2.375V to +3.60V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[5]
QFN
Still-air (θ_{JA}) ..... 60°C/W
Junction-to-board (ψ_{JB}) ..... 33°C/W

DC Electrical Characteristics[7]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range		2.375 3.0	2.5 3.3	2.625 3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		60	77	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)	IN, /IN, Note 9	V_{CC}–1.6		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)	IN, /IN	0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 5, Note 8	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing (|IN - /IN|)	See Figure 6	0.2			V
V_{IN_FSI}	Input Voltage Threshold that Triggers FSI			30	100	mV
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V
V_{T_IN}	Voltage from Input to V_T				1.28	V

Notes:
3. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
4. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
5. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
6. Due to the limited drive capability, use for input of the same package only.
7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
8. V_{IN} (max) is specified when V_T is floating.
9. V_{IH} (min) not lower than 1.2V.

CML Outputs DC Electrical Characteristics[10]

V_{CC} = +2.5V ±5% or +3.3V ±10%, R_L = 100Ω across the outputs; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	R_L = 50Ω to V_{CC}	V_{CC}-0.020	V_{CC}-0.010	V_{CC}	V
V_{OUT}	Output Voltage Swing	See Figure 5	325	400		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 6	650	800		mV
R_{OUT}	Output Source Impedance		45	50	55	Ω

Note:
10. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics

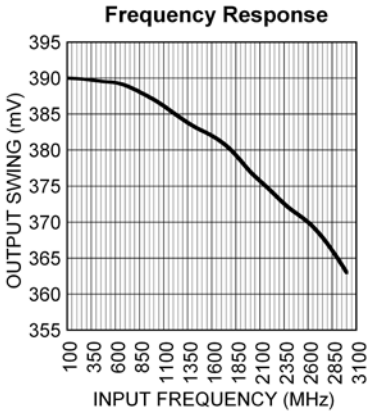
V_{CC} = +2.5V ±5% or +3.3V ±10%, R_L = 100Ω across the outputs, Input t_r/t_f: ≤300ps; T_A = –40°C to +85°C, unless otherwise stated.

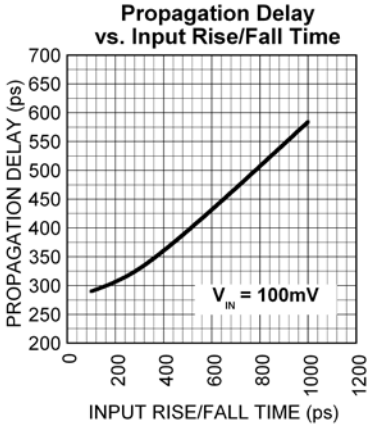
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	NRZ Data	4.25			Gbps
		V_{OUT} > 200mV Clock	2.5	3.0		GHz
t_{PD}	Propagation Delay IN-to-Q	V_{IN}: 100mV-200mV	150	270	400	ps
		V_{IN}: 200mV-800mV	120	220	320	ps
t_{Skew}	Within Device Skew	Note 11		3	15	ps
	Part-to-Part Skew	Note 12			100	ps
t_{Jitter}	Additive Jitter	Carrier = 622MHz Integration Range: 12kHz – 20MHz		100		fs_{RMS}
t_R t_F	Output Rise/Fall Time (20% to 80%)	At full output swing.	30	50	85	ps
	Duty Cycle	Differential I/O	47		53	%

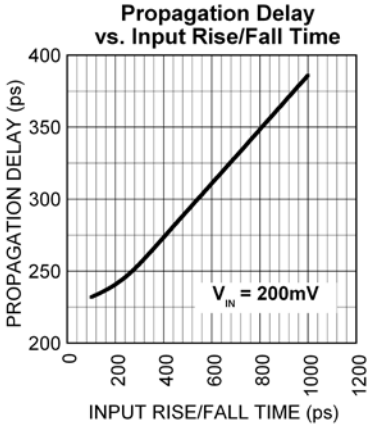
Notes:
11. Within device skew is measured between two different outputs under identical input transitions.
12. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

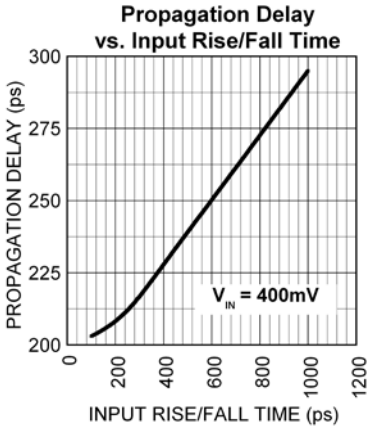
Typical Characteristics

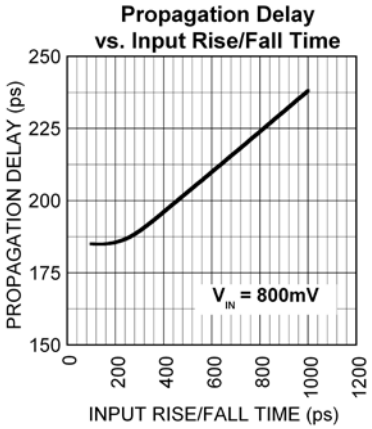
V_{CC} = 3.3V, GND = 0V, V_{IN} = 100mV, R_L = 100Ω across the outputs, T_A = 25°C, unless otherwise stated.











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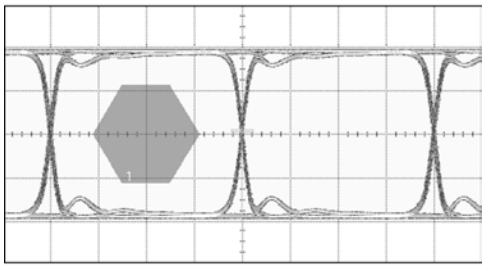
Functional Characteristics

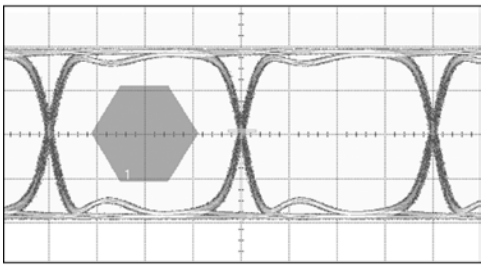
V_{CC} = 2.5V, GND = 0V, V_{IN} = 325mV, Data Pattern: 2^{23}-1, R_L = 100Ω across the outputs, T_A = 25°C, unless otherwise stated.

1.25Gbps Data



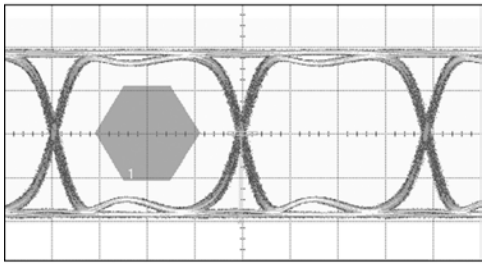
TIME (200ps/div.)

2.5Gbps Data



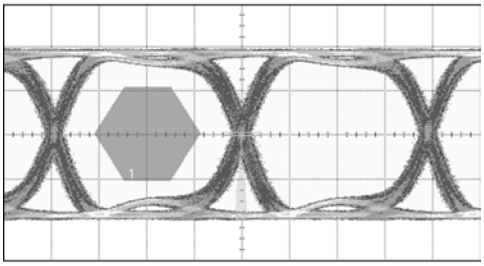
TIME (100ps/div.)

3.2Gbps Data



TIME (80ps/div.)

4.25Gbps Data



TIME (60ps/div.)

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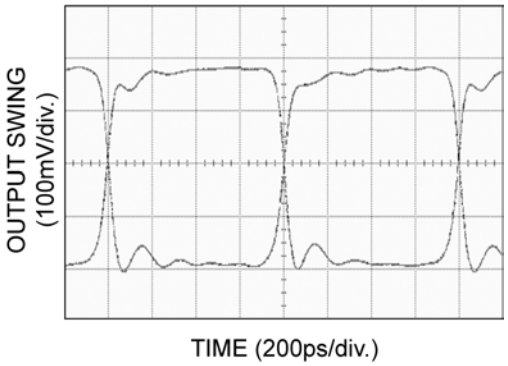
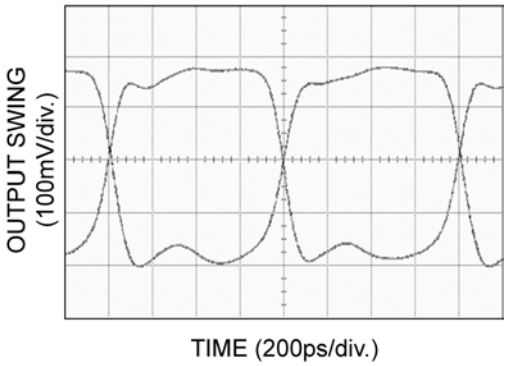
Functional Characteristics (continued)

V_{CC} = 2.5V, GND = 0V, V_{IN} = 325mV, R_L = 100Ω across the outputs, T_A = 25°C, unless otherwise stated.

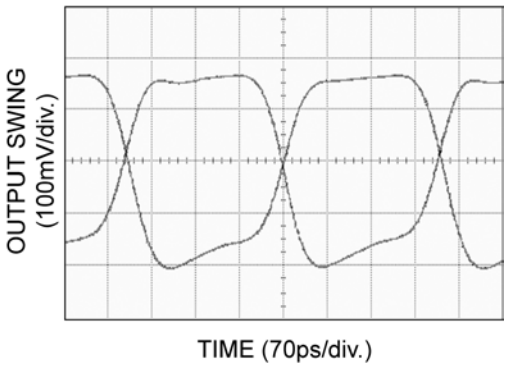
625MHz Clock



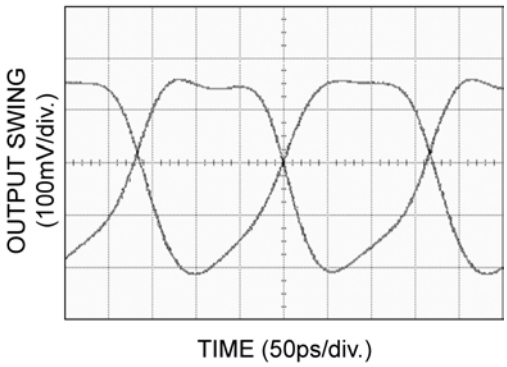
1.25GHz Clock



2GHz Clock



3GHz Clock



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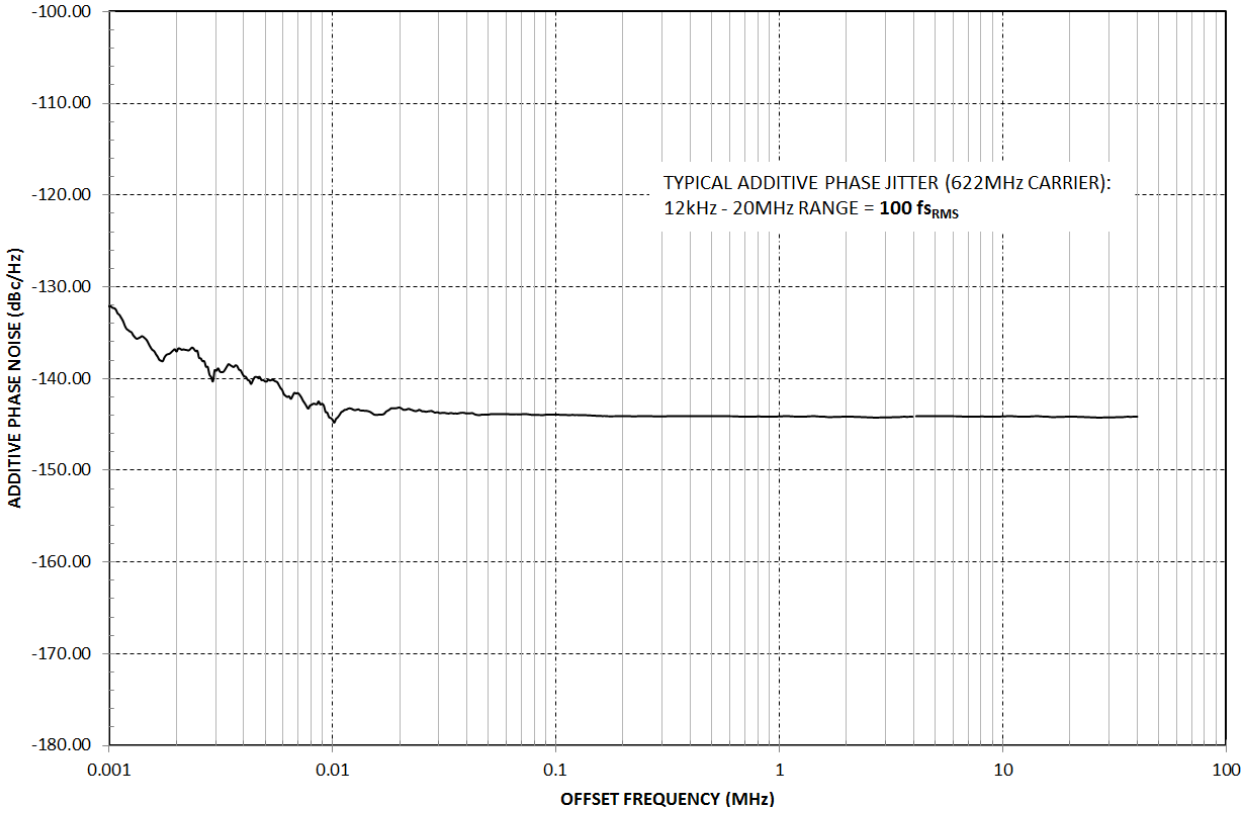
Additive Phase Noise Plot

V_{CC} = +3.3V, T_A = 25°C



Functional Description

Fail-Safe Input (FSI)

The input includes a special fail-safe circuit to sense the amplitude of the input signal and to latch the outputs when there is no input signal present, or when the amplitude of the input signal drops sufficiently below $100mV_{PK}$ ($200mV_{PP}$), typically $30mV_{PK}$. Maximum frequency of SY58606U is limited by the FSI function.

Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing, then the FSI function will eliminate a metastable condition and guarantee a stable output. No ringing and no undetermined state will occur at the output under these conditions.

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to “Typical Characteristics” for detailed information.

Timing Diagrams

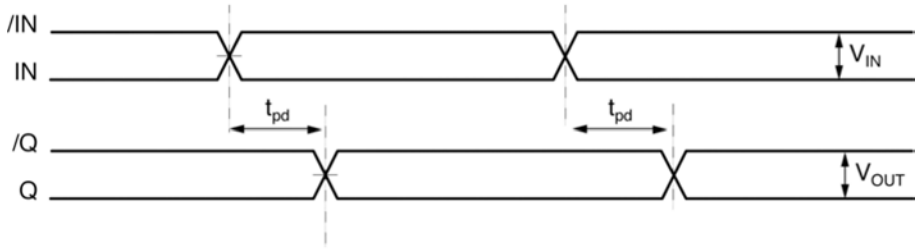


Figure 1. Propagation Delay

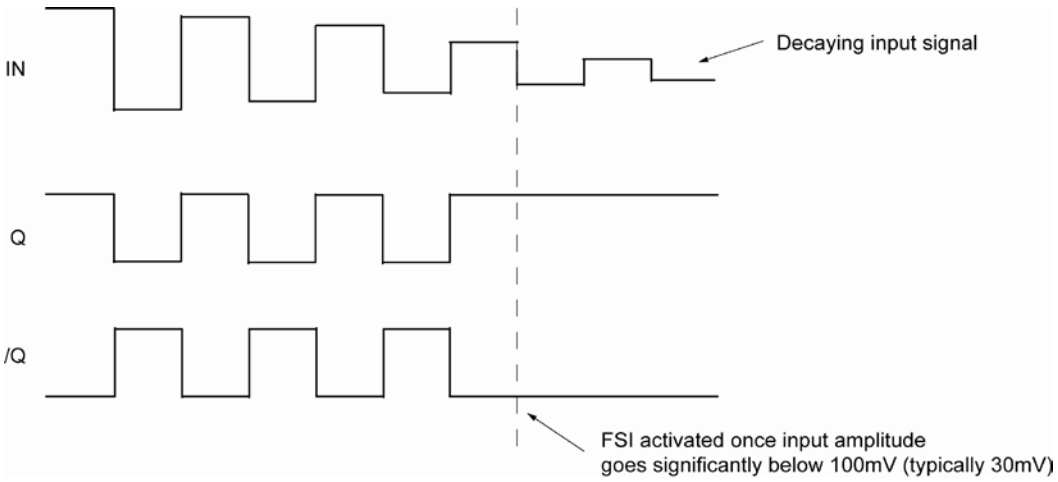


Figure 2 . Fail Safe Feature

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Input and Output Stage

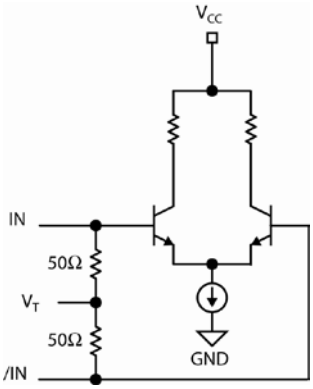

Figure 3. Simplified Differential Input Buffer

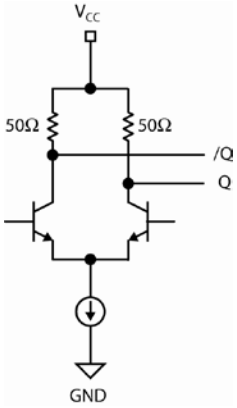

Figure 4. Simplified CML Output Buffer

Single-Ended and Differential Swings

Figure 5. Single-Ended Swing

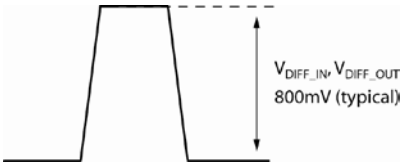

Figure 6. Differential Swing

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Input Interface Applications

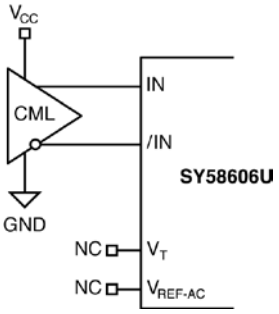

Figure 7. CML Interface (DC-Coupled)
Option: May connect V_T to V_{CC}

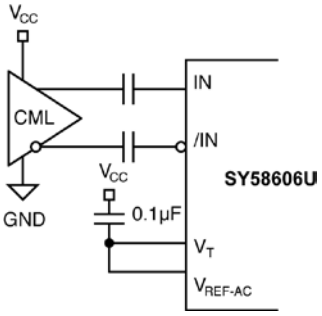

Figure 8. CML Interface (AC-Coupled)

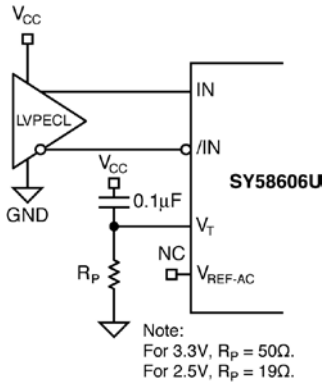

Figure 9. LVPECL Interface (DC-Coupled)

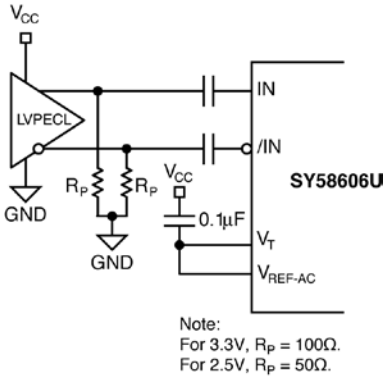

Figure 10. LVPECL Interface (A C-Coupled)

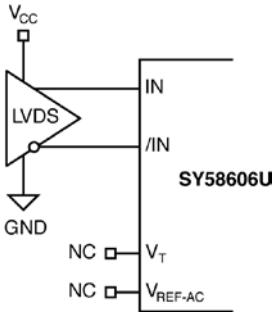

Figure 11. LVDS Interface

CML Output Termination

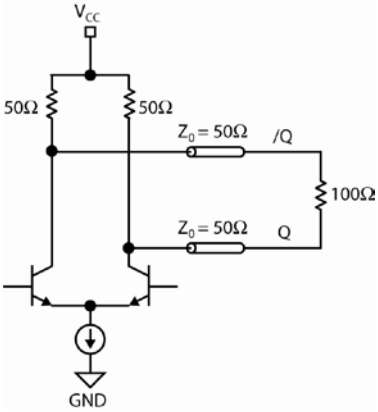

Figure 12. CML DC-Coupled Termination

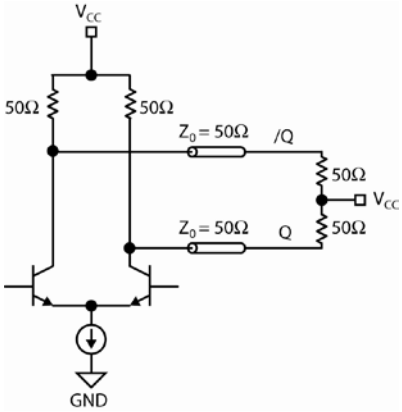

Figure 13. CML DC-Coupled Termination

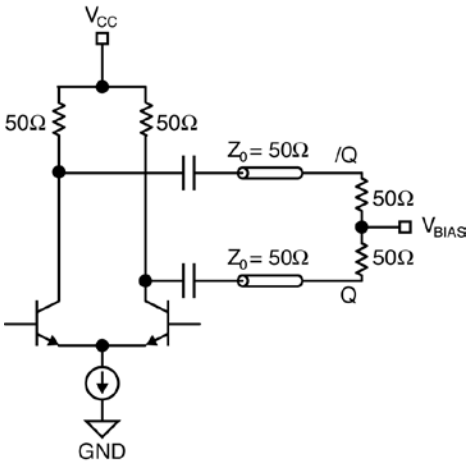

Figure 14. CML AC-Coupled Termination

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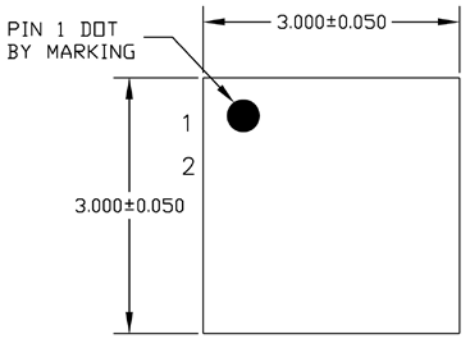
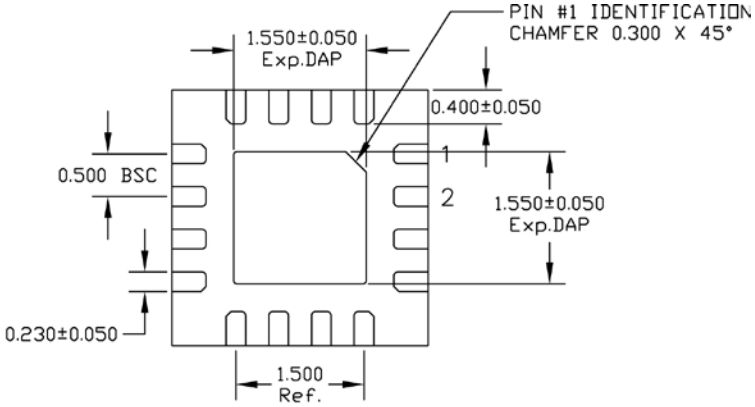
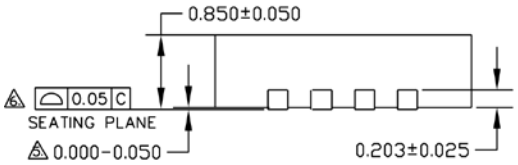
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. APPLIED ONLY FOR TERMINALS.
6. APPLIED FOR EXPOSED PAD AND TERMINALS.

16-Pin QFN

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