AT91SAM9XE-EK Evaluation Board

User Guide

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Section 1

Overview

1.1 Scope

The AT91SAM9XE-EK evaluation kit enables the evaluation of and code development for applications running on an AT91SAM9XE device.

This guide focuses on the AT91SAM9XE-EK board as an evaluation platform.

The board supports the AT91SAM9XE in an LFBGA217 package as well as in a PQFP208 package.

1.2 Deliverables

The AT91SAM9XE-EK package contains the following items:

- an AT91SAM9XE-EK board
- universal input AC/DC power supply with US, UK and Europe plug adapter
- one A/B-type USB cable
- one serial RS232 cable
- one RJ45 crossed Ethernet cable
- one CD-ROM that allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.

1.3 AT91SAM9XE-EK Evaluation Board

The board is equipped with an AT91SAM9XE (217-ball LFBGA package) together with the following:

- 64 Mbytes of SDRAM memory
- 256 Mbytes of NANDFlash memory
- one Atmel serial DataFlash®
- one Atmel TWI serial EEPROM
- one USB device port interface
- two USB Host port interfaces
- one DBGU serial communication port
- one complete MODEM serial communication port
- one additional serial communication port with RTS/CTS handshake control
- JTAG/ICE debug interface
- one PHY Ethernet 100-base TX with three status LEDs
- one Atmel AT73C213 Audio DAC
- one Power LED and one general-purpose LED

- two user input push buttons
- one Wakeup input push button
- one reset push button
- one DataFlash, SD/MMC card slot
- four expansion connectors (PIOA, PIOB, PIOC, IMAGE SENSOR)
- one BGA-like EBI expansion footprint connector
- one Lithium Coin Cell Battery Retainer for 12 mm cell size

Section 2

Setting Up the AT91SAM9XE-EK Board

2.1 Electrostatic Warning

The AT91SAM9XE-EK evaluation board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to set up the AT91SAM9XE-EK evaluation board, the following items are needed:

- the AT91SAM9XE-EK evaluation board itself.
- AC/DC power adapter (5V at 2A), 2.1 mm by 5.5 mm

2.3 Layout

Figure 2-1. AT91SAM9XE-EK Layout-Top View

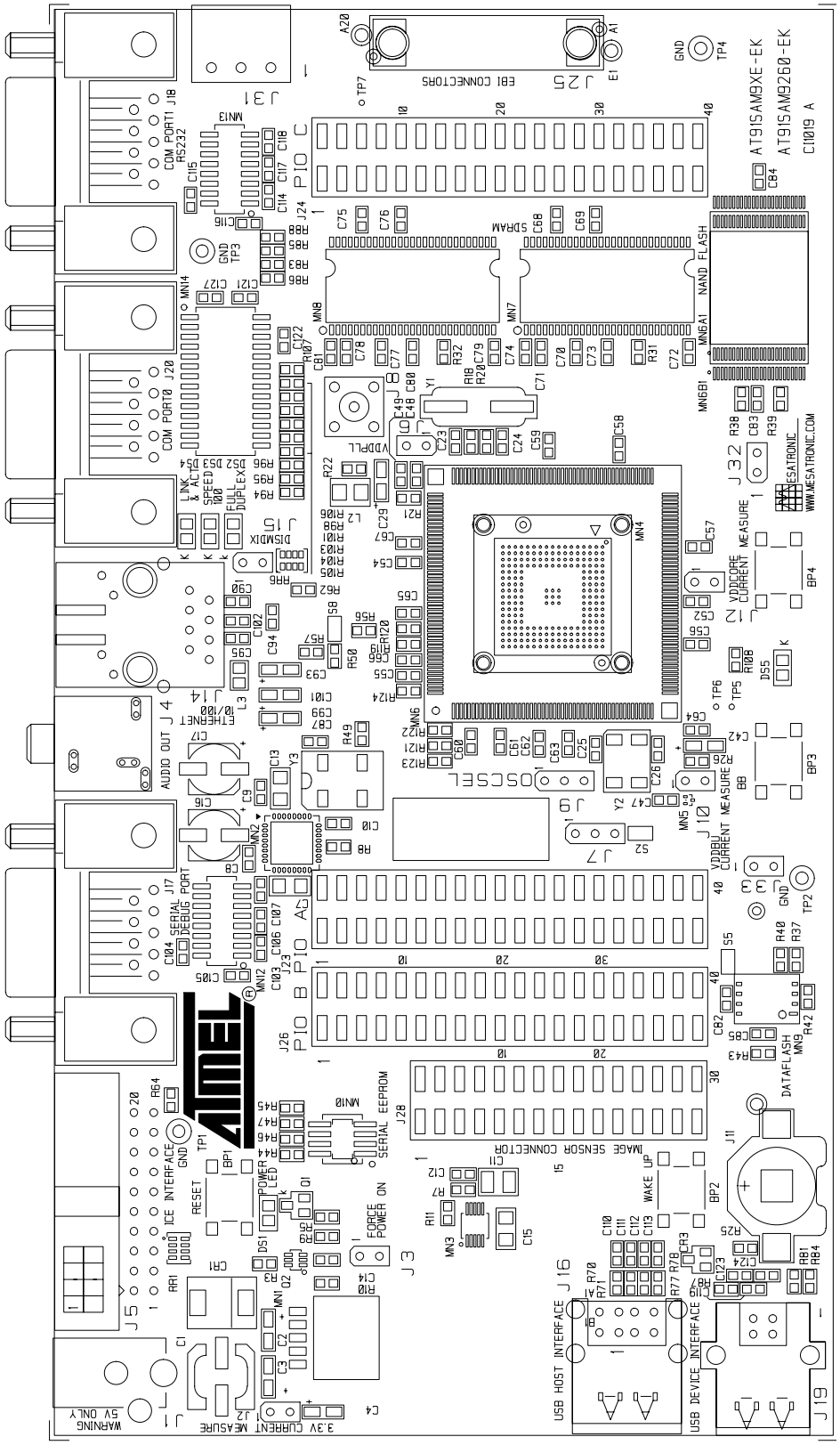
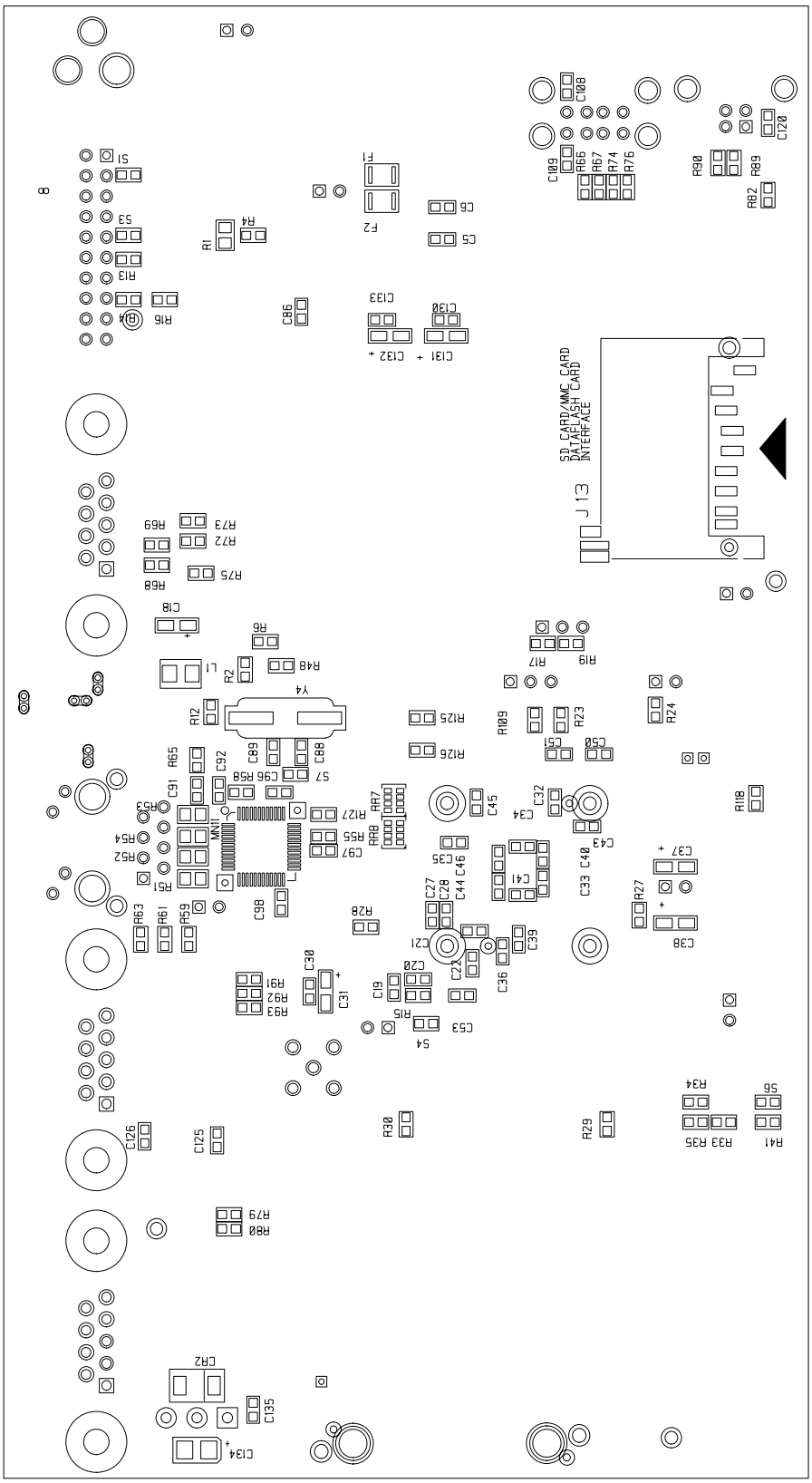


Figure 2-2. AT91SAM9XE-EK Layout - Bottom View



2.4 Powering Up the Board

The AT91SAM9XE-EK requires 5V DC (±5%). DC power is supplied to the board via the 2.1 mm by 5.5 mm socket J1. Coaxial plug center positive standard.

2.5 Backup Power Supply

The user has the possibility to plug a battery (3V Lithium Battery CR1225 or equivalent) in order to permanently power the backup part of the device. In this case, J10 configuration must be set in position 1, 2.

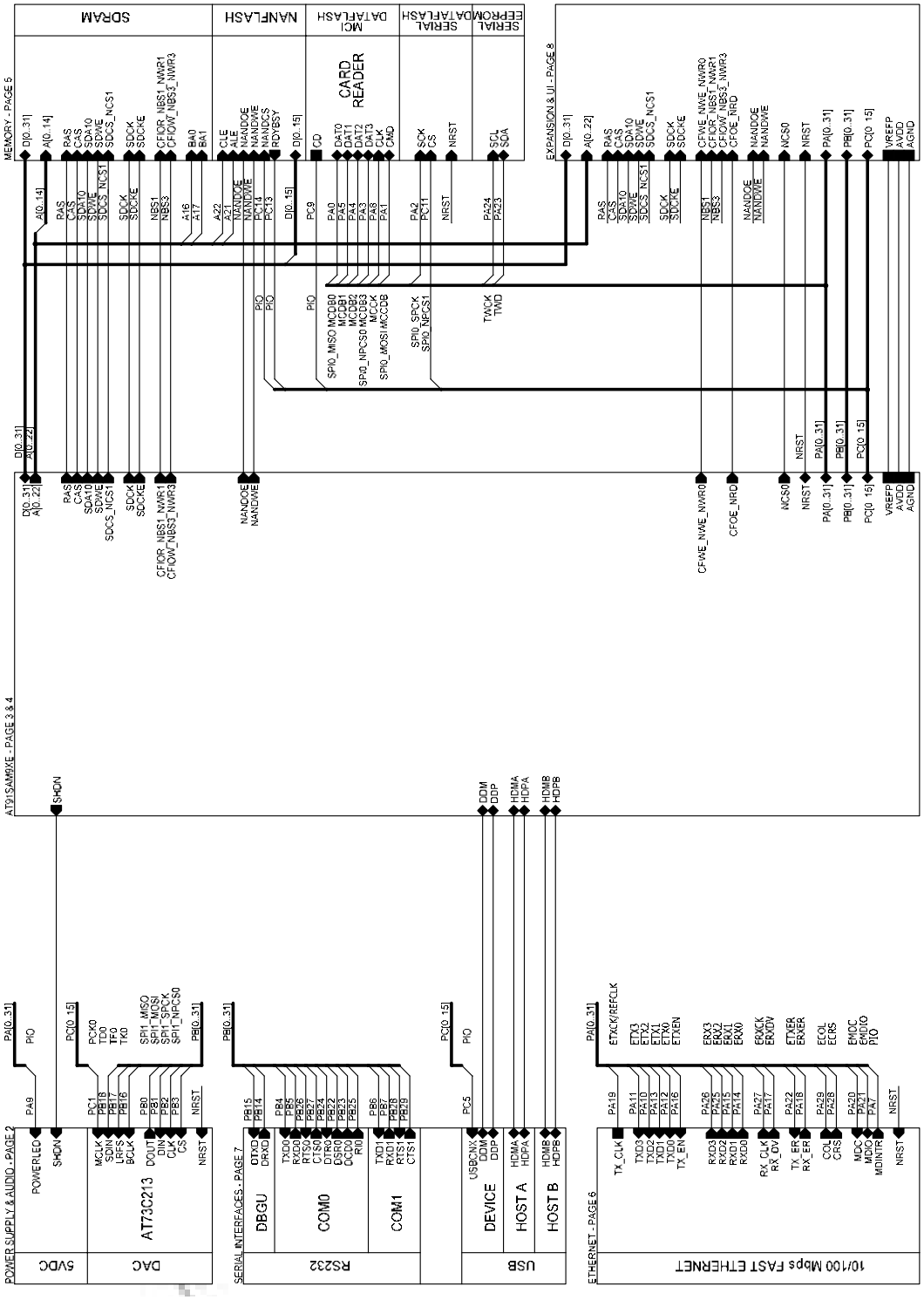
Refer to Section 4.1.

2.6 Getting Started

The AT91SAM9XE-EK evaluation board is delivered with a CD-ROM containing all necessary information and step-by-step procedures for working with the most common development toolchains. Please refer to this CD-ROM, or to the AT91 web site, http://www.atmel.com/products/AT91/, for the most up-to-date information on getting started with the AT91SAM9XE-EK.

2.7 AT91SAM9XE-EK Block Diagram

Figure 2-3. AT91SAM9XE-EK Block Diagram



Section 3

Board Description

3.1 AT91SAM9XE 512/256/128 Microcontroller

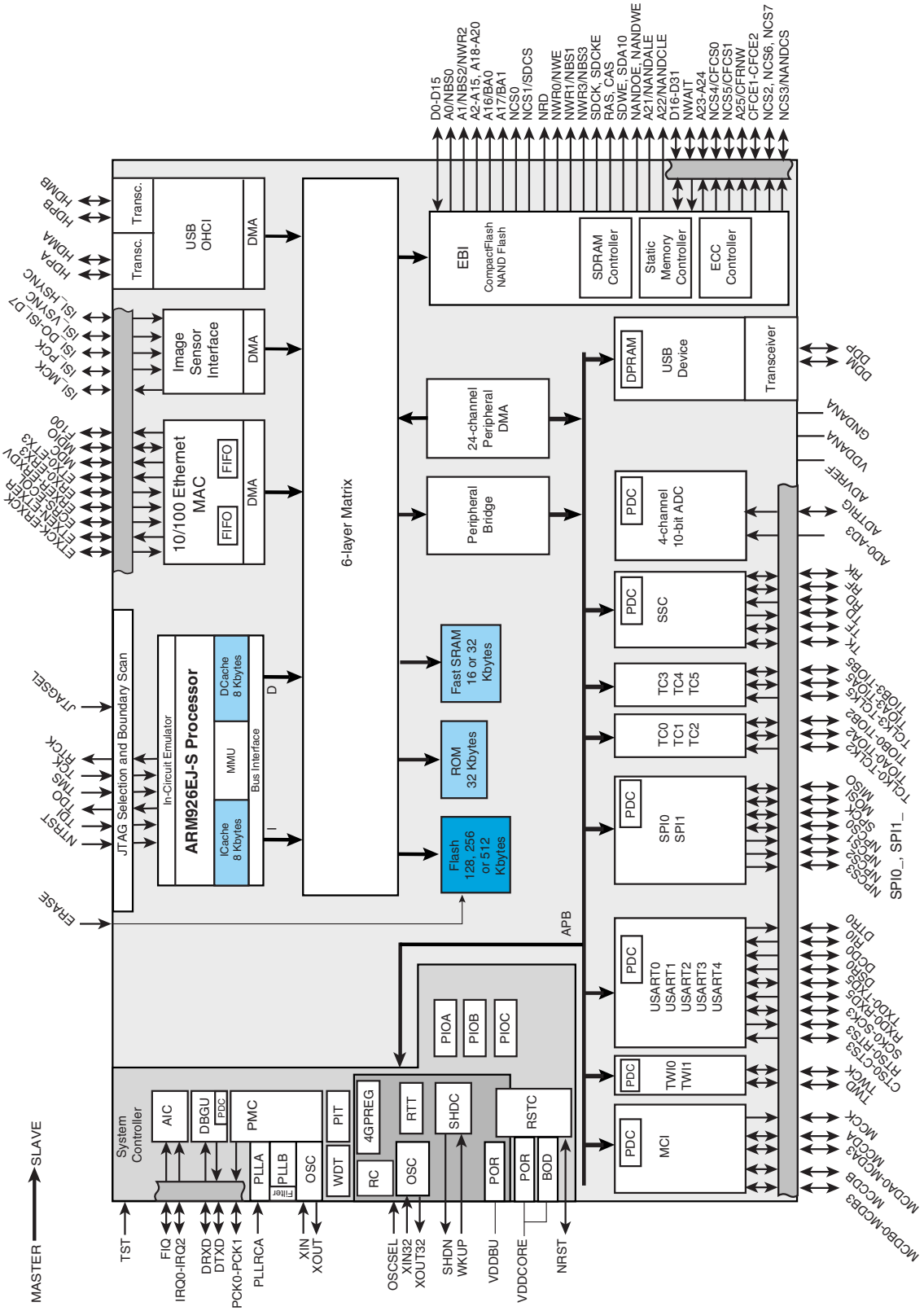
- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP instruction Extensions, ARM Jazelle® Technology for Java® Acceleration
  - 8 Kbyte Data Cache, 16 Kbyte Instruction Cache, Write Buffer
  - 200 MIPS at 180 MHz
  - Memory Management Unit
  - EmbeddedICE™, Debug Communication Channel Support
- Additional Embedded Memories
  - One 32 Kbyte Internal ROM, Single-cycle Access at Maximum Matrix Speed
  - One 32 Kbyte (for AT91SAM9XE256 and AT91SAM9XE512) or 16 Kbyte (for AT91SAM9XE128) Internal SRAM, Single-cycle Access at Maximum Matrix Speed
  - 128, 256 or 512 Kbytes of Internal High-speed Flash for AT91SAM9XE128, AT91SAM9XE256 or AT91SAM9XE512 Respectively. Organized in 256, 512 or 1024 Pages of 512 Bytes Respectively.
    - 128-bit Wide Access
    - Fast Read Time: 60 ns
    - Page Programming Time: 4 ms, Including Page Auto-erase, Full Erase Time: 10 ms
    - 10,000 Write Cycles, 10 Years Data Retention, Page Lock Capabilities, Flash Security Bit
- Enhanced Embedded Flash Controller (EEFC)
  - Interface of the Flash Block with the 32-bit Internal Bus
  - Increases Performance in ARM and Thumb Mode with 128-bit Wide Memory Interface
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, ECC-enabled NAND Flash and CompactFlash™
- USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 2,688-byte Configurable Integrated DPRAM
- USB 2.0 Full Speed (12 Mbits per second) Host Single Port in the 208-pin PQFP Device and Double Port in 217-ball LFBGA Device
  - Single or Dual On-chip Transceivers
  - Integrated FIFOs and Dedicated DMA Channels
- Ethernet MAC 10/100 Base-T
  - Media Independent Interface or Reduced Media Independent Interface
  - 28-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- Image Sensor Interface
  - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - 12-bit Data Interface for Support of High Sensibility Sensors
  - SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format
- Bus Matrix
  - Six 32-bit-layer Matrix
  - Remap Command

- Fully-featured System Controller, including
  - Reset Controller, Shutdown Controller
  - Four 32-bit Battery Backup Registers for a Total of 16 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Real-time Timer
- Reset Controller (RSTC)
  - Based on a Power-on Reset Cell, Reset Source Identification and Reset Output Control
- Clock Generator (CKGR)
  - Selectable 32,768 Hz Low-power Oscillator or Internal Low Power RC Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 3 to 20 MHz On-chip Oscillator, One Up to 240 MHz PLL and One Up to 100 MHz PLL
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Two Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and support for Debug Communication Channel, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer Plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Real-Time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- One 4-channel 10-bit Analog to Digital Converter
- Three 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC,)
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- Peripheral DMA Controller Channels (PDC)
- Two-slot Multimedia Card Interface (MCI)
  - SDCard/SDIO and MultiMediaCard™ Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
- One Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Four Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Signal Control on USART0
- One 2-wire UART
- Two Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
  - Synchronous Communications
- Two Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
  - High-Drive Capability on Outputs TIOA0, TIOA1, TIOA2

- Two Two-wire Interfaces (TWI)
  - Master, Multi-master and Slave Mode Operation
  - General Call Supported in Slave Mode
  - Connection to PDC Channel to Optimize Data Transfers in Master Mode Only
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
  - 1.65V to 1.95V for VDDBU, VDDCORE and VDDPLL
  - 1.65V to 3.6V for VDDIOP1 (Peripheral I/Os)
  - 3.0V to 3.6V for VDDIOP0 and VDDANA (Analog-to-digital Converter)
  - Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM (Memory I/Os)
- Available in a 208-pin PQFP Green and a 217-ball LFBGA Green Package

3.2 Block Diagram

Figure 3-1. AT91SAM9XE512/256/128 Block Diagram



3.3 Microcontroller

- One LFBGA 217-ball device fitted on board
- One LQFP 208-lead device footprint

To use the microcontroller in the LQFP package, the user has to unsolder MN4 and solder the PQFP208 microcontroller on the MN6 footprint.

3.4 Memory

- 32 Kbytes of Internal ROM
- 32 Kbyte of Internal SRAM
- 512 Kbytes of Internal High-speed Flash
- Atmel serial DataFlash
- 64 Mbytes of SDRAM memory (32-bit bus width)
- 256 Mbytes of NANDFlash memory (8-bit bus width)
- TWI serial EEPROM

3.5 Clock Circuitry

- 18.432 MHz standard crystal for the embedded oscillator
- Selectable 32768Hz Low-power external standard crystal Oscillator or Internal Low Power RC Oscillator

3.6 Reset Circuitry

- Internal reset controller with bi-directional reset pin
- External reset pushbutton

3.7 Shutdown Controller

- Programmable shutdown and Wake-Up
- Wake-up push button

3.8 Power Supply Circuitry

- On-board 1.8V High Efficiency step-down charge pump regulator with shutdown control
- On-board 3.3V linear regulator with shutdown control

3.9 Remote Communication

- One serial interface (DBGU COM Port) via RS-232 DB9 male socket
- One complete modem serial interface (COM Port 0) via RS-232 DB9 male socket
- One additional serial interface (COM Port 1) with RTS/CTS handshake control via RS-232 DB9 male

socket

- USB V2.0 full-speed compliant, 12 Mbits per second (UDP)
- Two[1] USB Host ports V2.0 full-speed compliant, 12 Mbits per second (UHP)
- One Ethernet 100-base TX with three status LEDs

3.10 Audio Stereo Interface

- One Atmel stereo audio DAC (AT73C213)
- One 32 Ohm/20 mW Stereo Headset output (J4) with master volume and mute controls

3.11 User Interface

- Two user input pushbuttons[2]
- One user green LED
- One yellow power LED (can be also software controlled)

3.12 Debug Interface

- 20-pin JTAG/ICE interface connector
- DBGU COM port

3.13 Expansion Slot

- One DataFlash, SD/MMC card slot
- All I/Os of the AT91SAM9XE are routed to peripheral extension connectors
- All I/Os of the AT91SAM9XE Image Sensor Interface are routed to peripheral extension connectors
- All EBI Signals of the AT91SAM9XE are routed to extension footprint connectors (J25)

This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.

Notes: ***1.*** **Only one available with the 208-lead PQFP package.**

2. **Not available with the 208-lead PQFP package.**

3.14 PIO Usage

Table 3-1. PIO Controller A

I/O Line	Peripheral A	Peripheral B	Comments	Function
PA0	SPI0_MISO	MCDB0		SPI DATAFLASH, SPI/MCI SD/MMC/DATAFLASH Slot
PA1	SPI0_MOSI	MCCDB		(PA0..PA5)
PA2	SPI0_SPCK			
PA3	SPI0_NPCS0	MCDB3		
PA4	RTS2	MCDB2		
PA5	CTS2	MCDB1		
PA6	MCDA0			User LED
PA7	MCCDA			ETHERNET DM9161A MII/RMII (IRQ)
PA8	MCCK			MCI SD/MMC/DATAFLASH Slot
PA9	MCDA1			Power LED
PA10	MCDA2	ETX2		ETHERNET DM9161A MII Interface (PA10..PA11)
PA11	MCDA3	ETX3		
PA12	ETX0			ETHERNET DM9161A RMII Interface (PA12..PA19)
PA13	ETX1			
PA14	ERX0			
PA15	ERX1			
PA16	ETXEN			
PA17	ERXDV			
PA18	ERXER			
PA19	ETXCK			
PA20	EMDC			ETHERNET DM9161A MII/RMII Interface (PA20..PA21)
PA21	EMDIO			
PA22	ADTRG	ETXER		ETHERNET DM9161A MII Interface
PA23	TWD	ETX2		SERIAL EEPROM (SDA)
PA24	TWCK	ETX3		SERIAL EEPROM (SCL)
PA25	TCLK0	ERX2		ETHERNET DM9161A MII Interface (PA25..PA29)
PA26	TIOA0	ERX3	High-Drive	
PA27	TIOA1	ERXCK	High-Drive	
PA28	TIOA2	ECRS	High-Drive	
PA29	SCK1	ECOL		
PA30	SCK2	RXD4		(BP3) User's interface Push Button
PA31	SCK0	TXD4		(BP4) User's interface Push Button

Table 3-2. PIO Controller B

I/O Line	Peripheral A	Peripheral B	Comments	Function
PB0	SPI1_MISO	TIOA3		Audio DAC AT73C213 (MISO)
PB1	SPI1_MOSI	TIOB3		Audio DAC AT73C213 (MOSI)
PB2	SPI1_SPCK	TIOA4		Audio DAC AT73C213 (SPCK)
PB3	SPI1_NPCS0	TIOA5		Audio DAC AT73C213 (Chip Select)
PB4	TXD0			COM PORT 0 (TXD)
PB5	RXD0			COM PORT 0 (RXD)
PB6	TXD1	TCLK1		COM PORT 1 (TXD)
PB7	RXD1	TCLK2		COM PORT 1 (RXD)
PB8	TXD2			
PB9	RXD2			
PB10	TXD3	ISI_D8		(J28) IMAGE SENSOR CONNECTOR (PB10..PB13)
PB11	RXD3	ISI_D9		
PB12	TXD5	ISI_D10		
PB13	RXD5	ISI_D11		
PB14	DRXD			SERIAL DEBUG PORT(RXD)
PB15	DTXD			SERIAL DEBUG PORT(TXD)
PB16	TK0	TCLK3		Audio DAC AT73C213 (BCLK)
PB17	TF0	TCLk4		Audio DAC AT73C213 (LRFS)
PB18	TD0	TIOB4		Audio DAC AT73C213 (SDIN)
PB19	RD0	TIOB5		(J28) IMAGE SENSOR CONNECTOR (CTRL2)
PB20	RK0	ISI_D0		(J28) IMAGE SENSOR CONNECTOR (PB20..PB31)
PB21	RF0	ISI_D1		
PB22	DSR0	ISI_D2		Warning: Shared with COM PORT 0 (PB22..PB27)
PB23	DCD0	ISI_D3		
PB24	DTR0	ISI_D4		
PB25	RI0	ISI_D5		
PB26	RTS0	ISI_D6		
PB27	CTS0	ISI_D7		
PB28	RTS1	ISI_PCK		Warning: Shared with COM PORT 1 (PB28..PB29)
PB29	CTS1	ISI_VSYNC		
PB30	PCK0	ISI_HSYNC		
PB31	PCK1	ISI_MCK		

Table 3-3. PIO Controller C

I/O Line	Peripheral A	Peripheral B	Comments	Function
PC0	AD0	SCK3		
PC1	AD1	PCK0		Audio DAC AT73C213 (MCLK)
PC2	AD2	PCK1		
PC3	AD3	SPI1_NPCS3		
PC4	A23	SPI1_NPCS2		(J28) IMAGE SENSOR CONNECTOR (CTRL1)
PC5	A24	SPI1_NPCS1		USB_CNX (VBUS DETECT)
PC6	TIOB2	CFCE1		
PC7	TIOB1	CFCE2		
PC8	NCS4/CFCS0	RTS3		
PC9	NCS5/CFCS1	TIOB0		
PC10	A25/CFRNW	CTS3		
PC11	NCS2	SPI0_NPCS1		SPI DATAFLASH memory (Chip Select)
PC12	IRQ0	NCS7		
PC13	FIQ	NCS6		NandFlash (RDYBSY)
PC14	NCS3/NANDCS	IRQ2		NandFlash (NANDCS)
PC15	NWAIT	IRQ1		
PC16	D16	SPI0_NPCS2		EBI Data Bus (PC16..PC31)
PC17	D17	SPI0_NPCS3		
PC18	D18	SPI1_NPCS1		
PC19	D19	SPI1_NPCS2		
PC20	D20	SPI1_NPCS3		
PC21	D21	EF100		
PC22	D22	TCLK5		
PC23	D23			
PC24	D24			
PC25	D25			
PC26	D26			
PC27	D27			
PC28	D28			
PC29	D29			
PC30	D30			
PC31	D31			

Section 4

Configuration

4.1 Jumpers

Table 4-1. Jumpers Configuration

Designation	Default Setting	Feature
J2	Closed	3.3V Jumper[1]
J3	Closed	Forces power on. To use the software shutdown control, J3 must be opened. 3V battery backup must be present.
J6	Closed	VDDPLL Jumper[1]
J7	2-3	Erase/Normal operation mode 1-2: Erase entire flash chip 2-3 or open: Normal operating mode
J9	2 - 3	Slow Clock OSCSEL 1-2: Internal RC Oscillator 2-3: External Crystal Oscillator
J10	Closed	VDDBU Jumper[1]
J12	Closed	VDDCORE Jumper[1]
J15	Closed	Enables Ethernet Auto MDIX control
J32	Closed	Enables the use of the embedded NANDFLASH device (MN6xx)
J33	Closed	Enables the use of the embedded DATAFLASH device (MN9)

Notes: ***1.*** These jumpers are provided for power consumption measurement. By default, they are closed. To use this feature, the user has to open the strap and insert an ammeter.

4.2 JTAG/ICE

Table 4-2. JTAG/ICE Configuration

Designation	Default Setting	Feature
S1	Opened	Disables the ICE NTRST input
S2	Opened	Selects ICE mode or JTAG mode
S3	Opened	Disables TCK <-> RTCK local loop. If S3 is closed, R13 must be unsoldered.
R13	Soldered	Enables the ICE RTCK return. S3 must be opened
R14	Soldered	Enables the ICE NRST input

4.3 Microcontroller Clock

Table 4-3. Microcontroller Clock Configuration

Designation	Default Setting	Feature
R18/R20	Soldered	Enables the use of 18.432MHz crystal. If an external clock is used, R18/R20 must be unsoldered and S4 closed.
S4	Opened	
J9		Slow Clock Setting. See Table 4-1.

4.4 Memory Configuration

Table 4-4. Memory Configuration

Designation	Default Setting	Feature
SDRAM		
R31 R32	Soldered Soldered	Enables MN7 Chip select access Enables MN8 Chip select access
NAND Flash (MN6x)		
R34 S6	Soldered Opened	Enables the use of Ready Busy signal Disables write protection.
SERIAL DATAFLASH (MN9)		
S5	Opened	Disables the write protection.
TWI SERIAL EEPROM (MN10)		
R46 R47	Soldered Soldered	Enables SCL access Enables SDA access

4.5 Ethernet

RMII is the factory default mode.

To evaluate the MII mode, the user has to unsolder R49, R50, R127, close S7, S8 and populate R119 to R126, C88, C89, Y4.

4.6 Miscellaneous

Refer to the TOP level schematic for the PIO usage.

Table 4-5. Miscellaneous

Designation	Default Setting	Feature
R82	Soldered	USB DEVICE: Enables the use of the USBCNX signal
R72 R73	Soldered Soldered	DBGU COM Port: Enables the use of DTXD output signal. Enables the use of DRXD input.
		RS232 COM Port 0: Enable the use of output signals.
R94 R95 R96	Soldered	RTS0 TXD0 DTR0
		RS232 COM Port 0: Enable the use of input signals.
R98 R101 R103 R104 R105 R106	Soldered	DCD0 DSR0 RXD0 CTS0 RI0 Enables all MAX3241E outputs buffer
		RS232 COM Port 1: Enables the use of output signals.
R83 R85	Soldered	TXD1 RTS1
		RS232 COM Port 1: Enables the use of input signals.
R86 R88	Soldered	RXD1 CTS1
TP1	N.A	GND Test point
TP2	N.A	GND Test point.
TP3	N.A	GND Test point.
TP4	N.A	GND Test point.
TP5	N.A	Reserved: do not use
TP6	N.A	Reserved: do not use

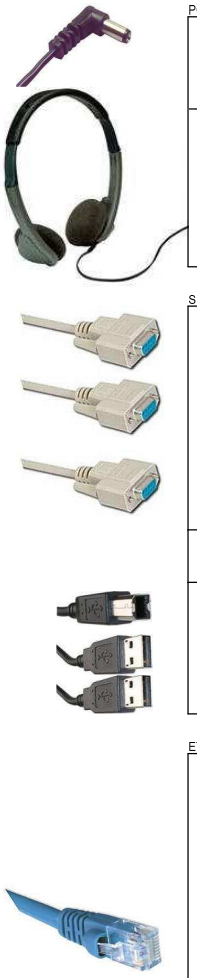
Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- Board Diagram - Schematic Top Level
- Power supply and audio
- 217-ball BGA AT91SAM9XE Microcontroller
- 208-pin LQFP AT91SAM9XE Microcontroller
- Memory
- Ethernet
- Serial Interface
- Expansion and User Interface



POWER SUPPLY & AUDIO - PAGE 2

5VDC
- POWERLED ← PA9 ← PA[0..31] PIO
- SHDN → SHDN (AT91SAM9XE - PAGE 3 & 4)

DAC — AT73C213
- MCLK ← PC1 ← PC[0..15] PCK0
- SDIN ← PB18 TD0
- LRFS ← PB17 TF0
- BCLK ← PB16 TK0
- DOUT → PB0 SPI1_MISO
- DIN ← PB1 SPI1_MOSI
- CLK ← PB2 SPI1_SPCK
- CS ← PB3 SPI1_NPCS0
- NRST ← NRST ← PB[0..31]

SERIAL INTERFACES - PAGE 7

RS232
- DBGU: DTXD ← PB15 ← PB[0..31]; DRXD → PB14
- COM0: TXD0 ← PB4; RXD0 → PB5; RTS0 ← PB26; CTS0 → PB27; DTR0 ← PB24; DSR0 ← PB22; DCD0 ← PB23; RI0 → PB25
- COM1: TXD1 ← PB6; RXD1 → PB7; RTS1 ← PB28; CTS1 → PB29

USB
- DEVICE: USBCNX ← PC5 ← PC[0..15] PIO; DDM ↔ DDM; DDP ↔ DDP
- HOST A: HDMA ↔ HDMA; HDPA ↔ HDPA
- HOST B: HDMB ↔ HDMB; HDPB ↔ HDPB

ETHERNET - PAGE 6

10/100 Mbps FAST ETHERNET
- TX_CLK ← PA19 ← PA[0..31] ETXCK/REFCLK
- TXD3 ← PA11 ETX3
- TXD2 ← PA10 ETX2
- TXD1 ← PA13 ETX1
- TXD0 ← PA12 ETX0
- TX_EN ← PA16 ETXEN
- RXD3 → PA26 ERX3
- RXD2 → PA25 ERX2
- RXD1 → PA15 ERX1
- RXD0 → PA14 ERX0
- RX_CLK → PA27 ERXCK
- RX_DV → PA17 ERXDV
- TX_ER ← PA22 ETXER
- RX_ER → PA18 ERXER
- COL → PA29 ECOL
- CRS → PA28 ECRS
- MDC ← PA20 EMDC
- MDIO ↔ PA21 EMDIO
- MDINTR → PA7 PIO
- NRST ← NRST

AT91SAM9XE - PAGE 3 & 4

- SHDN ← SHDN (POWER SUPPLY & AUDIO - PAGE 2)
- DDM ↔ DDM; DDP ↔ DDP (USB)
- HDMA ↔ HDMA; HDPA ↔ HDPA (USB)
- HDMB ↔ HDMB; HDPB ↔ HDPB (USB)
- D[0..31] ↔ D[0..31]; A[0..22] ↔ A[0..22]
- RAS, CAS, SDA10, SDWE, SDCS_NCS1 → SDRAM
- SDCK, SDCKE → SDRAM
- CFIOR_NBS1_NWR1, CFIOW_NBS3_NWR3 → SDRAM
- NANDOE, NANDWE → NANFLASH
- PIO → PC14, PC13 → NANFLASH
- D[0..15] ↔ NANFLASH
- PIO → PC9 → CARD READER (CD)
- SPI0_MISO MCDB0 ↔ PA0 (DAT0)
- MCDB1 ↔ PA5 (DAT1)
- MCDB2 ↔ PA4 (DAT2)
- SPI0_NPCS0 MCDB3 ↔ PA3 (DAT3)
- MCCK ↔ PA8 (CLK)
- SPI0_MOSI MCCDB ↔ PA1 (CMD)
- SPI0_SPCK → PA2 (SCK) → MCI DATAFLASH
- SPI0_NPCS1 → PC11 (CS) → MCI DATAFLASH
- NRST → NRST → MCI DATAFLASH
- TWCK → PA24 (SCL) → SERIAL EEPROM
- TWD → PA23 (SDA) → SERIAL EEPROM
- CFWE_NWE_NWR0 → NBS1, CFIOR_NBS1_NWR1, CFIOW_NBS3_NWR3, CFOE_NRD, NANDOE, NANDWE
- NCS0 → NCS0
- NRST → NRST
- PA[0..31] ↔ PA[0..31]
- PB[0..31] ↔ PB[0..31]
- PC[0..15] ↔ PC[0..15]
- VREFP, AVDD, AGND → VREFP, AVDD, AGND

MEMORY - PAGE 5

- SDRAM: D[0..31], A[0..14], RAS, CAS, SDA10, SDWE, SDCS_NCS1, SDCK, SDCKE, NBS1, CFIOR_NBS1_NWR1, CFIOW_NBS3_NWR3, A16 → BA0, A17 → BA1
- NANFLASH: A22 → CLE, A21 → ALE, NANDOE, NANDWE, PC14 → NANDCS, PC13 → RDYBSY, D[0..15]
- MCI DATAFLASH: CARD READER (CD, DAT0, DAT1, DAT2, DAT3, CLK, CMD)
- SERIAL DATAFLASH: SCK, CS, NRST
- SERIAL EEPROM: SCL, SDA

EXPANSION & UI - PAGE 8

- D[0..31], A[0..22]
- RAS, CAS, SDA10, SDWE, SDCS_NCS1, SDCK, SDCKE
- CFWE_NWE_NWR0, CFIOR_NBS1_NWR1, CFIOW_NBS3_NWR3, CFOE_NRD, NANDOE, NANDWE
- NCS0, NRST
- PA[0..31], PB[0..31], PC[0..15]
- VREFP, AVDD, AGND

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AT91SAM9XE-EK

DIAGRAM

SCALE 1/1

REV. A

SHEET 1/8

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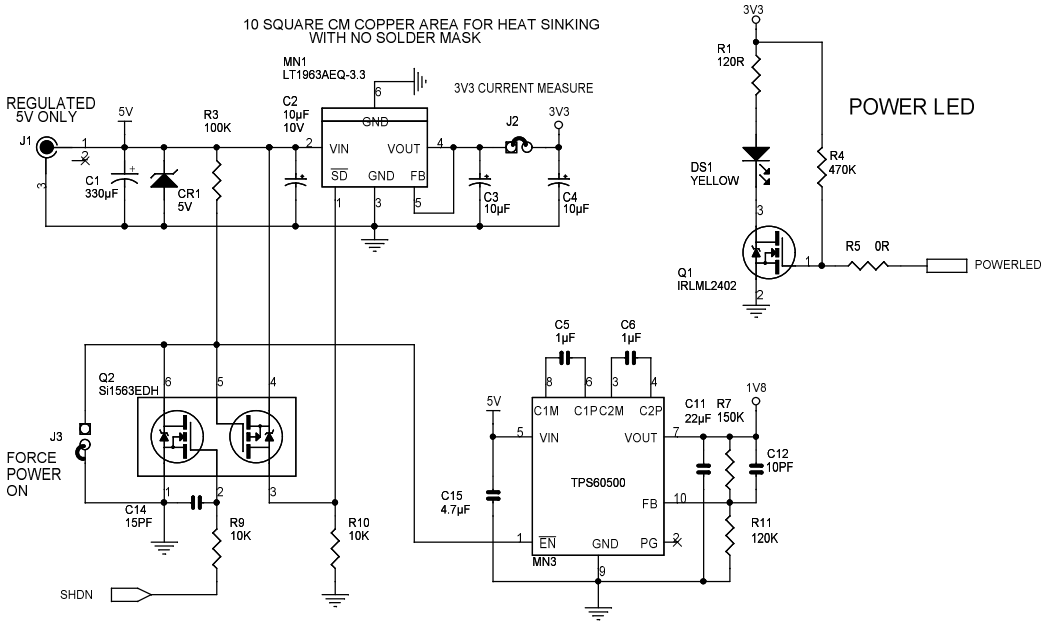

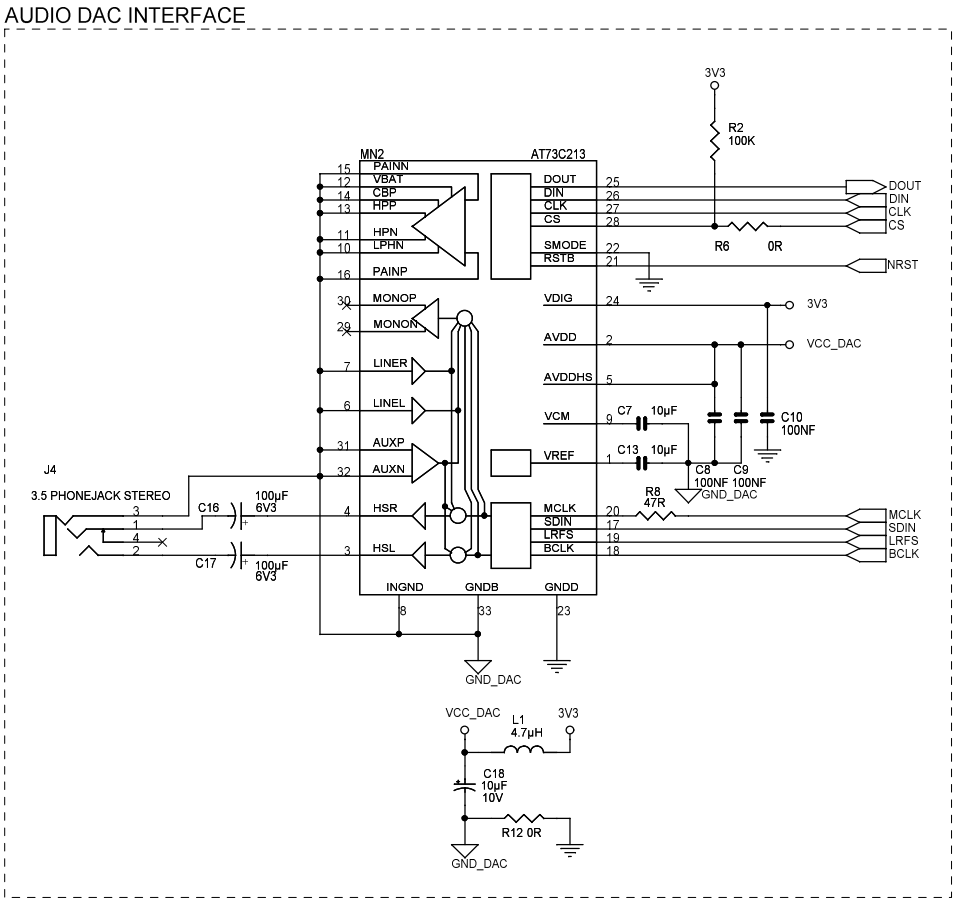

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AT91SAM9XE-EK				REV.	SHEET	
POWER SUPPLY & AUDIO	SCALE 1/1			A	2/8	

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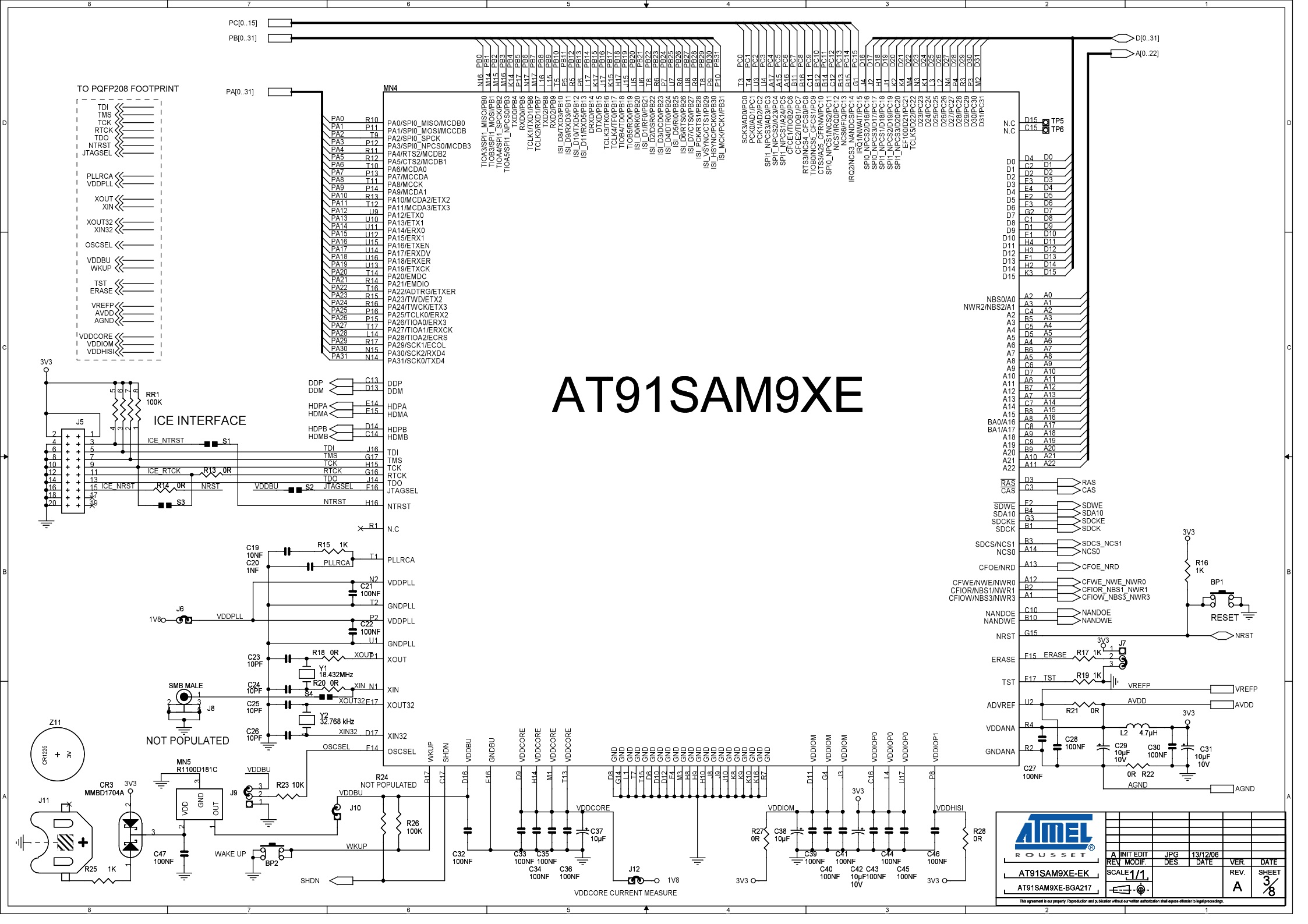
AT91SAM9XE
MN4
TO PQFP208 FOOTPRINT
ICE INTERFACE
NOT POPULATED
RESET
VDDCORE CURRENT MEASURE
SMB MALE
Y1 18.432MHz
Y2 32.768 kHz
MN5 R1100D181C
CR3 MMBD1704A
Z11
J11
J5
J6
J7
J8
J9
J10
J12
BP1
BP2
TP5
TP6
PC[0..15]
PB[0..31]
PA[0..31]
D[0..31]
A[0..22]
3V3
1V8
VDDPLL
VDDBU
VDDCORE
VDDIOM
VDDIOP0
VDDIOP1
VDDHISI
WAKE UP
SHDN
WKUP
VREFP
AVDD
AGND
ATMEL ROUSSET
AT91SAM9XE-EK
AT91SAM9XE-BGA217
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REV. A
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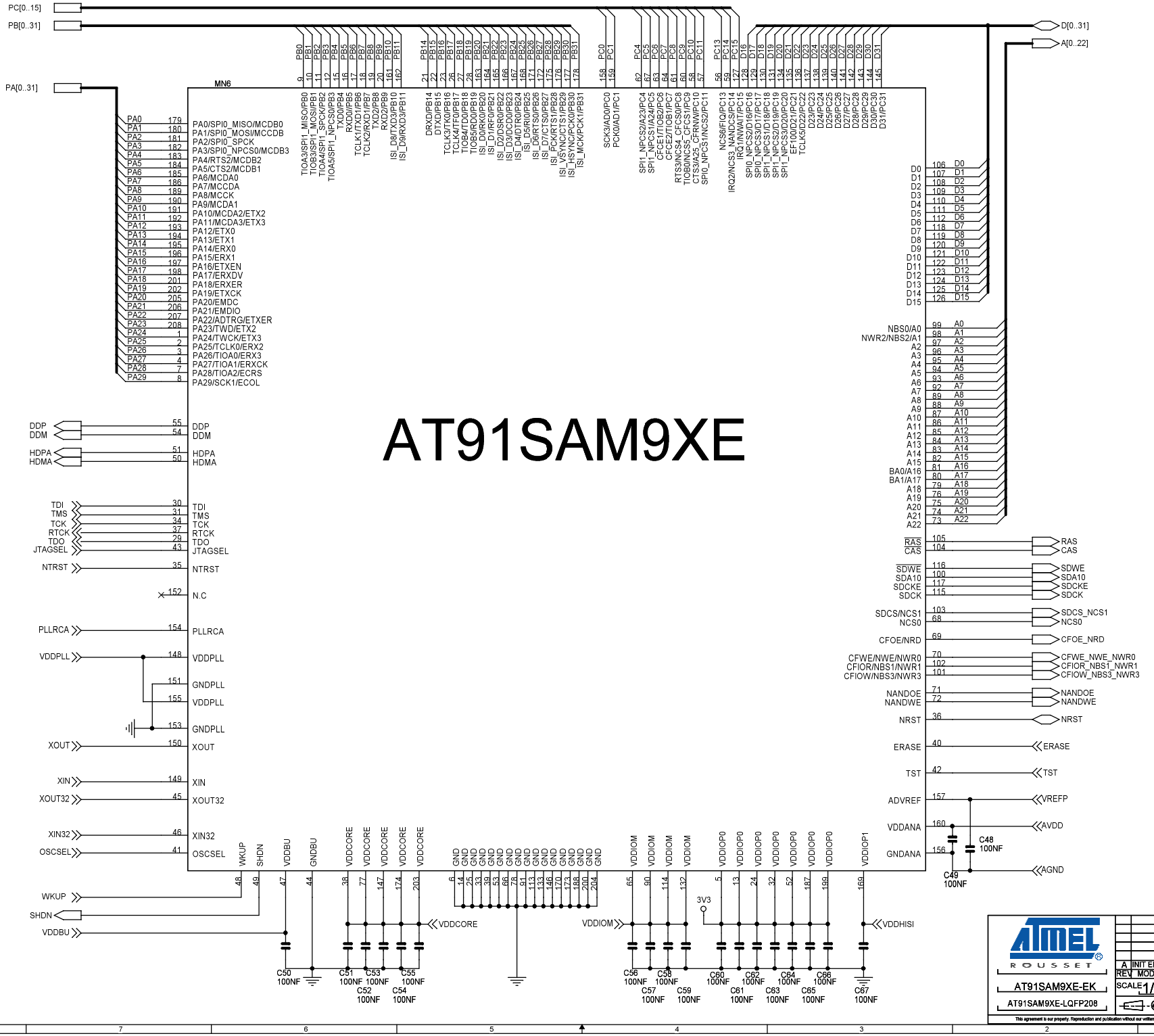
AT91SAM9XE
MN6
PC[0..15]
PB[0..31]
PA[0..31]
D[0..31]
A[0..22]
PA0/SPI0_MISO/MCDB0
PA1/SPI0_MOSI/MCCDB
PA2/SPI0_SPCK
PA3/SPI0_NPCS0/MCDB3
PA4/RTS2/MCDB2
PA5/CTS2/MCDB1
PA6/MCDA0
PA7/MCCDA
PA8/MCCK
PA9/MCDA1
PA10/MCDA2/ETX2
PA11/MCDA3/ETX3
PA12/ETX0
PA13/ETX1
PA14/ERX0
PA15/ERX1
PA16/ETXEN
PA17/ERXDV
PA18/ERXER
PA19/ETXCK
PA20/EMDC
PA21/EMDIO
PA22/ADTRG/ETXER
PA23/TWD/ETX2
PA24/TWCK/ETX3
PA25/TCLK0/ERX2
PA26/TIOA0/ERX3
PA27/TIOA1/ERXCK
PA28/TIOA2/ECRS
PA29/SCK1/ECOL
DDP
DDM
HDPA
HDMA
TDI
TMS
TCK
RTCK
TDO
JTAGSEL
NTRST
N.C
PLLRCA
VDDPLL
GNDPLL
XOUT
XIN
XOUT32
XIN32
OSCSEL
WKUP
SHDN
VDDBU
GNDBU
VDDCORE
VDDIOM
VDDIOP0
VDDIOP1
VDDHISI
3V3
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
NBS0/A0
NWR2/NBS2/A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
BA0/A16
BA1/A17
A18
A19
A20
A21
A22
RAS
CAS
SDWE
SDA10
SDCKE
SDCK
SDCS/NCS1
NCS0
CFOE/NRD
CFWE/NWE/NWR0
CFIOR/NBS1/NWR1
CFIOW/NBS3/NWR3
NANDOE
NANDWE
NRST
ERASE
TST
ADVREF
VDDANA
GNDANA
VREFP
AVDD
AGND
C48
100NF
C49
100NF
C50
100NF
C51
100NF
C52
100NF
C53
100NF
C54
100NF
C55
100NF
C56
100NF
C57
100NF
C58
100NF
C59
100NF
C60
100NF
C61
100NF
C62
100NF
C63
100NF
C64
100NF
C65
100NF
C66
100NF
C67
100NF
ATMEL
ROUSSET
AT91SAM9XE-EK
AT91SAM9XE-LQFP208
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SHEET 4/8
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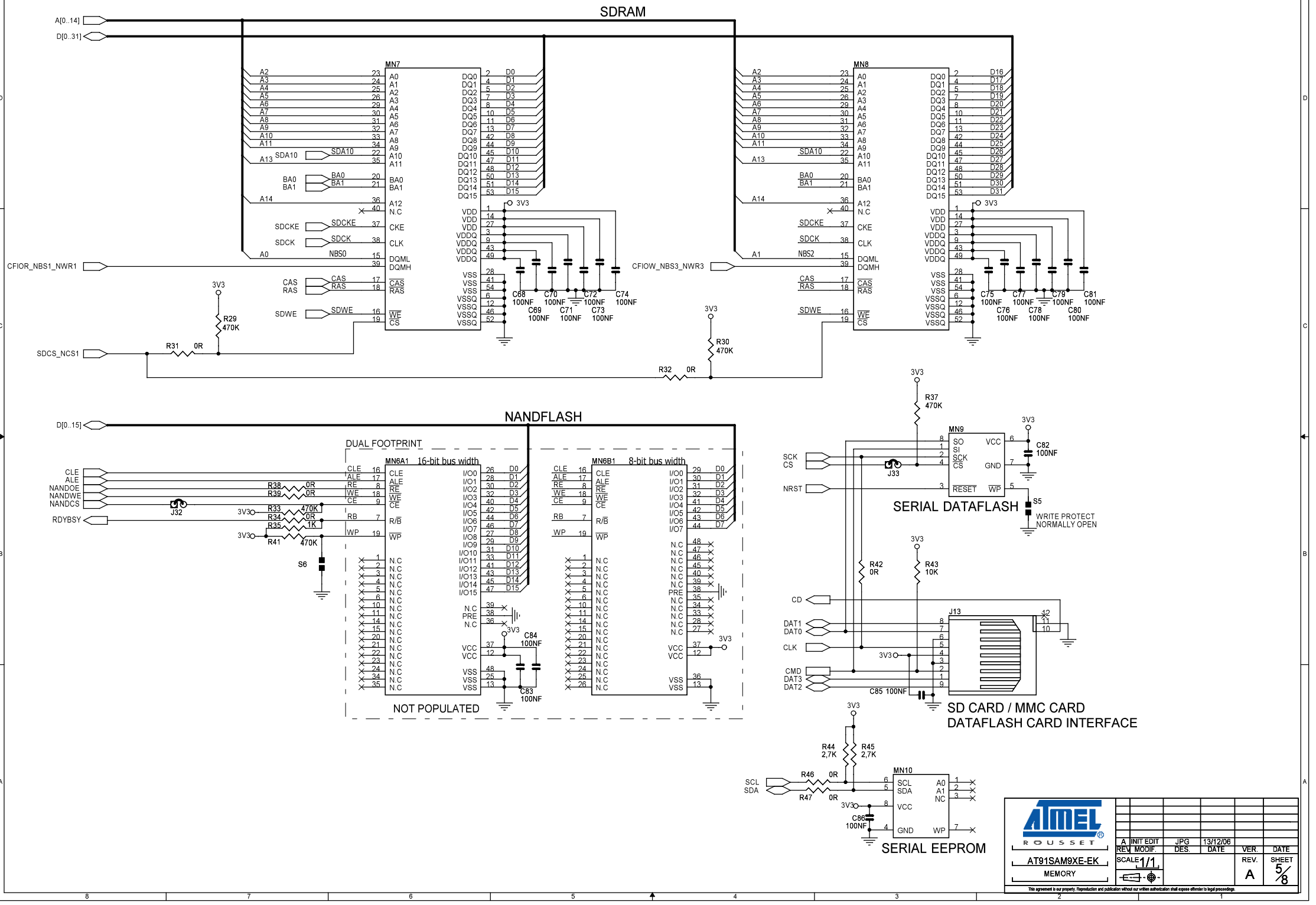
SDRAM
A[0..14]
D[0..31]
MN7
MN8
CFIOR_NBS1_NWR1
CFIOW_NBS3_NWR3
SDCS_NCS1
R29 470K
R30 470K
R31 0R
R32 0R
C68 100NF
C69 100NF
C70 100NF
C71 100NF
C72 100NF
C73 100NF
C74 100NF
C75 100NF
C76 100NF
C77 100NF
C78 100NF
C79 100NF
C80 100NF
C81 100NF
NANDFLASH
D[0..15]
DUAL FOOTPRINT
MN6A1 16-bit bus width
MN6B1 8-bit bus width
CLE
ALE
NANDOE
NANDWE
NANDCS
RDYBSY
J32
R33 470K
R34 0R
R35 1K
R38 0R
R39 0R
R41 470K
S6
C84 100NF
C83 100NF
NOT POPULATED
R37 470K
MN9
SCK
CS
NRST
J33
C82 100NF
SERIAL DATAFLASH
S5
WRITE PROTECT
NORMALLY OPEN
R42 0R
R43 10K
J13
CD
DAT1
DAT0
CLK
CMD
DAT3
DAT2
C85 100NF
SD CARD / MMC CARD
DATAFLASH CARD INTERFACE
R44 2,7K
R45 2,7K
R46 0R
R47 0R
MN10
SCL
SDA
C86 100NF
SERIAL EEPROM
ATMEL ROUSSET
AT91SAM9XE-EK
MEMORY
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REV. A
SHEET 5/8
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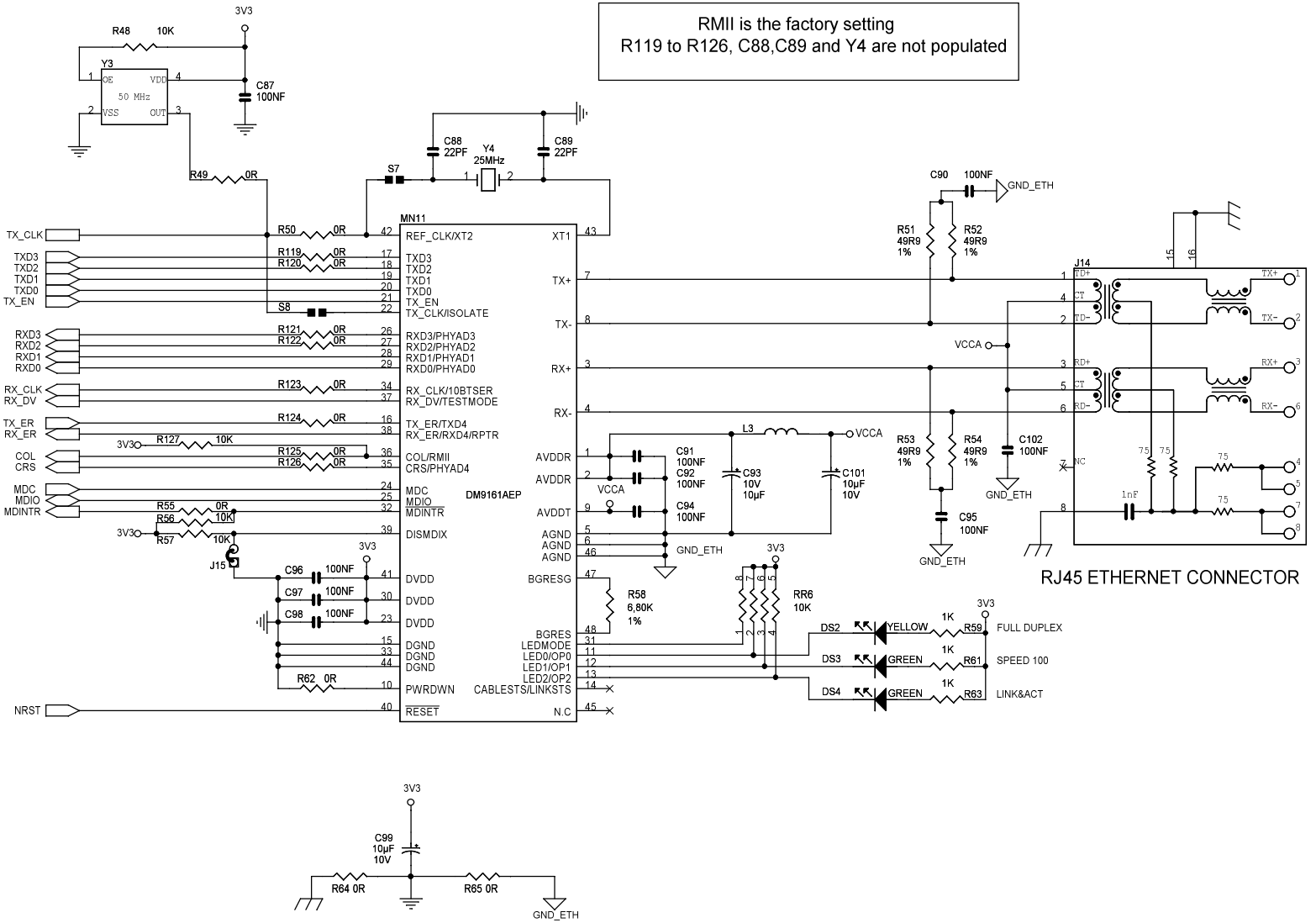
RMII is the factory setting
R119 to R126, C88,C89 and Y4 are not populated



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AT91SAM9XE-EK				REV.	SHEET
ETHERNET	SCALE 1/1			A	6/8

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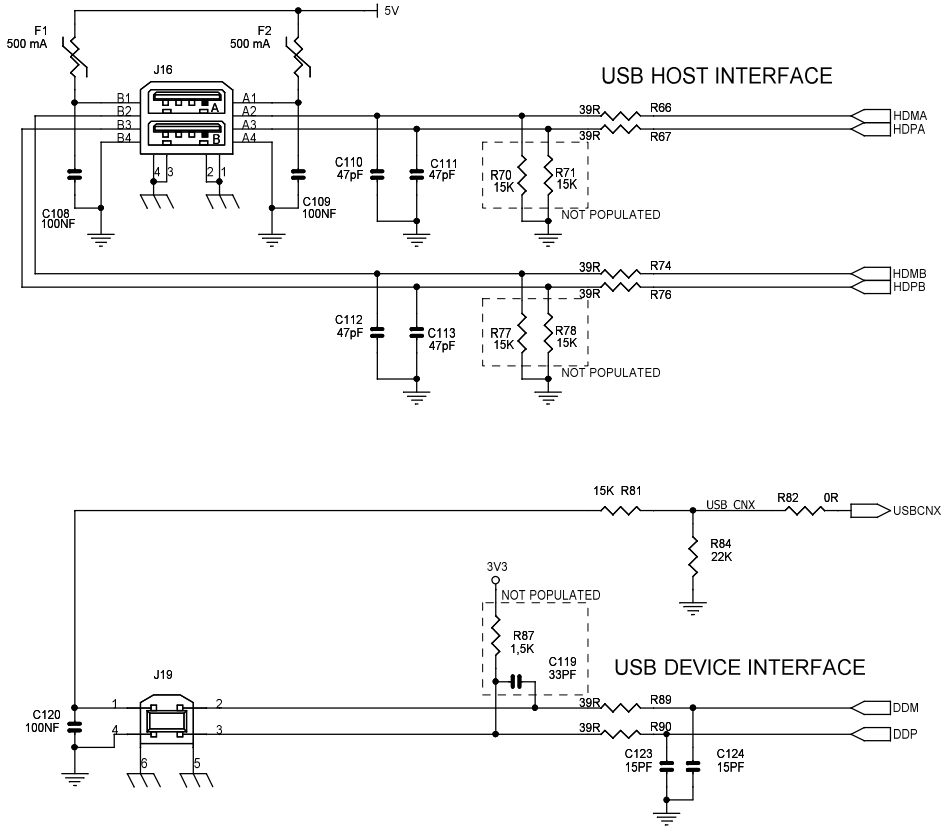

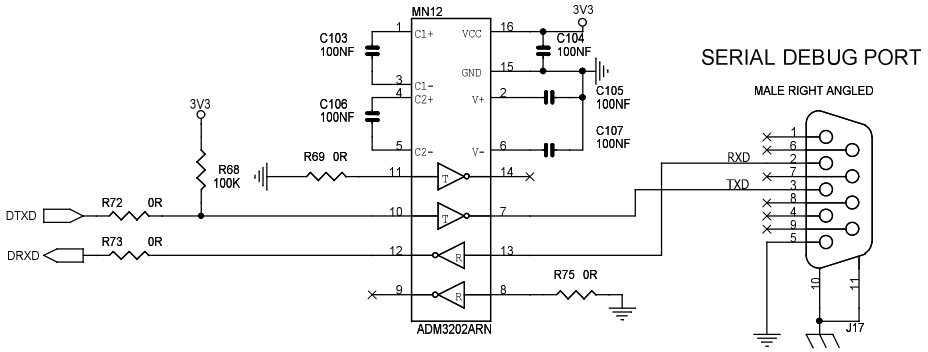

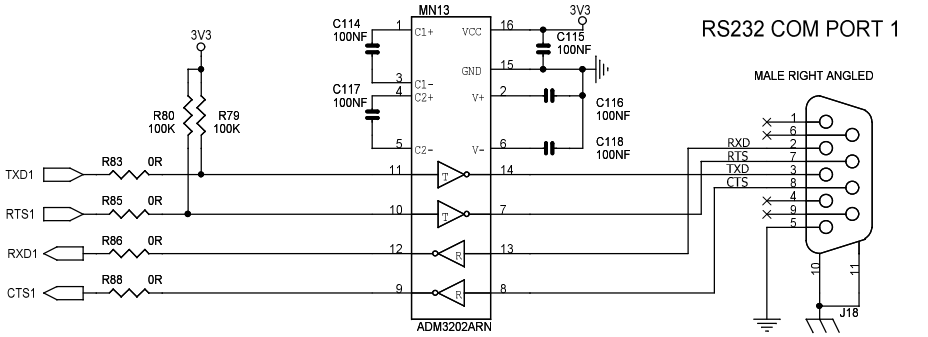

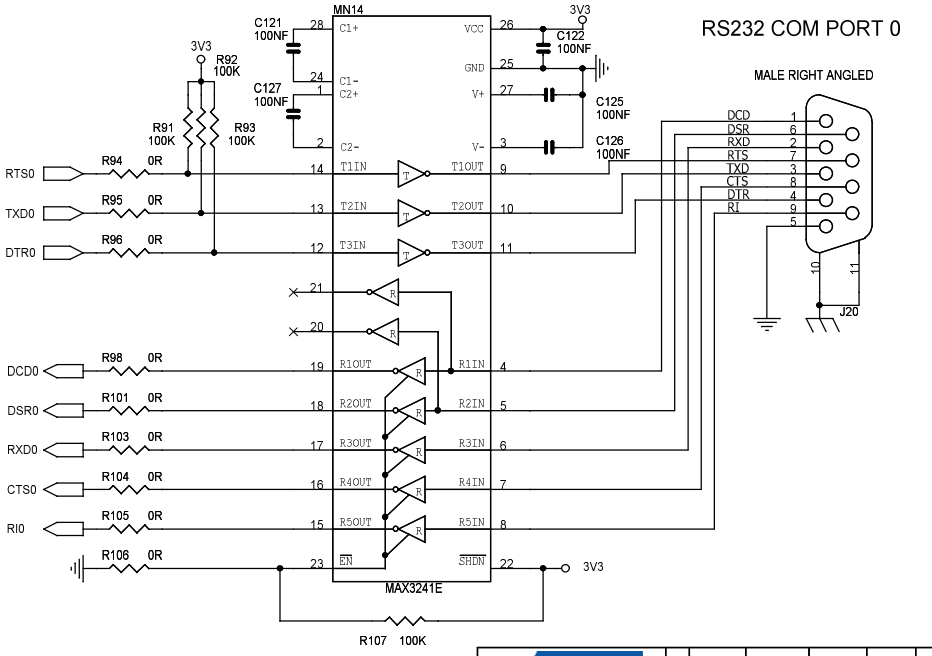

ATMEL ROUSSET

REV	MODIF.	DES.	DATE	VER.	DATE
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AT91SAM9XE-EK
SERIAL INTERFACES

SCALE 1/1

REV. A

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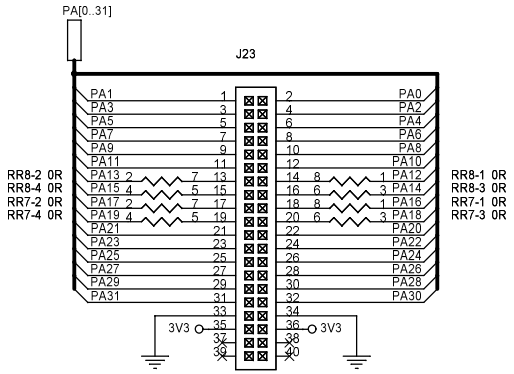
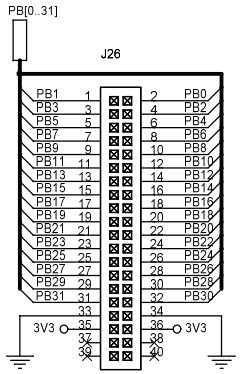


PIO A



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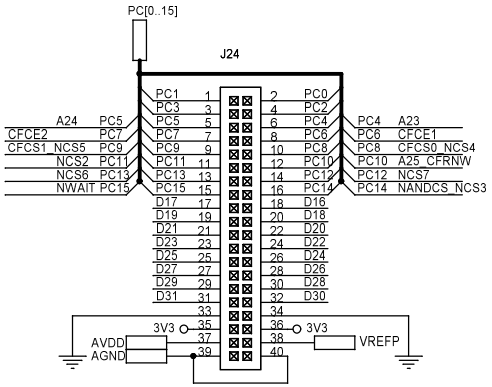


PIO C & ADC

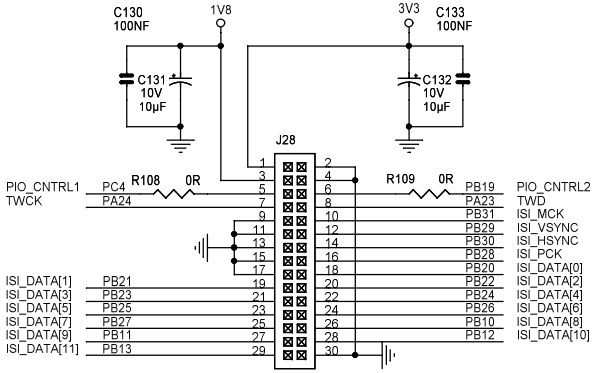
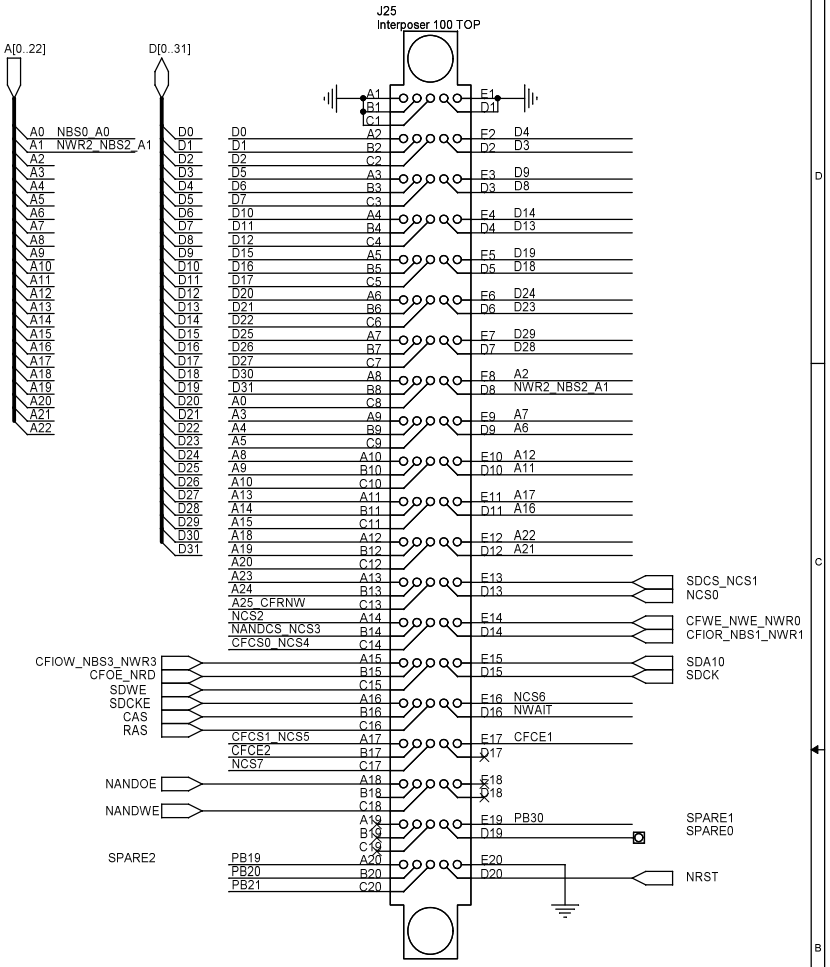


IMAGE SENSOR CONNECTOR



EBI CONNECTORS
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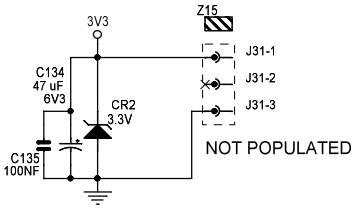
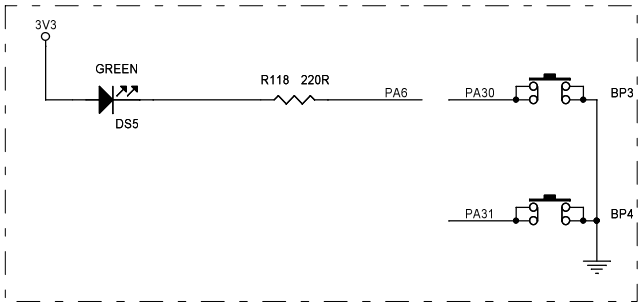


NOT POPULATED

USER INTERFACE



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EXPANSION & UI

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Section 6

Revision History

6.1 Revision History

Table 6-1.

Document	Comments	Change Request Ref.
6311A	First issue.	

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