

PIC16(L)F1508/1509 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1508/1509 family devices that you have received conform functionally to the current Device Data Sheet (DS41609A), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).


The errata described in this document will be addressed in future revisions of the PIC16(L)F1508/1509 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on [page 5](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
 - a) For MPLAB IDE 8, select *Programmer > Reconnect*.
 - b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1508/1509 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID<13:0>		
	Device ID<8:0> ⁽¹⁾	REV<4:0> Silicon Revision ⁽²⁾	
		A0	A2
PIC16F1508	10 1101 001	0 0000	0 0010
PIC16LF1508	10 1101 111	0 0000	0 0010
PIC16F1509	10 1101 010	0 0000	0 0010
PIC16LF1509	10 1110 000	0 0000	0 0010

- Note 1:** The Device ID is located in the configuration memory at address 8006h.
- 2:** Refer to the “PIC12(L)F1501/PIC16(L)F150X Memory Programming Specification” (DS41573) for detailed information on Device and Revision IDs for your specific device.

PIC16(L)F1508/1509

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾	
				A0	A2
Oscillator	HFINTOSC Ready/Stable bit	1.1	Bits remained set to '1' after initial trigger.	X	
Oscillator	Clock Switching	1.2	Clock switching fails.	X	
Oscillator	Oscillator Start-up Timer (OST) bit	1.3	OST bit remains set.	X	
Low-Dropout (LDO) Voltage Regulator	Low-Power Sleep mode	2.1	Unexpected Resets may occur at ambient temperatures below 0°C.	X	X
Fixed Voltage Reference (FVR)	Gain Amplifier Output	3.1	Use of FVR module can cause device Reset.	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: Oscillator

1.1 OSCSTAT bits: HFIOFR and HFIOFS

When HFINTOSC is selected, the HFIOFR and HFIOFS bits will become set when the oscillator becomes ready and stable. Once these bits are set they become “stuck”, indicating that HFINTOSC is always ready and stable. If the HFINTOSC is disabled, the bits fail to be cleared.

Work around

None.

Affected Silicon Revisions

A0	A2							
X								

1.2 Clock Switching

When switching clock sources between an INTOSC clock source and an external clock source, one corrupted instruction may be executed after the switch occurs.

This issue affects Two-Speed Start-up and Fail-Safe Clock Monitor operation.

Work around

When clock switching from an external oscillator clock source, first switch to 16 MHz HFINTOSC. Once running at 16 MHz HFINTOSC, configure IRCF to run at desired frequency.

When clock switching from an INTOSC to an external oscillator clock source, first switch from desired INTOSC frequency to HFINTOSC High-Power mode (8 MHz or 16 MHz). Once running from HFINTOSC, switch to the external oscillator clock source.

Affected Silicon Revisions

A0	A2							
X								

1.3 Oscillator Start-up Timer (OST) bit

During the Two-Speed Start-up sequence, the OST is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set, the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as the primary clock and Fail-Safe Clock mode is enabled (FCMEN = 1), any of the following conditions will result in the Oscillator Start-up Timer (OST) failing to restart:

- MCLR Reset
- Wake from Sleep
- Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators which take longer than the clock failure time-out period to start.

Work around

None.

Affected Silicon Revisions

A0	A2							
X								

2. Module: Low-Dropout (LDO) Voltage Regulator

2.1 Low-Power Sleep mode at Ambient Temperatures Below 0°C

Under the following conditions:

- ambient temperatures below 0°C
- while in Sleep mode
- VREGCON configured for Low-Power Sleep mode (VREGPM = 1)

On very rare occasions, the LDO voltage will drop below the minimum VDD, causing unexpected device Resets.

Work around

For applications that operate at ambient temperatures below 0°C, use the LDO voltage regulator in Normal-Power mode (VREGPM = 0).

Affected Silicon Revisions

A0	A2							
X	X							

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3. Module: Fixed Voltage Reference (FVR)

3.1 Gain Amplifier Output

When using the FVR module, if the gain amplifier outputs are set via the CDAFVR or ADFVR bits in FVRCON while the module is disabled (FVREN = 0), the internal oscillator frequency may shift, device current consumption can increase, and a Brown-out Reset may occur.

Work around

Set the FVREN bit of FVRCON to enable the module prior to adjusting the amplifier output selections with the CDAFVR and ADFVR bits. If switching from the 4x output setting to the 1x output setting, select the 2x output setting as an intermediary step. Always set the amplifier output selections to off ('00') before disabling the FVR module.

Affected Silicon Revisions

A0	A2						
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41609A):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Oscillator

5.5 Fail-Safe Clock Monitor

5.5.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a `SLEEP` instruction or changing the SCS bits of the `OSCCON` register. When the SCS bits are changed, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in `OSCCON`. When the OST times out, the Fail-Safe condition is cleared **after successfully switching to the external clock source. The OSFIF bit should be cleared prior to switching to the external clock source. If the Fail-Safe condition still exists, the OSFIF flag will again become set by hardware.**

2. Module: Electrical Specifications

29.8 AC Characteristics: PIC16(L)F1508/9

TABLE 29-2: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$								
Param. No.	Sym.	Characteristic	Freq. Tolerance	Min.	Typ†	Max.	Units	Conditions
OS08	HFosc	Internal Calibrated HFINTOSC Frequency ⁽¹⁾	$\pm 2\%$	—	16.0	—	MHz	$V_{DD} = 3.0\text{V}$ at 25°C (Note 2)
OS09	LFosc	Internal LFINTOSC Frequency	—	—	31	—	kHz	(Note 3)
OS10*	TIOsc ST	HFINTOSC Wake-up from Sleep Start-up Time	—	—	5	15	μs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, V_{DD} and V_{SS} must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

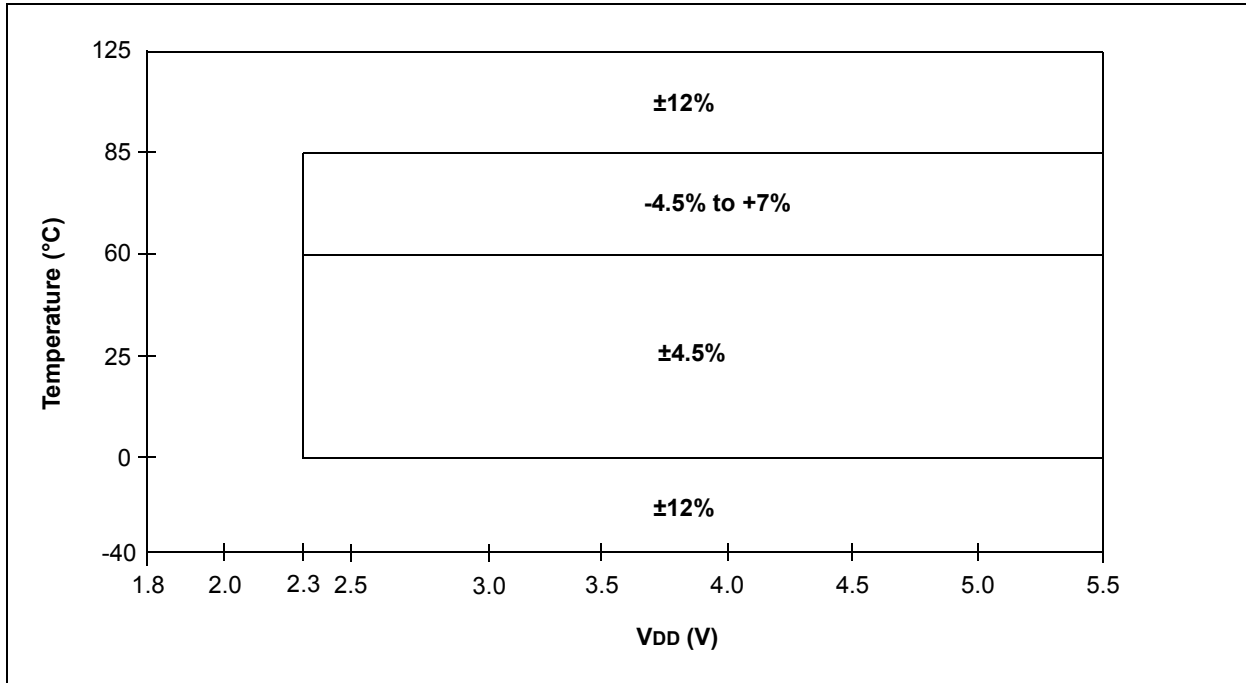
2: See [Figure 29-3](#), HFINTOSC Frequency Accuracy over Device V_{DD} and Temperature, [Figure 30-73](#), HFINTOSC Accuracy Over Temperature, $V_{DD} = 1.8\text{V}$, PIC16LF1508/9 Only, and [Figure 30-74](#), HFINTOSC Accuracy Over Temperature, $2.3\text{V} \leq V_{DD} \leq 5.5\text{V}$.

3: See [Figure 30-71](#), LFINTOSC Frequency over V_{DD} and Temperature, PIC16LF1508/9 Only, and [Figure 30-72](#), LFINTOSC Frequency over V_{DD} and Temperature, PIC16F1508/9.

[Figure 29-3](#) and [Figures 30-71](#) through [30-74](#) were added for [Table 29-2](#) reference.

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FIGURE 29-3: HFINTOSC FREQUENCY ACCURACY OVER DEVICE V_{DD} AND TEMPERATURE



30.0 DC and AC Characteristics Graphs and Charts

FIGURE 30-71: LFINTOSC FREQUENCY OVER V_{DD} AND TEMPERATURE, PIC16LF1508/1509 ONLY

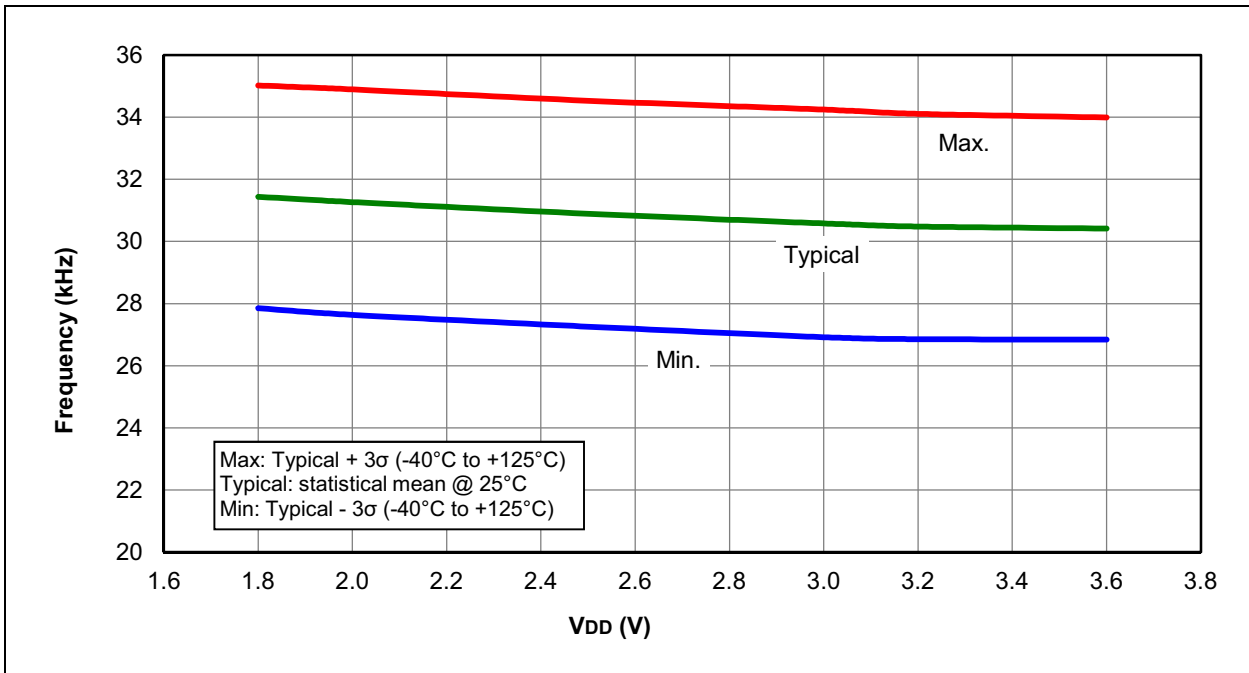
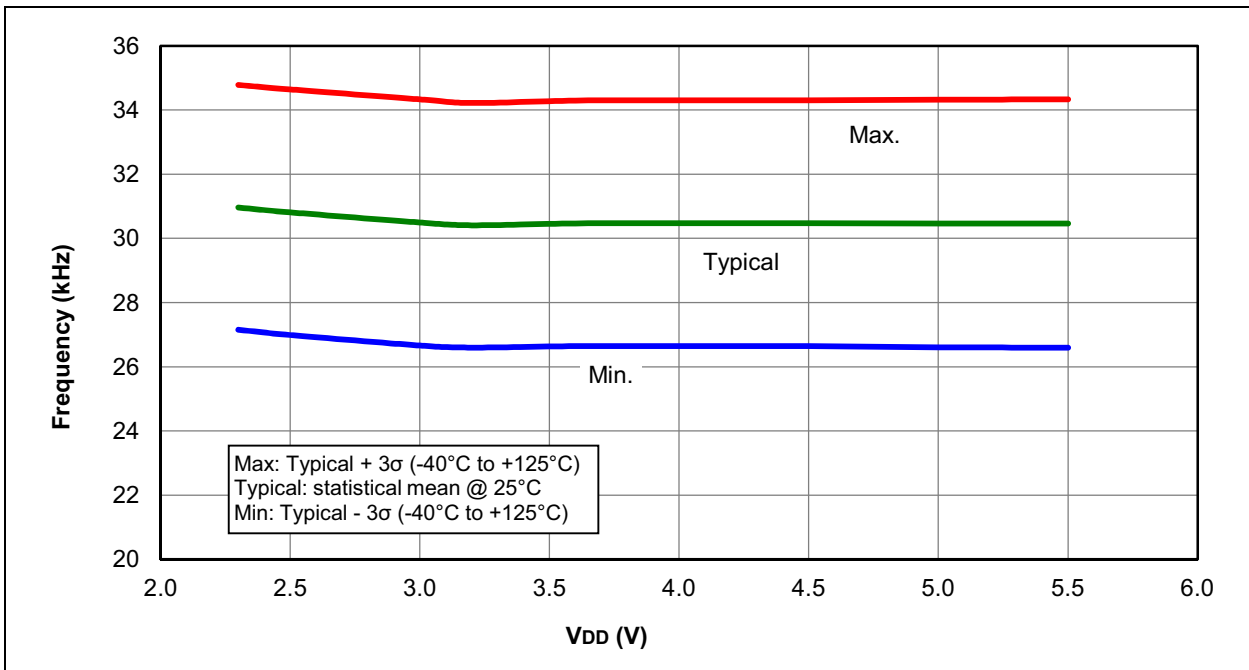


FIGURE 30-72: LFINTOSC FREQUENCY OVER V_{DD} AND TEMPERATURE, PIC16F1508/1509 ONLY



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**FIGURE 30-73: HFINTOSC ACCURACY OVER TEMPERATURE, $V_{DD} = 1.8V$
PIC16LF1508/1509 ONLY**

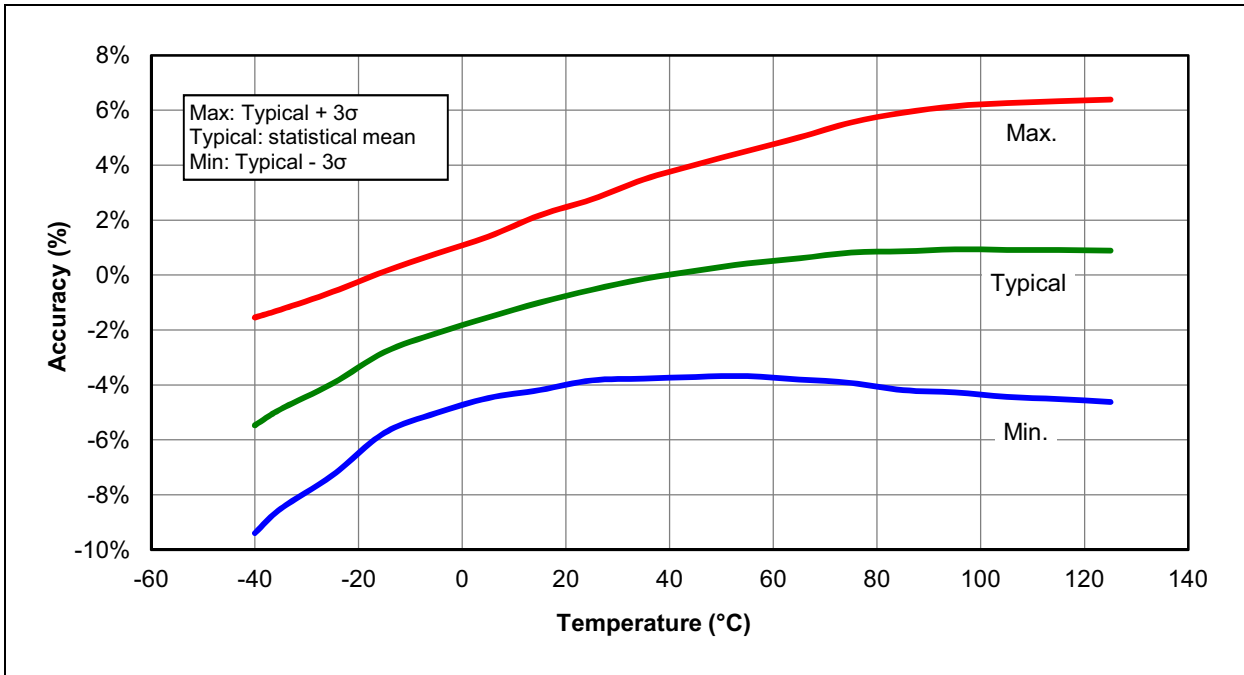
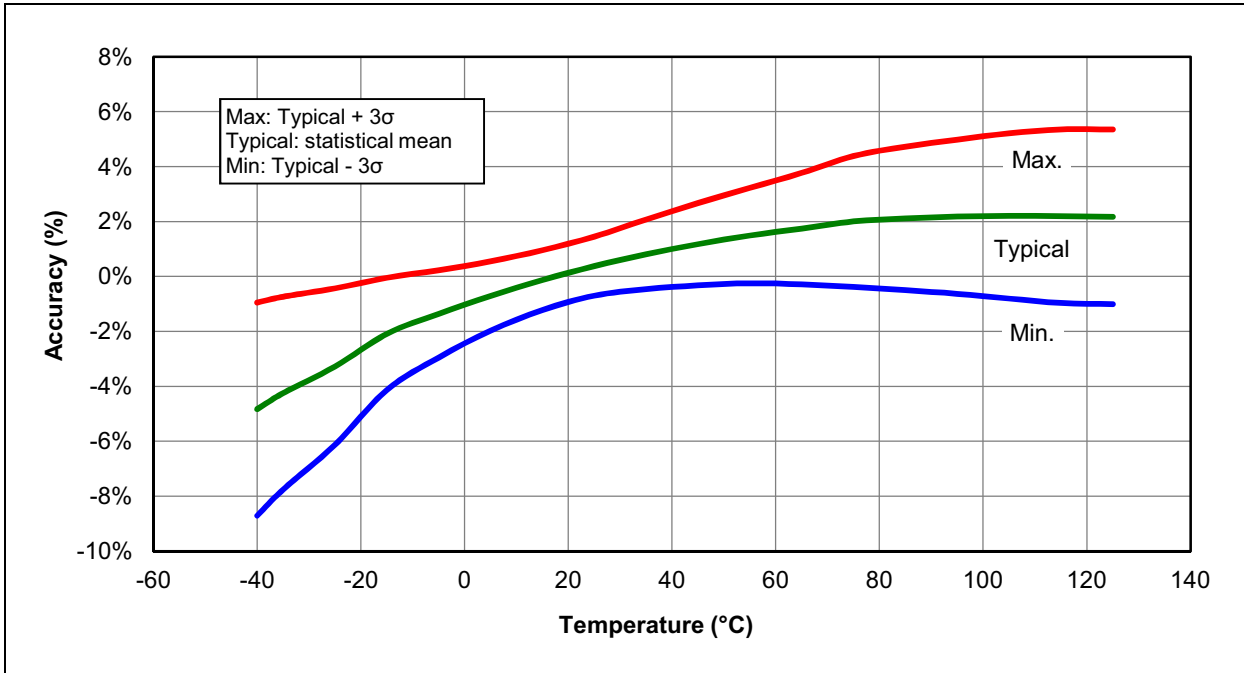


FIGURE 30-74: HFINTOSC ACCURACY OVER TEMPERATURE, $2.3V \leq V_{DD} \leq 5.5V$



APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (02/2012)

Initial release of this document.

Rev B Document (06/2012)

Added MPLAB X IDE; Updated Module 1.2.

Data Sheet Clarifications:

Added Module 2: Electrical Specifications/
AC Characteristics.

Rev C Document (07/2012)

Added Modules 2 and 3.

Rev D Document (01/2013)

Added Silicon Revision A2.

Data Sheet Clarifications:

Updated Module 2, Electrical Specifications.

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NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

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