CMOS ISCC™ INTEGRATED SERIAL COMMUNICATIONS CONTROLLER

Z16C35

Product Brief

PB006502-0608

FEATURES

- Low Power CMOS Technology
- Two General-Purpose SCC Channels, Four DMA Channels; and Universal Bus Interface Unit.
- Software Compatible to the Zilog CMOS SCC
- Four DMA Channels; Two Transmit and Two Receive Channels to and from the SCC
- Four Gigabyte Address Range per DMA Channel
- Fly-by DMA Transfer Mode
- Programmable DMA Channel Priorities
- Independent DMA Register Set
- A Universal Bus Interface Unit Providing Simple InterfacetoMostCPUs MultiplexedorNon-Multiplexed Bus; Compatible with 680x0 and 8x86 CPUs.
- 32-Bit Addresses Multiplexed to 16-Pin Address/Data Lines
- 68-Pin PLCC
- Supports all Zilog CMOS SCC Features.
- Two Independent, 0 to 4.0 Mbit/sec, Full-Duplex Channels, each with a Separate Crystal Oscillator, BaudRate Generator, andDigital Phase-Locked Loop Circuit for Clock Recovery.
- Multi-Protocol Operation Under Program Control; Programmable for NRZ, NRZI, or FM Data Encoding.
- Asynchronous Mode with Five to Eight Bits and One, One and One-Half, or Two Stop Bits Per Character; Programmable Clock Factor; Break Detection and Generation; Parity, Overrun, and Framing Error Detection.
- Synchronous Mode with Internal or External Character Synchronization on One or Two Synchronous Characters and CRC Generation and Checking with CRC-16 or CRC-CCITT Preset to Either 1's or 0's.
- SDLC/HDLC Mode with Comprehensive Frame-Level Control, Automatic Zero Insertion and Deletion, I-Field Residue Handling, Abort Generation and Detection, CRCGeneration and Checking, andSDLC Loop Mode Operation.
- Full CMOS SCC Register Set
- 10 and 16 MHz Speeds Suitable for T1 Full Duplex Operation

General Description

The Z16C35 ISCC™ is a CMOS Superintegrated device with a flexible Bus Interface Unit (BIU) connecting a built-in Direct Memory Access (DMA) cell to the CMOS Serial Communications Control (SCC) cell.

The ISCC is a dual-channel, multi-protocol data communications peripheral which easily interfaces to CPUs with either multiplexed or non-multiplexed address and data buses. The advanced CMOS process offers lower power consumption, higher performance, and superior noise immunity. The programming flexibility of the internal registers allow the ISCC to be configured for a wide variety of serial communications applications. The many on-chip features such as, streamlined bus interface, four channel DMA, baud rate generators, digital phase-locked loops, and crystal oscillators dramatically reduce the need for external logic.

The ISCC can address up to 4 gigabytes per DMA channel by using the /UAS and /AS signals to strobe out 32-bit multiplexed addresses.

The ISCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC.

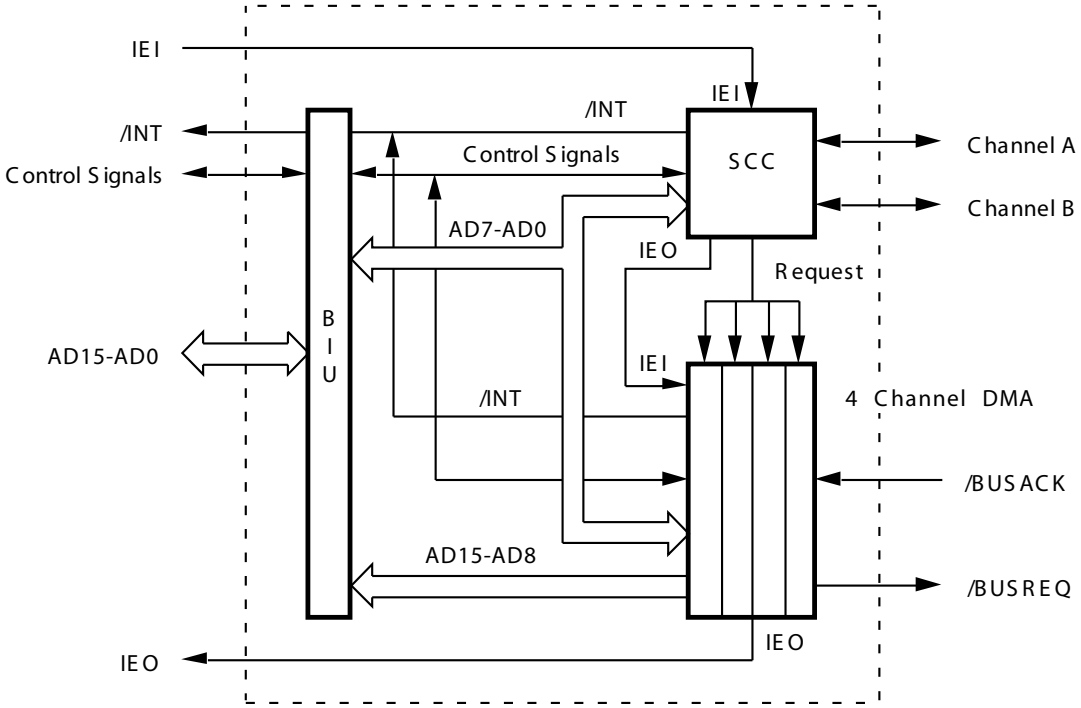

Figure 1. Z16C35 Functional Block Diagram

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